Ixia Platform Reference Manual

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For viewing the FAQs related to the product, go to Ixia Technical Support Online:

https://ebsoprod.ixiacom.com/OA_HTML/jtflogin.jsp

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About This Guide

The information in this section is provided to help you navigate this guide and make better use of its content. A list of related documents is also included.

Purpose

This guide provides information about Ixia hardware theory, features, functions, and options, as well as additional test setup details.

Manual Content

This guide contains the following sections:

Section	Description
About This Guide	Provides information on this manual, including its purpose, content, and related documentation. Also explains how to contact technical support.
Chapter 1, *Platform and Reference Overview*	Provides a basic overview of Ixia hardware and theory of operation. Hardware includes descriptions of all supported chassis and load modules.
Chapter 2, *Theory of Operation: General*	Provides a general overview of the various technologies used in both IxExplorer and in the IxOS.
Chapter 3, *Theory of Operation: Protocols*	Provides a general overview of the various technologies used in IxNetwork and IxRouter.
Chapter 4, *Optixia XM12 Chassis*	Provides a detailed description of the features and systems of the Optixia XM12 chassis.
Chapter 5, *Optixia XM2 Chassis*	Provides a detailed description of the features and systems of the Optixia XM2 chassis.
Chapter 6, *XG12 Chassis*	Provides a detailed description of the features and systems of the XG12 chassis.
Chapter 7, *Optixia X16 Chassis*	Provides a detailed description of the features and systems of the Optixia X16 chassis.

Section	Description
Chapter 8, *Optixia XL10 Chassis*	Provides a detailed description of the features and systems of the Optixia XL10 chassis.
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Chapter 14, *Ixia GPS Auxiliary Function Device (AFD1)*	Provides a detailed description of the features and systems of the Ixia Auxiliary Function Device (AFD1).
Chapter 15, *Ixia IRIG-B Auxiliary Function Device (AFD2)*	Provides a detailed description of the features and systems of the Ixia IRI-B Auxiliary Function Device (AFD2).
Chapter 16, *IXIA 10/100/1000 Load Modules*	Provides a detailed description of the features and capabilities of 10/100/1000 Ethernet load modules.
Chapter 17, *IXIA 1GbE and 10GbE Aggregation Load Modules*	Provides a detailed description of the features and capabilities of 1 Gigabit Ethernet and 10GbE aggregation load modules.
Chapter 18, *IXIA Network Processor Load Modules*	Provides a detailed description of the features and capabilities of Xcellon-Ultra NP and Xcellon-Ultra XP load modules. It also provides card specifications and description of features when Xcellon-Ultra card is used in IxN2X mode with added IxN2X capability. The card is reported as Xcellon-Ultra NG by IxExplorer when it is running in IxN2X mode. Xcellon-Ultra NP, Xcellon-Ultra XP, and Xcellon-Ultra NG are all physically similar.
Chapter 19, *IXIA 40/100 Gigabit Ethernet Load Modules*	Provides a detailed description of the features and capabilities of 40 and 100 Gigabit Ethernet load modules.
Chapter 20, *IXIA 10 Gigabit Ethernet Load Modules*	Provides a detailed description of the features and capabilities of 10 Gigabit Ethernet load modules.
Chapter 21, *IXIA 10GE LAN/WAN and OC 192 POS Load Modules*	Provides a detailed description of the features and capabilities of OC192c Optical Carrier load modules.
Chapter 22, *IXIA OC12 ATM/POS Load Modules*	Provides a detailed description of the features and capabilities of ATM load modules.
Chapter 23, *IXIA 10/100 Load Modules*	Provides a detailed description of the features and capabilities of 10/100 Ethernet load modules.
Chapter 24, *IXIA 100 Load Modules*	Provides a detailed description of the features and capabilities of 100 Ethernet load modules.

Section	Description
Chapter 25, *IXIA Gigabit Load Modules*	Provides a detailed description of the features and capabilities of Gigabit Ethernet load modules.
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Chapter 31, *IXIA Impairment Load Modules*	Provides a detailed description of the features and capabilities of Xdensity (XDM10G32S) load module.
Chapter 32, *IXIA Xcellon-Lava Load Modules*	Provides a detailed description of the features and capabilities of Xcellon-Lava load module.
Chapter 33, *IXIA Power over Ethernet Load Modules*	Provides a detailed description of the features and capabilities of Power over Ethernet load modules.
Chapter 34, *IXIA Stream Extraction Modules*	Provides a detailed description of the features and capabilities of Ethernet Stream Extraction load modules.
Chapter 35, *IxVM*	Provides a detailed description of the features and capabilities of IxVM load modules.
Appendix A, *XAUI Connector Specifications*	Provides a detailed description of various XAUI connectors provided by Ixia for various modules.
Appendix B, *Available Statistics*	Lists all the statistics, by module and by technology, collected by Ixia hardware.
Appendix C, *GPS Antenna Installation Requirements*	Describes the recommended installation method for an IXIA GPS Antenna.
Appendix D, *Hot-Swap Procedure*	Describes the procedure for removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis.
Index	Provides a comprehensive index listing for the manual.

Related Documentation

The following guides help you learn more about the hardware for IxOS. The guides are available on the CD shipped with the application, as well as on the Ixia Website at www.ixiacom.com.

- *IxExplorer User Guide*: Provides details on the usage of the IxExplorer GUI for operation with an Ixia chassis and Ixia load modules.

- *IxServer User Guide*: Provides details on the usage of the IxServer GUI for operation on an Ixia chassis.
- *IxOS Tcl Development Guide:* Provides details on the structure and conventions of the IxExplorer Tcl API and provides detailed information on all API commands.
- Ixia online Glossary of technical terms is located at www.ixiacom.com/glossary/.

Technical Support

You can obtain technical support for any Ixia product by contacting Ixia Technical Support by any of the methods mentioned on the inside cover of this manual. Technical support from Ixia's corporate headquarters is available Monday through Friday from 06:00 to 18:00, UTC (excluding American holidays). Technical support from Ixia's EMEA and India locations is available from Monday through Friday, 08:00 to 17:00 local time (excluding local holidays).

Notes, Cautions, Warnings

Power Cords

Power cords that are included in shipments of Ixia equipment meet the approved/recognized standards of the national safety organization(s) of the destination country.

Battery Replacement

Caution: Danger of explosion if battery is incorrectly replaced. You should not attempt to replace the battery.

Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.

Ventilation Requirements

The following caution applies to equipment installed into equipment racks.

Caution: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced.
Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

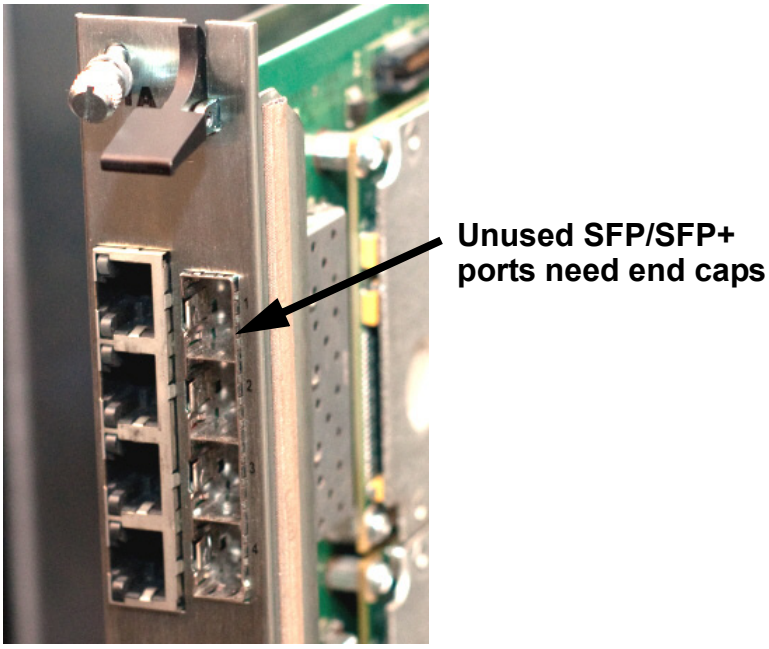
Use End Caps on Open Ports

The metal edges of the SFP port are sharp. To avoid injury, always keep unused SFP ports covered with end caps. When installing a load module into a chassis or removing from a chassis, ensure that end caps are in place on unused ports.

Warning: To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports uncovered. When transceivers are not installed, end caps must be used.

Figure 1-1 shows the precautionary measure to be taken while handling unused SFP/SFP+ Ports in the laboratory.

Figure 1-1. Unused Ports



Affected load modules include the following:

- NGY with SFP+ interface, 2/4/8-port, all models
- Dual PHY SFF cards with RJ45 and SFP Gigabit (TXS and STXS)
- Xcellon-Ultra NP, XP, and NG
- LSM1000XMV 4/8/12/16-port
- LSM1000XMS
- ASM1000XMV
- AFM1000SP
- ELM1000ST

Use Ejector Tabs Properly

Ejector tabs on load modules are to be used only to eject a load module from the chassis backplane connector. They are not designed to support the weight of the

load module. Ejector tabs can bend or break if used improperly as handles to push, pull, or carry a load module.

Caution: Do not use ejector tabs as handles to support a load module while installing and seating into the chassis. The ejector tabs are to be used only to eject the module from the chassis backplane connector.

China RoHS Declaration Table—Chassis

零件项目(名称) (Component Name)	有毒有害物质或元素(Hazardous Substances or Elements)					
	铅 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Chromium VI Compounds (Cr6+)	多溴联苯 Poly-brominated Biphenyls (PBB)	多溴二苯醚 Poly-brominated Diphenyl Ethers (PBDE)
印制电路配件 (Printed Circuit Assemblies)	X	O	O	O	O	O
内部线路 (Internal wiring)	X	O	O	O	O	O
底架 (Chassis)	O	O	O	O	O	O
金属外壳 (Metal Enclosure)	O	O	O	O	O	O
螺帽,螺钉(栓),螺旋(钉),垫圈, 紧固件 (Nuts, bolts, screws, washers, Fasteners)	O	O	O	O	O	O
电源供应器 (Power Supply Unit)	O	O	O	O	O	O
风扇 (Fan)	O	O	O	O	O	O
正面(前)面板 (Front panel)	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006标准规定的限量要求以下.
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006标准规定的限量要求.
X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.

1 Platform and Reference Overview

The Ixia system is the most comprehensive tool available for testing multilayer 10/100 Mbps Ethernet, Ethernet Gigabit, 10 Gigabit Ethernet, ATM, and Packet over SONET switches, routers, and networks.

The Ixia product family includes chassis, load modules, the Ixia IxExplorer software program, and optional Tcl scripts and related software. A chassis can be configured with any mix of load modules, and multiple chassis can be daisychained and synchronized to support very large and complex test environments. The Ixia IxExplorer software provides complete configuration, control, and monitoring of all Ixia resources in the test network, and the Tcl scripts allow to rapidly conduct the most popular industry benchmark tests.

The Optixia XM12 provides high port density and hot swappable capability. The Optixia XM2 provides hot-swappable capability in a more portable format. The Optixia X16 chassis also provides hot-swappable capability for up to 16 load modules.

The Optixia XL10 offers the highest port density with support for up to 240 Gigabit Ethernet ports and 54 10-GbE ports in a single chassis. Other chassis models are the IXIA 400T (supports up to four load modules), the IXIA 250 (supports one built-in module and two extra modules), and IXIA 100 (supports one card). Depending on network technology, one to 48 ports can be packaged on a card. A card is also referred to as a load module. For most media, any combination of load modules may be included in a single chassis. The highly scalable architecture supports daisy-chaining of up to 256 chassis that may be locally synchronized. Thus, even the most complex systems can be tested thoroughly and cost-effectively.

You can configure and control the unit directly through connections to a keyboard, mouse, monitor, and printer. Also, the unit can be connected to an Ethernet network, and an administrator can remotely monitor and control it using the IxExplorer software program. Multiple users can access the unit simultaneously, splitting the ports within a chassis and controlling the activity and configuration of all ports and functions.

Front panel displays give immediate indication of link state, transmission or reception of packets, and error conditions.

Ixia produces a number of load modules which provide data transmission and reception capabilities for a variety of Ethernet, ATM, and Packet Over Sonet (POS) speed and technologies. These load modules reside in an Ixia chassis, which provide different numbers of load module slots and power. This chapter introduces the Ixia hardware components. The Ixia chassis and load modules are compared and contrasted.

Ixia Chassis

The following Ixia chassis are currently available for sale:

- *XG12 Chassis*: The XG12 Chassis is the next generation high performance chassis platform capable of supporting next generation load modules. It is a 12 slot chassis with increased power and airflow delivery along with reservations for increased performance to the card. The 12-slot platform allows for higher port density load modules.
- *Optixia XM12 Chassis*: Capable of holding up to 12 Ixia load modules and equipped with extra power and fans required for high-powered load modules. Supports higher port density. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules. An optional Sound Reducer (PN 943-0021) can be installed on the rear of the XM12 chassis, to reduce the fan noise by approximately 10 dB. The XM12 High Performance version (PN OPTIXIAXM12-02) has two 2.0 kW power supply; the standard XM12 version has two 1.6 kW power supply.
- *Optixia XM2 Chassis*: Capable of holding two Ixia load modules and equipped with extra power and fans required for some high-powered load modules. Supports higher port density. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules.
- *Optixia X16 Chassis*: Capable of holding up to 16 Ixia load modules and equipped with extra power and fans required for some high-powered load modules. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules.
- *Optixia XL10 Chassis*: Capable of holding a combination of high-density Ixia load modules with 24 ports. It supports up to 240 10/100/1000 Mbps ports. It is equipped with redundant power supplies. Modules can be inserted and removed from the chassis without shutting the chassis down, and a load module can be removed without impacting the processes of other load modules. The Optixia XL10 chassis includes sufficient power and airflow to support high-powered load modules.
- *IXIA 400T Chassis*: Capable of holding up to four Ixia load modules and equipped with extra power and fans required for some high-powered load modules.

- *IXIA 250 Chassis*: A portable Field Service Unit (FSU) which includes a single port (either copper 10/100/1000 or fiber 1000) and capable of holding up to two additional Ixia load modules. May optionally be equipped with a built-in CDMA receiver.

The following Ixia chassis are no longer available for sale:

- *IXIA 1600T Chassis*: Capable of holding up to 16 Ixia load modules and equipped with extra power and fans required for some high-powered load modules.
- *Ixia 100 Chassis*: The IXIA 100 is capable of holding one Ixia load module and includes a built-in GPS or CDMA receiver.

All Ixia chassis have the ability to hold one or more standard load modules. Ixia load modules provide media dependent and independent ports to Devices Under Test (DUTs). Any of the chassis may be daisy-chained and provide synchronized operations. The IXIA 100 chassis includes timing provisions based on GPS which allows accurate worldwide synchronization without local inter-chassis connections.

Each chassis contains a self-contained computer running Windows XP Professional™ and includes a 10/100/1000MB network interface and local disk. They may include a floppy drive, a CD-ROM drive, or DVD-ROM drive. A chain of chassis may be controlled through a monitor, keyboard, and mouse directly connected to any of the chassis or remotely through the network interface card. Multiple users may safely share ports in a chassis chain. Several of the high-end load modules consume more power and generate additional heat. Only a limited number of such modules may be used in selected chassis. The basic characteristics of these chassis are compared in *Table 1-1* on page 1-3. The process of initial chassis configuration is explained in *Chapter 1, Platform and Reference Overview*. Each chassis is further described in its own chapter.

Table 1-1. Ixia Chassis Comparison

Chassis	# of slots	Special Feature	Mounting
XG12	12	The XG12 Chassis is the next generation high performance chassis platform capable of supporting next generation load modules. It is a 12 slot chassis with increased power and airflow delivery along with reservations for increased performance to the card. The 12-slot platform allows for higher port density load modules.	Rack
Optixia XM12	12	12 slots for load modules. Modular subcomponents for higher serviceability. Higher port density. Hot-swappable load modules. DVD-ROM drive. The XM12 High Performance verstion (OPTIXIAXM12-02) has two 2.0 kW power suplies.	Rack

Table 1-1. Ixia Chassis Comparison

Chassis	# of slots	Special Feature	Mounting
Optixia XM2	2	Two slots for load modules. Modular subcomponents for higher serviceability. Higher port density. Hot-swappable load modules. DVD-ROM drive.	Desktop/ Rack
Optixia X16	16	16 slots for load modules. Modular subcomponents for higher serviceability. Hot-swappable load modules. DVD-ROM drive.	Rack
Optixia XL10	10	10 slots for large high-density load modules. Redundant power supplies. Hot-swappable load modules. CD-ROM drive.	Free standing/ Rack
1600T	16	16 slots for load modules. Floppy drive.	Rack
400T	4	Four slots for load modules. Floppy drive.	Desktop/ Rack
250	2	Built-in 10/100/1000 TXS4 or 1000 SFPS4 port. Floppy drive.	Desktop/ Portable
100	1	Built-in GPS for worldwide synchronization	Rack

Note: Based on power requirements, Ixia chassis do not support all possible mixes of load modules. The Ixia chassis notifies you of conflicts on chassis power-up. Contact Ixia support for configuration verification.

Ixia Load Modules

Ixia offers a number of load modules that provide one to 24 ports of technology and media dependent interfaces to DUTs. The load modules are divided into logical families. Each family of load modules is discussed in details in its own chapter in this manual.

- *IXIA 40/100 Gigabit Ethernet Load Modules*: Provide 40 and 100 Gbps Ethernet with a variety of interfaces.
- *IXIA 10 Gigabit Ethernet Load Modules*: Provide 10 Gbps Ethernet with a variety of interfaces.
- *IXIA 1GbE and 10GbE Aggregation Load Modules*: Provide 10 Gbps and 1 Gbps Ethernet on the same module with a variety of interfaces.
- *IXIA 10GE LAN/WAN and OC 192 POS Load Modules*: Provide Optical Carrier interfaces that operate in concatenated mode at OC192 or 10 Gigabit Ethernet rates. One of the following modes can be used:
  - 10 Gigabit Ethernet LAN
  - 10 Gigabit Ethernet WAN

  - Packet over Sonet (POS)
  - Bit Error Rate Testing (BERT)
- *IXIA 10/100/1000 Load Modules*: Provide either 10 Mbps, 100 Mbps, or 1000 Mbps Ethernet speeds with auto-negotiation (except for Gigabit).
- *IXIA Gigabit Load Modules*: Provide 1000 Mbps Ethernet speeds.
- *IXIA OC12 ATM/POS Load Modules*: Provide Asynchronous Transfer Mode (ATM) functions.
- *IXIA 10/100 Load Modules*: Utilize a copper interface and provide either 10 Mbps or 100 Mbps Ethernet speeds with auto-negotiation with or without a per-port CPU.
- *IXIA 100 Load Modules*: Utilize a fiber interface and provide 100 Mbps Ethernet with auto-negotiation.
- *IXIA OC12c/OC3c Load Modules*: Provide selectable Optical Carrier interfaces that operate in concatenated mode at OC3 or OC12 rates. Packet over Sonet (POS) is implemented on the interfaces.
- *IXIA OC48c Load Modules*: Provide Optical Carrier interfaces that operate in concatenated mode at OC48 rates. Either Packet over Sonet (POS) or Bit Error Rate Testing (BERT) may be performed.
- *IXIA Power over Ethernet Load Modules*: Provide 10/100/1000 port emulation of network Powered Devices.
- *IXIA Stream Extraction Modules*: Provide 10/100/1000 stream capture and analysis of network devices.

Load modules with part numbers that contain -3 or -M are limited in their functionality. Newer boards also may have an ‘L’ before the last number in their part number, signifying the same limited functionality (that is, LSM10GL1-01). In general, -3 and -M modules do **not** have the following functions:

- Flows, except where Streams are not supported
- Advanced Streams (however, included with OC48C-3)
- Packet Groups (however, included with OC48C-3)
- Latency (however, included with OC48C-3)
- Sequence Checking (however, included with OC48C-3)
- Data Integrity (however, included with OC48C-M)
- Multiple DLCIs on OC48c load modules
- Convert to streams in capture view
- Protocol Server for router testing

‘L’ modules do **not** have the following functions:

- Advanced Routing functions
- Receive port filtering

Reduced vs. Full Feature

Some load modules are available in a Reduced Features version, which is identified by an 'R' before the last number in their part number. The following table illustrates the differences for one family of cards, NGY.

Table 1-2. Comparison of Full/Reduced Features, NGY Cards

	Standard	eXtra Performance 8-port	eXtra Performance 2/4-port	Reduced
PCPU	800 MHz	800MHz	1GHz	400MHz
PCPU Memory	512MB	1GB	1GB	128MB
Capture Memory	512MB	350MB	350MB	64MB
Table UDF Entries	1M	1M	1M	32K
UDF Range List	512K	512K	512K	256K
UDF Value List Entries	512K	512K	512K	256K
PGID	1M	1M	1M	64K

Load Module Names

The load module names used within the IxExplorer software differ slightly from the load module names used in Ixia marketing literature. *Table 1-3* on page 1-6 describes the mapping from load module names to the names in the Ixia price list and those used in IxExplorer. The reverse mapping, alphabetized, is shown in *Table 1-4* on page 1-11.

Note: Load modules without a price list column entry are no longer available for purchase.

Table 1-3. Load Module to IxExplorer Card Name Map

Family	Load Module	Price List Names	IxExplorer Card Name
10/100 Ethernet	LM100TX	LM100TX	10/100
	LM100TX3	n/a	10/100-3
	LM100TX8	LM100TX8	10/100 TX8
	LM100TXS8	LM100TXS8	10/100 TXS8
	LM100MII	n/a	10/100 MII
10/100/1000 Ethernet	ALM1000T8	ALM1000T8	10/100/1000 ALM T8
	ASM1000XMV12X-01	ASM1000XMV12X-01	10/100/1000 ASM XMV12X
	Xcellon-Ultra XP-01	Xcellon-Ultra XP	Xcellon-Ultra XP
	Xcellon-Ultra NP-01	Xcellon-Ultra NP	Xcellon-Ultra NP
	Xcellon-Ultra NG-01	Xcellon-Ultra NG	Xcellon-Ultra NG

Table 1-3. Load Module to IxExplorer Card Name Map

Family	Load Module	Price List Names	IxExplorer Card Name
	CPM1000T8	CPM1000T8	10/100/1000 CPM T8
	ELM1000ST2	ELM1000ST2	10/100/1000 ELM ST2
	LM1000T-5	LM1000T-5	Copper 10/100/1000
	LM1000TX4	LM1000TX4	10/100/1000 TX4
	LM1000TXS4	LM1000TXS4, LM1000TXS4-256	10/100/1000 TXS4 10/100/1000 TXS4-256
	LM1000STX2	LM1000STX2	10/100/1000 STX2
	LM1000STX4	LM1000STX4	10/100/1000 STX4
	LM1000STXS2	LM1000STXS2	10/100/1000 STXS2
	LM1000STXS4	LM1000STXS4, LM1000STXS4-256	10/100/1000 STXS4 10/100/1000 STXS4-256
	LM1000SFP4	LM1000SFP4	1000 SFP4
	LM1000SFPS4	LM1000SFPS4 LM1000SFPS4-256	1000 SFPS4 1000 SFPS4-256
	LSM1000XMS12-01 LSM1000XMSR12-01	LSM1000XMS12-01 LSM1000XMSR12-01	10/100/1000 XMS12 10/100/1000 XMSR12
	LSM1000XMV16-01 LSM1000XMVR16-01	LSM1000XMV16-01 LSM1000XMVR16-01	10/100/1000 LSM XMV16 10/100/1000 LSM XMVR16
	LSM1000XMV12-01 LSM1000XMVR12-01	LSM1000XMV12-01 LSM1000XMVR12-01	10/100/1000 LSM XMV12 10/100/1000 LSM XMVR12
	LSM1000XMV8-01 LSM1000XMVR8-01	LSM1000XMV8-01 LSM1000XMVR8-01	10/100/1000 LSM XMV8 10/100/1000 LSM XMVR8
	LSM1000XMV4-01 LSM1000XMVR4-01	LSM1000XMV4-01 LSM1000XMVR4-01	10/100/1000 LSM XMV4 10/100/1000 LSM XMVR4
	LSM1000XMSP12-01	LSM1000XMSP12-01	10/100/1000 LSM XMSP12
	LSM1000XMVDC4-01	LSM1000XMVDC4-01	10/100/1000 LSM XMVDC4
	LSM1000XMVDC4-NG	LSM1000XMVDC4-NG	10/100/1000 LSM XMVDC4NG
	LSM1000XMVDC8-01	LSM1000XMVDC8-01	10/100/1000 LSM XMVDC8
	LSM1000XMVDC12-01	LSM1000XMVDC12-01	10/100/1000 LSM XMVDC12
	LSM1000XMVDC16-01	LSM1000XMVDC16-01	10/100/1000 LSM XMVDC16
	LSM10/100/ 1000XMVDC16NG	LSM10/100/ 1000XMVDC16NG	LSM10/100/1000XMVDC16NG
	OLM1000STX24	OLM1000STX24	10/100/1000 STX24
	OLM1000STXS24	OLM1000STXS24	10/100/1000 STXS24
100MB Ethernet	LM100FX	n/a	100 Base FX MultiMode
	LM100FXSM	n/a	100 Base FX SingleMode

Table 1-3. Load Module to IxExplorer Card Name Map

Family	Load Module	Price List Names	IxExplorer Card Name
Gigabit	LM1000SX	n/a	Gigabit
	LM1000SX3	n/a	Gigabit-3
	LM1000GBIC	n/a	GBIC
	LM1000GBIC-P1	n/a	GBIC-P1
ATM	LM622MR, LM622MR-512	LM622MR w/ OPTATMMR, LM622MR-512 w/ OPTATMMR	ATM 622 Multi-Rate
		LM622MR w/ OPTPOSMR	ATM/POS 622 Multi-Rate
		LM622MR w/ OPTATMMR+ OPTPOSMR	ATM/POS 622 Multi-Rate
OC12c/OC3c	LMOC12c/LMOC3c	LMOC12c, LMOC12cSM	OC12c/OC3c POS
OC48	LMOC48cPOS		OC48c POS
	LMOC48cPOS-M		OC48c POS-M
	LMOC48cBERT		OC48c BERT
	LMOC48POS/BERT		OC48c POS/BERT
	LMOC48VAR		OC48c POS VAR
	MSM2.5G1-01	MSM2.5G1-01	2.5G MSM
OC192	LMOC192cPOS		OC192c POS
	LMOC192cVSR-POS		OC192c VSR POS
	LMOC192cBERT		OC192c BERT
	LMOC192cVSR-BERT		OC192c VSR BERT
	LMOC192cPOS+BERT		OC192c POS/BERT
	LMOC192cVSR-POS+BERT		OC192c VSR POS/BERT
	LMOC192cPOS+WAN		OC192c POS/10GE WAN
	LMOC192cPOS+BERT+WAN		OC192c POS/BERT/10GE WAN
10GE	LM10GELAN		10GE LAN
	LM10GELAN-M		10GE LAN-M
	LM10GEWAN		10GE WAN
	LSM10G1-01	LSM10G1-01	10GE LSM
	LSM10GL1-01	LSM10GL1-01	10GE LSM LAN XFP
	LSM10GMS-01	LSM10GMS-01	10GE LSM MACSec

Table 1-3. Load Module to IxExplorer Card Name Map

Family	Load Module	Price List Names	IxExplorer Card Name
	LSM10GXL6-01	LSM10GXL6-01	10GE LSM XL6
	LM10GEXAUI		10GE XAUI
	LM10GEXAUI+ BERT		10GE XAUI/BERT
	LM10GEXAUI BERT only		10GE XAUI BERT
	LM10GEXENPAK		10GE XENPAK
	LM10GEXENPAK-M		10GE XENPAK-M
	LM10GEXENPAK+BERT		10GE XENPAK/BERT
	LM10GEXENPAK-MA+BERT		10GE XENPAK-M/BERT
	LM10GEXENPAK BERT only		10GE XENPAK BERT
	LM10G	LM10GUEF, LM10GUEF-FEC, LM10GUEF-P, LM10GULF, LM10GUVF w/OPT10GELWAN	10G UNIPHY, 10G UNIPHY-P 10G UNIPHY-XFP 10G UNIPHY-FEC
	LSM10GXM3-01 LSM10GXMR3-01	LSM10GXM3-01 LSM10GXMR3-01	10GE LSM XM3 10GE LSM XMR3
	LSM10GXM8-01 LSM10GXMR8-01 LSM10GXM8XP-01 LSM10GXM8S-01 LSM10GXMR8S-01 LSM10GXM8GBT-01 LSM10GXMR8GBT-01 NGY-NP8-01	LSM10GXM8-01 LSM10GXMR8-01 LSM10GXM8XP-01 LSM10GXM8S-01 LSM10GXMR8S-01 LSM10GXM8GBT-01 LSM10GXMR8GBT-01 NGY-NP8-01	10GE LSM XM8 10GE LSM XMR8 10GE LSM XM8XP 10GE LSM XM8S 10GE LSM XMR8S 10GE LSM XM8 10GBASE-T 10GE LSM XMR8 10GBASE-T NGY-NP8 (10GE LSM XM8-NP)
	LSM10GXM4-01 LSM10GXMR4-01 LSM10GXM4XP-01 LSM10GXM4S-01 LSM10GXMR4S-01 LSM10GXM4GBT-01 LSM10GXMR4GBT-01 NGY-NP4-01	LSM10GXM4-01 LSM10GXMR4-01 LSM10GXM4XP-01 LSM10GXM4S-01 LSM10GXMR4S-01 LSM10GXM4GBT-01 LSM10GXMR4GBT-01 NGY-NP4-01	10GE LSM XM4 10GE LSM XMR4 10GE LSM XM4XP 10GE LSM XM4S 10GE LSM XMR4S 10GE LSM XM4 10GBASE-T 10GE LSM XMR4 10GBASE-T NGY-NP4 (10GE LSM XM4-NP)
	LSM10GXM2XP-01 LSM10GXMR2-01 LSM10GXM2S-01 LSM10GXMR2S-01 LSM10GXM2GBT-01 LSM10GXMR2GBT-01 NGY-NP2-01	LSM10GXM2XP-01 LSM10GXMR2-01 LSM10GXM2S-01 LSM10GXMR2S-01 LSM10GXM2GBT-01 LSM10GXMR2GBT-01 NGY-NP2-01	10GE LSM XM2XP 10GE LSM XMR2 10GE LSM XM2S 10GE LSM XMR2S 10GE LSM XM2 10GBASE-T 10GE LSM XMR2 10GBASE-T NGY-NP2 (10GE LSM XM2-NP)
	MSM10G1-02	MSM10G1-02	10G MSM
	ASM1000XMV12X-01	ASM1000XMV12X-01	10/100/1000 ASM XMV12X
	Xcellon-Ultra XP-01	Xcellon-Ultra XP	Xcellon-Ultra XP

Table 1-3. Load Module to IxExplorer Card Name Map

Family	Load Module	Price List Names	IxExplorer Card Name
	Xcellon-Ultra NP-01	Xcellon-Ultra NP	Xcellon-Ultra NP
	Xcellon-Ultra NG-01	Xcellon-Ultra NG	Xcellon-Ultra NG
40GE	HSE40GETSP1-01	HSE40GETSP1-01	40GE LSM XMV
100GE	HSE100GETSP1-01	HSE100GETSP1-01	100GE LSM XMV
40/100GE	HSE40GETSP1-01	HSE40GETSP1-01	40GE LSM XMV
	HSE100GETSP1-01	HSE100GETSP1-01	100GE LSM XMV
	HSE40/100GETSP1-01	HSE40/100GETSP1-01	40/100GE LSM XMV
	HSE40GEQSFP1-01	HSE40GEQSFP1-01	40GE LSM XMV QSFP
Power over Ethernet	PLM1000T4-PD	PLM1000T4-PD	Power over Ethernet PLM 20W
	LSM1000POE4-02	LSM1000POE4-02	Power over Ethernet PLM 30W
Stream Extraction Module	AFM1000SP-01	AFM1000SP-01	AFM - Stream Extraction Module
Voice Quality	VQM01XM	VQM01XM	Voice Quality Resource Module
Excellon-Flex	FlexAP10G16S		FlexAP10G16S
	FlexFE10G16S		FlexFE10G16S
10GE Ethernet	Xdensity		XDM10G32S
ImpairNet	EIM10G4S		EIM10G4S
	EIM1G4S		EIM1G4S
Xcellon-Lava	Lava AP40/100GE 2P		Lava AP40/100GE 2P
	Lava AP40/100GE 2P		Lava AP40/100GE 2P

Table 1-4. IxExplorer Card Name to Load Module Name Map (Alphabetical)

IxExplorer Card Name	Load Module	Price List Names
10/100	LM100TX	LM100TX
10/100-3	LM100TX3	LM100TX3
10/100 MII	LM100MII	
10/100 TX8	LM100TX8	LM100TX8
10/100 TXS8	LM100TXS8	LM100TXS8
10/100/1000 ALM T8	ALM1000T8	ALM1000T8
10/100/1000 ASM XMV12X	ASM1000XMV12X-01	ASM1000XMV12X-01
10/100/1000 CPM T8	CPM1000T8	CPM1000T8
10/100/1000 ELM ST2	ELM1000ST2	ELM1000ST2
10/100/1000 LSM XMSP12	LSM1000XMSP12-01	LSM1000XMSP12-01
10/100/1000 LSM XMVDC4	LSM1000XMVDC4-01	LSM1000XMVDC4-01
10/100/1000 LSM XMVDC4NG	LSM1000XMVDC4-NG	LSM1000XMVDC4-NG
10/100/1000 LSM XMVDC8	LSM1000XMVDC8-01	LSM1000XMVDC8-01
10/100/1000 LSM XMVDC12	LSM1000XMVDC12-01	LSM1000XMVDC12-01
10/100/1000 LSM XMVDC16	LSM1000XMVDC16-01	LSM1000XMVDC16-01
10/100/1000 LSM XMVDC16NG	10/100/1000 LSM XMVDC16NG	10/100/1000 LSM XMVDC16NG
10/100/1000 LSM XMV16 10/100/1000 LSM XMVR16	LSM1000XMV16-01 LSM1000XMVR16-01	LSM1000XMV16-01 LSM1000XMVR16-01
10/100/1000 LSM XMV12 10/100/1000 LSM XMVR12	LSM1000XMV12-01 LSM1000XMVR12-01	LSM1000XMV12-01 LSM1000XMVR12-01
10/100/1000 LSM XMV8 10/100/1000 LSM XMVR8	LSM1000XMV8-01 LSM1000XMVR8-01	LSM1000XMV8-01 LSM1000XMVR8-01
10/100/1000 LSM XMV4 10/100/1000 LSM XMVR4	LSM1000XMV4-01 LSM1000XMVR4-01	LSM1000XMV4-01 LSM1000XMVR4-01
10/100/1000 STX2	LM1000STX2	LM1000STX2
10/100/1000 STX24	OLM1000STX24	OLM1000STX24
10/100/1000 STX4	LM1000STX4	LM1000STX4
10/100/1000 STXS2	LM1000STXS2	LM1000STXS2
10/100/1000 STXS24	OLM1000STXS24	OLM1000STXS24
10/100/1000 STXS4 10/100/1000 STXS4-256	LM1000STXS4	LM1000STXS4, LM1000STXS4-256
10/100/1000 TX4	LM1000TX4	LM1000TX4
10/100/1000 TXS4 10/100/1000 TXS4-256	LM1000TXS4	LM1000TXS4, LM1000TXS4-256

Table 1-4. IxExplorer Card Name to Load Module Name Map (Alphabetical)

IxExplorer Card Name	Load Module	Price List Names
10/100/1000 XMS12 10/100/1000 XMSR12	LSM1000XMS12-01 LSM1000XMSR12-01	LSM1000XMS12-01 LSM1000XMSR12-01
100 Base FX MultiMode	LM100FX	
100 Base FX SingleMode	LM100FXSM	
1000 SFP4	LM1000SFP4	LM1000SFP4
1000 SFPS4 1000 SFPS4-256	LM1000SFPS4	LM1000SFPS4, LM1000SFPS4-256
2.5G MSM	MSM2.5G1-01	MSM2.5G1-01
10G MSM	MSM10G1-02	MSM10G1-02
10G UNIPHY, 10G UNIPHY-P 10G UNIPHY-XFP 10G UNIPHY-FEC	LM10G	LM10GUEF, LM10GUEF-FEC, LM10GUEF-P, LM10GULF, LM10GUVF w/ OPT10GELWAN
10GE LAN	LM10GELAN	
10GE LAN-M	LM10GELAN-M	
10GE LSM	LSM10G1-01	LSM10G1-01
10GE LSM LAN XFP	LSM10GL1-01	LSM10GL1-01
10GE LSM MACSec	LSM10GMS-01	LSM10GMS-01
10GE LSM XL6	LSM10GXL6-01	LSM10GXL6-01
10GE LSM XM3 10GE LSM XMR3	LSM10GXM3-01 LSM10GXMR3-01	LSM10GXM3-01 LSM10GXMR3-01
10GE LSM XM8 10GE LSM XMR8 10GE LSM XM8XP 10GE LSM XM8S 10GE LSM XMR8S 10GE LSM XM8 10GBASE-T 10GE LSM XMR8 10GBASE-T NGY-NP8	LSM10GXM8-01 LSM10GXMR8-01 LSM10GXM8XP-01 LSM10GXM8S-01 LSM10GXMR8S-01 LSM10GXM8GBT-01 LSM10GXMR8GBT-01 NGY-NP8-01	LSM10GXM8-01 LSM10GXMR8-01 LSM10GXM8XP-01 LSM10GXM8S-01 LSM10GXMR8S-01 LSM10GXM8GBT-01 LSM10GXMR8GBT-01 NGY-NP8-01
10GE LSM XM4 10GE LSM XMR4 10GE LSM XM4XP 10GE LSM XM4S 10GE LSM XMR4S 10GE LSM XM4 10GBASE-T 10GE LSM XMR4 10GBASE-T NGY-NP4	LSM10GXM4-01 LSM10GXMR4-01 LSM10GXM4XP-01 LSM10GXM4S-01 LSM10GXMR4S-01 LSM10GXM4GBT-01 LSM10GXMR4GBT-01 NGY-NP4-01	LSM10GXM4-01 LSM10GXMR4-01 LSM10GXM4XP-01 LSM10GXM4S-01 LSM10GXMR4S-01 LSM10GXM4GBT-01 LSM10GXMR4GBT-01 NGY-NP4-01

Table 1-4. IxExplorer Card Name to Load Module Name Map (Alphabetical)

IxExplorer Card Name	Load Module	Price List Names
10GE LSM XM2XP 10GE LSM XMR2 10GE LSM XM2S 10GE LSM XMR2S	LSM10GXM2XP-01 LSM10GXMR2-01 LSM10GXM2S-01 LSM10GXMR2S-01	LSM10GXM2XP-01 LSM10GXMR2-01 LSM10GXM2S-01 LSM10GXMR2S-01
10GE LSM XM2 10GBASE-T 10GE LSM XMR2 10GBASE-T NGY-NP2	LSM10GXM2GBT-01 LSM10GXMR2GBT-01 NGY-NP2-01	LSM10GXM2GBT-01 LSM10GXMR2GBT-01 NGY-NP2-01
10GE WAN	LM10GEWAN	LM10GE123F, LM10GE124F
10GE XAUI	LM10GEXAUI	
10GE XAUI BERT	LM10GEXAUI BERT only	
10GE XAUI/BERT	LM10GEXAUI+ BERT	
10GE XENPAK	LM10GEXENPAK	
10GE XENPAK BERT	LM10GEXENPAK BERT only	
10GE XENPAK/BERT	LM10GEXENPAK+BERT	
10GE XENPAK-M	LM10GEXENPAK-M	
10GE XENPAK-M/BERT	LM10GEXENPAK- MA+BERT	
40GE LSM XMV	HSE40GETSP1-01	HSE40GETSP1-01
100GE LSM XMV	HSE100GETSP1-01	HSE100GETSP1-01
40/100GE LSM XMV	HSE40/100GETSP1-01	HSE40/100GETSP1-01
40GE LSM XMV QSFP	HSE40GEQSFP1-01	HSE40GEQSFP1-01
Xcellon-Ultra NP	Xcellon-Ultra NP-01	Xcellon-Ultra NP
Xcellon-Ultra XP	Xcellon-Ultra XP-01	Xcellon-Ultra XP
Xcellon-Ultra NG	Xcellon-Ultra NG-01	Xcellon-Ultra NG
AFM1000SP-01	AFM Stream Extraction Module	AFM1000SP-01
ATM 622 Multi-Rate	LM622MR	LM622MR w/OPTATMMR
ATM/POS 622 Multi-Rate		LM622MR w/OPTPOSMR
ATM/POS 622 Multi-Rate		LM622MR w/ OPTATMMR+ OPTPOSMR, LM622MR-512 w/ OPTATMMR+ OPTPOSMR
Copper 10/100/1000	LM1000T-5	LM1000T-5
GBIC	LM1000GBIC	
GBIC-P1	LM1000GBIC-P1	

Table 1-4. IxExplorer Card Name to Load Module Name Map (Alphabetical)

IxExplorer Card Name	Load Module	Price List Names
Gigabit	LM1000SX	
Gigabit-3	LM1000SX3	
OC12c/OC3c POS	LMOC12c/LMOC3c	LMOC12c, LMOC12cSM
OC192c BERT	LMOC192cBERT	
OC192c POS	LMOC192cPOS	
OC192c POS/10GE WAN	LMOC192cPOS+WAN	
OC192c POS/BERT	LMOC192cPOS+BERT	
OC192c POS/BERT/10GE WAN	LMOC192cPOS+BERT+WAN	
OC192c VSR BERT	LMOC192cVSR-BERT	
OC192c VSR POS	LMOC192cVSR-POS	
OC192c VSR POS/BERT	LMOC192cVSR-POS+BERT	
OC48c BERT	LMOC48cBERT	
OC48c POS	LMOC48cPOS	
OC48c POS VAR	LMOC48VAR	
OC48c POS/BERT	LMOC48POS/BERT	
OC48c POS-M	LMOC48cPOS-M	
Power over Ethernet	LM1000T4-PD	LM1000T4-PD
Voice Quality Resource Module	VQM01XM	VQM01XM
Lava AP40/100GE 2P	Lava AP40/100GE 2P	
Lava AP40/100GE 2P	Lava AP40/100GE 2P	

Ixia Load Module Properties

The Ixia load modules, or load modules, support a wide range of features, which are described in Table 1-5.

The full set of supported features per card is described in the spreadsheet *Port Features by Port Type* on the *Ixiacom.com* website, under *Support/User Guides/ Spreadsheets*.

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
Basic	Local CPU	Each port on the card is supported by an individual CPU for use in protocol server and other sophisticated operations.
	Layer 2/3 Only	The card only supports Layer 2 and 3 control and operation. No protocols except ARP and PING are supported.
	Layer 7 Only	The card only supports Layer 7 usage through the local CPU. This type of card is generally only useful for application testing as in IxLoad and Chariot.
Statistics Selection	Checksum errors (IPv4/TCP/UDP)	Support generation and checking of special checksums for IPv4, TCP, and UDP packets.
	Data integrity	Supports data integrity generation and checking.
	Tx Duration	Supports the generation of a transmit duration statistic.
	Per stream stats	Statistics are available for each stream.
Receive Modes	Capture	Received data may be captured to a capture buffer.
	Packet groups	Supports generation of packet group IDs in packets.
	Latency S&Fwd LB to FB	Latency measurement offers the option of measuring the time from last data bit out to first data bit in
	Latency S&Fwd LB to FP	Latency measurement offers the option of measuring the time from last data bit out to first preamble bit in

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	Inter-arrival Jitter	Inter-Arrival Time (IAT) compares the time between PGID packet arrivals. In this case, when a packet with a PGID is received, the PGID is examined. If a packet has already been received with the same PGID, then the timestamp of the previous packet is subtracted from the current timestamp. The interval between the timestamps is the jitter, and it is recorded for statistical purposes.
	Delay Variation	Offers the option of measuring variation between latency of consecutive frames.
	MEF Frame Delay	Measurement method: First data bit in to DUT; last data bit out of DUT.
	Forwarding Delay	Measurement method: Last data bit in to DUT; last data bit out of DUT.
	Advanced PG Filter	A set of features which allow packet group matching to ignore or mask: • Group ID • Signature • Filter data
	Round-trip flows	Supports calculation of round-trip flows.
	Data integrity	Supports data integrity generation and checking.
	First time stamp	Supports first time stamp operation.
	Tx/Rx Time Stamp Mode	Allows the system to use the time stamp of the last bit of the packet; this is useful when multiple rates are present in the network topology.
	Sequence checking	Supports packet sequence generation and verification.
	Sequence checking per packet ID	When packet groups are used, allows sequence checking generation and verification.
	ISL encapsulation	Receive side of port can accommodate ISL encapsulation on receive side.
	Small packets	Supports the ability to capture packets smaller than a legal packet; captured data may be corrupted when this feature is used.
	Wide packet groups	This feature allows ports, which utilize packet groups, to extend the number of bits in the PGID to 17 bits (or more).

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	PRBS Mode	When the Receive Mode is set to PRBS mode, both Wide Packet Groups and Sequence Checking are automatically enabled. In PRBS mode, all latency-related statistics are removed and the following per PGID statistics are added: • PRBS Bits Received • PRBS Errored Bits • PRBS BER
	Split PGIDs	Allows for the creation of split PGID data.
	Latency bins	Latency data may be categorized by latency values for each packet group.
	Time bins	Latency may be measured over time.
	Echo	Ports with this feature may echo all received traffic as transmitted packets.
	Preamble capture	Frame's preamble may be included in the capture buffer.
	Simulate cable disconnect	A cable disconnect state may be simulated.
	Flexible Pattern Offset	Allows to set the Filter/Trigger pattern to a specific offset.
	Multi Switched-Path	Allows for the detection of loss/duplicate packets.
	Intrinsic Latency Adjustment	Reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). Retrieves pre-determined latency value for a 'known' transceiver, or calculates and stores that value for a 'new' transceiver.
	Misdirected Mask	Sets the signature mask used for identifying misdirected packets.
	Rate Monitoring (convergence)	Enables testing convergence times and service interruptions.
	Auto-Detect Instrumentation	On the receive side, automatically detects a specified signature and Instrumentation parameters for Data Integrity, Sequence Checking, or Latency for streams generated with Automatic Instrumentation Offsets using Ixia software applications.
	TSO/LRO	Transmit Segmentation Offload/Large Receive Offload (TSO/LRO) operation mode.

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
Transmit Modes	Packet streams	Supports the generation of packet streams.
	Packet flows	Supports the generation of packet flows.
	Advanced scheduler	Supports the operation of the advanced scheduler, which allows inter-mixing of multiple packet streams.
	Forced collisions	Supports the insertion of forced collisions.
	Tx Data integrity	Supports data integrity generation and checking.
	Odd preamble	Supports the ability to send a preamble with an odd number of bytes. This is not applicable to boards with dual PHYs (Ethernet/Fiber) when a port is in fiber mode.
	Gap time units	The inter-frame, -burst, and -stream gaps can be programmed in discreet units of time as opposed to indirectly through a percentage of maximums frame rate.
	Gap byte count	Gaps may be expressed as a number of bytes.
	Modifiable preamble	The packet's preamble content may be modified. On 10GE load modules that support this feature there are two options: modify the 7 rightmost bytes of the 8 byte preamble or modify the inner 6 bytes of the 8 byte preamble.
	Forced minimum IPG	In advanced scheduler mode, a minimum gap may be enforced.
	Increment frame size by N	Frame sizes may be incremented by an arbitrary value between transmitted frames.
	Increment/ Decrement DA/SA by N	DA and SA values may be incremented or decremented by an arbitrary value between transmitted frames.
	Random data on even offset only	When random data is generated within a frame's content, the random data may only be placed at even byte boundaries.
	Insert bad TCP checksum	Supports the generation of bad TCP checksums.
	Checksum Override	Overrides IPv4, IPv6 and TCP checksums.

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	Frequency offset	The frequency for the card as a whole may be modified a few percent from nominal.
	Echo	The port echoes all received packets.
	Flexible Time Stamp	The position of the time stamp in transmitted packets may be repositioned.
	Protocol Offset	The beginning of the IP (or other) protocol header may be repositioned so as to accommodate leading headers, as in PPP.
	Random IPG	The IPG between packets may be set to a random value.
	Copper RJ45/Fiber SFP	The port has the ability to transmit and receive from either its copper RJ-45 Ethernet or Fiber SFP optic interface.
	Weighted Random Frame Size	The port has the ability to generate packets with random frame sizes. The frame sizes are programmed through a set of frame sizes and weightings.
	Scheduled duration	The duration of the transmit operation may be scheduled for a number of seconds.
	Simulate cable disconnect	A cable disconnect state may be simulated.
	Repeatable Random Streams	Allows for repeating randomly generated stream data.
	GRE	An IP transport protocol available for insertion into transmitted streams.
	Stacked VLANs	Allows for sending multiple VLAN IDs in a single packet.
	Tx Ignore Link	Allows for transmission of packets with the link down.
	Protocol Pad	Allows for a data pad to be added before the protocol head field in a frame.
	Dynamic Rate Change	Allow rate change without stopping transmit.
	Dynamic Frame Size Change	Allow frame size change without stopping transmit.
	New Incrementing Frame Size	Allow packets/burst setting in incrementing frame size mode

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	Auto-Detect Instrumentation	On the transmit side, automatically configures a specified signature and Instrumentation parameters for Data Integrity, Sequence Checking, Latency, or PRBS for streams generated for Ixia software applications that use Automatic Instrumentation Offsets.
	Intrinsic Latency Adjustment	Reduce the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). Retrieves pre-determined latency value for a 'known' transceiver, or calculates and stores that value for a 'new' transceiver.
	PRBS	When the port is in PRBS mode, all latency-related statistics are removed and the following per-PGID statistics are added: • PRBS Bits Received • PRBS Errored Bits • PRBS BER
	TSO/LRO	Transmit Segmentation Offload/Large Receive Offload (TSO/LRO) operation mode.
User Defined Fields (UDF)	Odd offset	UDFs are allowed to start at an odd offset.
	Overlap	UDFs may overlap within a 4-octet boundary. Otherwise UDFs must start at least 4 octets apart.
	Cascade	UDFs may continue from previous stream values.
	Cascade from self	UDFs may continue from previous values on the same UDF.
	Split	UDFs may be split into multiple 8-bit and 16-bit counters.
	Bit mask	UDFs output data may be masked with an arbitrary bit mask. Otherwise limitations on the number of changes of bits applies.
	Incr By N	Allows UDFs to increment by an arbitrary value.
	UDF5	The port has a fifth UDF.

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	Advanced	The port supports additional UDF features, including: Nested counters Linked lists Step size Value list Range list
	IPv4	The port supports UDF - IPv4 type counting.
	Range List	The port supports UDF generated values over a list of value ranges.
	Value List	The port supports UDF generated values from a list of values.
	Nested Counter	The port supports UDF generated values from two nested counters.
	Table	The port supports a UDF that derives values from a table of offsets and values, by packet.
	Chained UDFs	The port supports the ability to chain from a specified UDF.
	Protocol Pad	Allows for a data pad to be added before the protocol head field in a frame.
POS/ BERT	POS	Supports Packet over SONET operation.
	BERT	Supports Bit Error Rate Testing through the generation and verifications of patterns.
	Channelized BERT	Support channelized BERT testing.
	BERT error insertion	Supports BERT error insertion.
	DCC	Supports additional DCC channel streams.
	SRP	Supports Serial Reuse Protocol—passive receive.
	SRP Full	Supports Serial Reuse Protocol—active send/receive.
	RPR	Supports Resilient Packet Ring operation.
	FEC	Support Forwarding Error Correction.
	GFP	Supports the Generic Framing Protocol.
	SONET error insertion list	Support the insertion of Sonet errors.

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	Multiple DLCIs	Supports the use of more than one DLCI in frame relay testing.
	CJPAT/CRPAT	Supports generated CJPAT and CRPAT frame data patterns.
10 Gigabit Ethernet	OC192	Supports OC192 POS operation.
	WAN	Supports 10 GE WAN operation.
	LAN	Supports 10 GE LAN operation.
	XAUI	Supports 10GE XAUI interface.
	XENPAK	Supports 10GE XENPAK interface.
	LASI	Supports Link Alarm Status Interrupt.
	XFP	Supports an XFP interface.
	SFP	Supports an SFP (small form-factor pluggable) transceiver interface.
	UNIPHY	Supports UNIPHY operation, which allows the same port to operate in LAN, WAN, POS and BERT modes.
	Lane skew	Supports the ability to skew multiple PCS (Physical Coding Sublayer) lanes.
	Set pause destination address	The destination for pause control packets may be set.
	Link Fault Signalling	Supports the link fault signalling protocol.
	Gap Control Mode	Allows for the selection of the gap control algorithm, as defined by IEEE.
	Pre-Emphasis	Allows for boosting transmit signal.
	MACSec	Supports MACSec functionality. Media Access Control Security (MACsec) is a L2 protocol which authenticates the entire L2 frame (except for the Ethernet CRC) and provides confidentiality for all or some of the MACsec data segment. This protocol is defined in IEEE 802.1AE
Protocol Server	Basic Routing	Supports basic routing protocols, including BGP, IS-IS and OSPF, but none of those in the list for *Advanced Routing*.
	DHCP	Supports the DHCP protocol.

Table 1-5. Ixia Load Module Feature Descriptions

Feature Category	Feature	Usage
	DHCPv6	Supports the DHCPv6 protocol.
	Advanced Routing (note 1)	Supports advanced routing protocols: • BGP-IPv6 • IGMP (new) with IPMPv3 • ISIS-IPv6 • OSPFv3 • PIM-SM • Layer 2 VPN (LDP) • Layer 3 VPN (BGP) • LDP • MLD • RIPng
	ARP	Supports ARP generation and receipt handling.
	Gratuitous ARP	Gratuitous ARP is sent by the host when its IP to MAC mapping changes, so that everybody else on the subnet updates their ARP tables.
	ARP rate control	The rate at which multiple ARP packets are transmitted may be controlled.
	IGMP rate control	The rate at which multiple IGMP packets are transmitted may be controlled.
	PING	Supports PING generation and receipt.
	FCoE/NPIV	Supports Fibre Channel over Ethernet and N_Port_ID Virtualization.
	PTP	Supports Precision Time Protocol.
	RTP	Supports Real-time Transport Protocol

Notes:

1. On older OC48c, OC192c and 10GE modules, these protocols require that the ports have been upgraded to 128MB of CPU memory.

Card Properties

Details about the card characteristics described in *Table 1-6* are presented in the chapters about specific load modules.

Table 1-6. Card Specifications

Specification	Usage
# ports	The number of ports supported by the card(s).
-3/-M/L Card Available	Whether a limited feature card is available.
L2/L3 Card Available	Whether a Layer 2/3 only card is available.
Layer 7 Card Available	Whether a Layer 7 only card is available.
Data Rate	The choice of data rates offered by the card.
Connector/Frequency-Mode	The connector type used on the card. For optical connections, the light frequency used and whether the fiber is used for singlemode or multimode.
Capture buffer size	The size of each port's capture buffer.
Captured packet size	The range of packet sizes that may be captured on the card.
Streams per port	The number of streams available on each port.
Flows per port	The number of stream flows available on each port. If available, this is always 15,872.
Advanced streams	The number of advanced streams available on each port.
Preamble size: min-max	The range of sizes, in bytes, for generated preambles.
Frame size: min-max	The range of sizes, in bytes, for generated frames.
Inter-frame gap: min-max	The gap between frames, expressed as a range of time.
Inter-burst gap: min-max	The gap between bursts of frames, expressed as a range of time.
Inter-stream gap: min-max	The gap between streams, expressed as a range of time. Sometimes expressed as a percentage of the maximum rate.

Table 1-6. Card Specifications

Specification	Usage
Latency	The accuracy of latency operations.
Intrinsic Latency Adjustment	Reduce the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). Retrieves pre-determined latency value for a 'known' transceiver, or calculates and stores that value for a 'new' transceiver.

Number of captured packets, an important characteristic, cannot be expressed as a simple number. It is dependent on a number of factors as mentioned in the following list:

- Size of the capture buffer
- Size of the captured packet
- Size of the capture slice, set by you
- Memory used by other functions
- Memory overhead per captured packet

The general equation is:

```
# of captured packets = (size of capture buffer) -
(memory used by other functions)

(min (captured packet, capture slice) + (per packet
overhead)
```

To get an idea of the memory available for packet capture, a set of simple experiments can be run. For example, Table 1-7 indicates the measured number of packets captured for different packet sizes. The type of card used is an LM100TX, which has a 2MB capture buffer. The buffer slice is set to 8191.

Table 1-7. Measured Number of Packets for an LM100TX Card

Packet Size	Number of Packets Captured	Memory Used by Captured Packets
64 bytes	18,668	1,194,752
1K bytes	1,698	1,738,752
4K bytes	436	1,785,856
8K bytes	219	1,794,048

The experiment indicates that there is approximately 1.8 MB available for data capture.

Maximum number of PGIDs

The maximum number of PGIDs for designated load module families is provided in Table 1-8.

Table 1-8.Maximum PGID Summary

Load Module Family	Receive Mode	Maximum Number PGIDs[1](Decimal)
LM100TX		
	Packet Group	57344
	First Timestamp	
LM1000GBIC		
	Packet Group	57344
	Sequence Checking	N/A
	First Timestamp	
LM100TXS8		
	Packet Group	65536
	Packet Group + Sequence Checking	128
	Capture + Sequence Checking	128
	Wide Packet Group	131072
LM1000STXS4 and **LSM1000XMS12-01**, **LSM1000XMSP12-01**		
	Packet Group	65536
	Packet Group + Sequence Checking	128
	Capture + Sequence Checking	128
	Wide Packet Group	131072
	Wide Packet Group (Reduced Feature)	65536
LSM1000XMV family (4, 8, 12, and 16-port)		
	Wide Packet Group	131072
	Wide Packet Group (Reduced Feature)	65536
	Wide Packet Group/Wide Bin Mode (Full Feature)	1048576
ASM1000XMV	Wide Packet Group/Wide Bin Mode	1048576
LSM10G including **MSM10G** and **MSM2.5G**		
	Wide Packet Group	2097152
	Wide Packet Group (Reduced Feature)	65536
100GE LSM XMV, **40GE LSM XMV, and 40/100GE LSM XMV**	Wide Packet Group	1048576

Table 1-8.Maximum PGID Summary

Load Module Family	Receive Mode	Maximum Number PGIDs[1](Decimal)
LM10G and **LM10GE**		
	Packet Group	65536
	Sequence Checking	8192
	Packet Group + Sequence Checking	8192
	Wide Packet Group	131072
LMOC-12		
	Packet Group	57344
	Sequence Checking	N/A
LMOC-48		
	Packet Group	65536
	Packet Group + Sequence Checking	512
	Capture + Sequence Checking	512
LMOC-192		
	Packet Group	1024
	Sequence Checking	1024
	Packet Group + Sequence Checking	1024
	Wide Packet Group	131072
LM622MR		
	Packet Group	65536
	Packet Group + Sequence Checking	128
	Capture + Sequence Checking	128
	Wide Packet Group	131072
LavaAP40/100GE		
	Sequence Checking	1048576
	Data Integrity	
	Wide Packet Groups	1048576
	Latency/Jitter	

1. The maximum number of PGIDs is the maximum hardware PGID that can be supported by a particular load module in a particular mode. If time bin, latency, or other parameters are enabled, the maximum PGID that can be supported is reduced.

   All modules have a maximum 2048 time bins. All modules that support latency bins have quantity 16 latency bins.

New in Version 6.20

New Products

The following products are new for this release:

- The Xcellon-Lava 40/100-Gigabit Ethernet load modules belong to the family of Ixia's High Speed Ethernet (HSE) products. These load modules combine the advantages of the Xcellon architecture and provide the highest 40GE and 100GE port densities. Lava load modules can be used for testing layer 2 to layer 7 applications. They are supported by Ixia's test applications, including IxNetwork and IxLoad. For more information, see Chapter 32, *IXIA Xcellon-Lava Load Modules*.
- IxVM is a software-based test platform that enables you to turn standard Linux Ethernet ports into virtual Ixia ports. IxVM can create virtual Ixia ports from the virtual Ethernet ports on a Linux virtual machine (VM), or from the physical Ethernet ports on a physical Linux server. For more information, see Chapter 35, *IxVM*.

2 Theory of Operation: General

This chapter discusses the unifying concepts behind the Ixia system. Both the software and hardware structures, and their usage, are discussed. The chapter is divided into the following major sections:

Ixia Hardware

This section discusses the range and capabilities of the Ixia hardware, including general discussions of several technologies used by Ixia hardware. This section is divided into the following general areas:

Chassis Chain (Hardware)

At the highest level, the Ixia hardware is structured as a chain of different types of chassis, up to 256 units. The chassis list is mentioned in the following table:

Table 2-1. Currently Available Ixia Chassis

Chassis	Number of Load Modules Supported
XG12	12 high density modules
Optixia XM12	12 high density modules
Optixia XM2	Two high density modules
Optixia XL10	10 large modules
Optixia X16	16 standard load modules
Ixia 100	One standard load modules
Ixia 250	Two standard load modules, plus a single built-in 10/100/1000 Ethernet port.
Ixia 400T	Four standard load modules
Ixia 1600T	16 standard load modules

All non-Optixia chassis support load modules that each may contain one to 8 ports. Up to 16 ports per load module are supported on Optixia XM2 and XM12 chassis, and up to 24 ports are supported on Optixia XL10 load modules, which can result in a very large number of ports for the overall system.

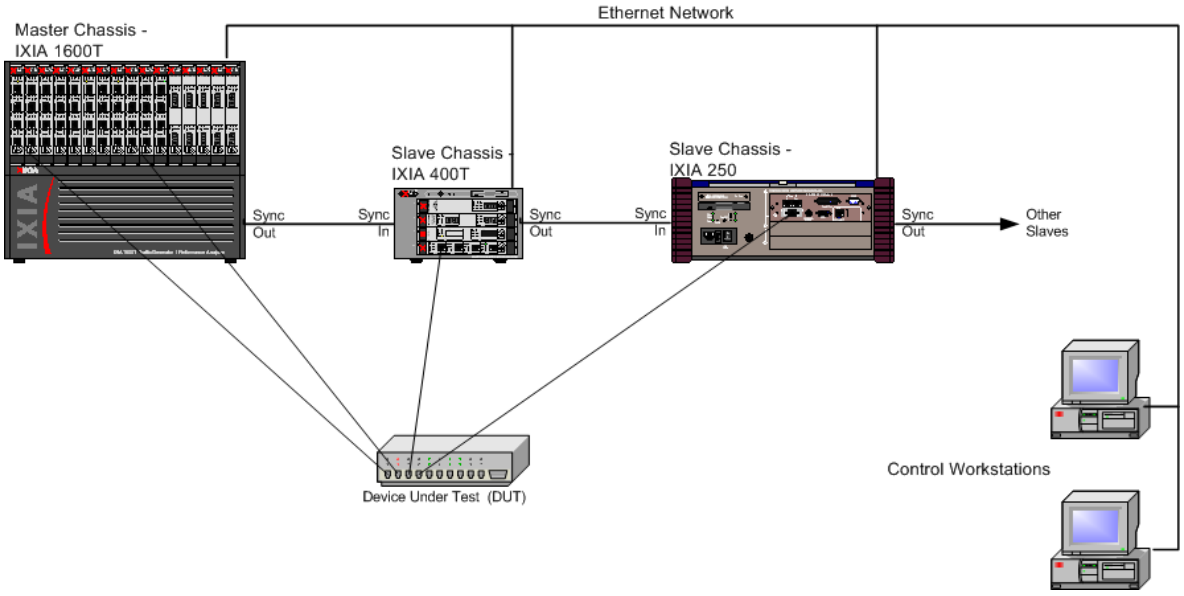
Multiple Ixia chassis are chained together through special Sync-out/Sync-in cables that allow for port-to-port synchronization across locally connected chassis in accordance with the specification mentioned in the *Chassis Chain Timing Specification* section.

Note: There are several rules that must be observed when constructing chassis chains. If a rule is violated, chassis timing may not meet the specification.

- Sync cable length between two chassis in a chain should be less than or equal to 6 feet.
- In a physical chassis chain, the Optixia chassis must be grouped together, and the non-Optixia chassis must be grouped together; that is, the two types can be on the same chassis chain, but cannot be intermingled. In a virtual chain that consists of several physical chains, each physical chain must obey this rule.
- Sequence numbers must be unique in a chain. Within a chain, there cannot be duplicate sequence numbers.The master chassis must have the smallest sequence value in the physical chain. The order of sequence numbers must match the order of chassis (up to 99999). The numbers do not have to be sequentially contiguous (1, 2, 3, and so on.) but they must be sequentially increasing in value (1, 5, 8, and so on.)
- Certain load modules must be used in only the first 3 chassis in a chain. These include LM100TXS8, LM100TXS2, LM100TX8, LM100TX2, LM100TX, LM100TX1, LM100TX2, and LM100TX3. If these boards are used in the fourth or later chassis in a chain, the network ports may not operate reliably.

The following figure is a representation of an independent Ixia chassis chain and control network. Chassis are chained together through their sync cables. The first chassis in a chain has a Sync-out connection (but no Sync-in unless it is the AFD1 GPS receiver), and is called the *master* chassis. All other chassis in the chain are termed *subordinates*.

Figure 2-1. Ixia Chassis Chain and Control Workstation



Multiple, geographically-separated, independent chassis may be synchronized with a high degree of accuracy by using an Ixia chassis. Specific chassis include an integral GPS or CDMA receiver which is used for worldwide chassis

synchronization. See *Chassis Synchronization* on page 2-5 for a complete discussion of chassis timing.

Note: Plugging-in or removing the sync cable while IxServer is starting or running can cause the IxServer to detect the change in the sync-in connection and shut down. If this occurs, restart IxServer, then restart all Ixia applications.

Ports from the chassis are connected to the Device Under Test (DUT) using cables appropriate for the media. Ports from any chassis may be connected to the similar ports on the DUT. It is even possible to connect multiple independent DUTs to different ports on different chassis.

Each chassis is driven by an Intel Pentium-based computer running Windows XP Professional and Ixia-supplied software. Each chassis may be directly connected to a monitor, keyboard, and mouse to create a standalone system, but it is typical to connect all chassis through an Ethernet network and run the IxExplorer client software or Tcl client software on one or more external control PC workstations. IxExplorer client software runs on any Windows 2000/XP based system or Windows Server 2003 (console usage or simultaneous remote terminal access for multiple users). Tcl client software runs on Windows 2000/XP based systems and several Unix-based systems.

Chassis Chain Timing Specification

- Chassis timing skew between like chassis <= +/- 40ns.
- Chassis timing skew between unlike chassis <= +/- 80ns.

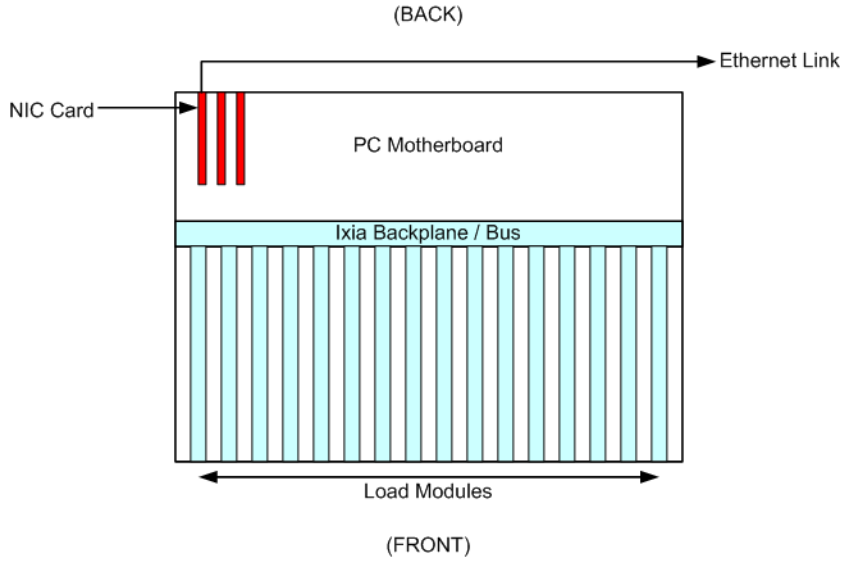
Based on the above numbers:

- Maximum latency error between like chassis due to the chassis <= +/- 40ns.
- Maximum latency error between unlike chassis due to the chassis <= +/- 80ns.

Chassis

Each Ixia chassis can operate as a complete standalone system when connected to a local monitor, keyboard, and mouse. The interior of an Ixia 1600T chassis is shown in the following figure.

Figure 2-2. Ixia 1600T Interior View (Top View)



The PC embedded in the chassis system is an Intel-compatible computer system which includes the following components:

- A Pentium processor
- Main memory
- Keyboard interface
- Mouse interface
- Internal connection to the Ixia Backplane
- Video interface capable of 1024 x 768 or greater resolution
- 10/100/1000 Mbps Ethernet Network Interface Card (NIC)

The Ixia Backplane is connected to the PC Motherboard, through an Ixia custom PCI interface card, and to the card slots where the Ixia load modules are installed.

Chassis Synchronization

Measurement of unidirectional latency and jitter in the transmission of data from a transmit port to a receive port requires that the relationship between time signatures at each of the ports is known. This can be accomplished by providing the following signals between chassis:

- Clock (frequency standard): This allows chassis to phase-lock their frequency standards so that a cycle counter on any chassis counts the same number of cycles during the same time interval. Each Ixia port maintains such a counter from a common chassis-wide frequency standard.
- Reset: A means must exist to either discover the fixed offset between their counters, or to simultaneously set the counters to a known value. You may think of this as the *zero reset*.

The use of both **Reset** and **Phase Lock** allow the establishment and maintenance of a fixed time reference between two or more chassis and the ports supported by the chassis.

In test setups where chassis and ports are physically close together, a sync cable is used to connect chassis in a 'chassis chain' for synchronization operation.

In widely distributed applications, such as monitoring traffic characteristics over a WAN, clock reference and/or reset signals cannot be transmitted between chassis over a physical connection because of unknown delay characteristics. An alternative means is required to satisfy these requirements.

Ixia has facilities that allow for the synchronization of independent Ixia chassis located anywhere in the world by replacing the existing inter-chassis sync cables with a widely available frequency and time standard supplied from an external source. This source provides a reference time used to obtain accurate latency and other measurements in a live global network. When geographically dispersed chassis are connected in this way, the combination is called a *virtual chassis chain*.

Physical Chaining

Independent Ixia 400T, 1600T, Optixia XL10, Optixia XM12, Optixia XM2, or Optixia X16 chassis may synchronize themselves with other chassis as shown in the following figure. The timing choices are explained in Table 2-2.

Figure 2-3. Physical Chaining

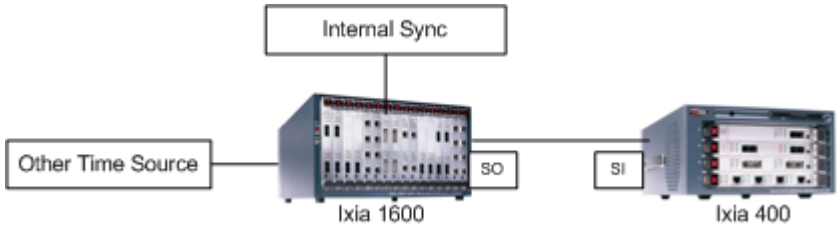


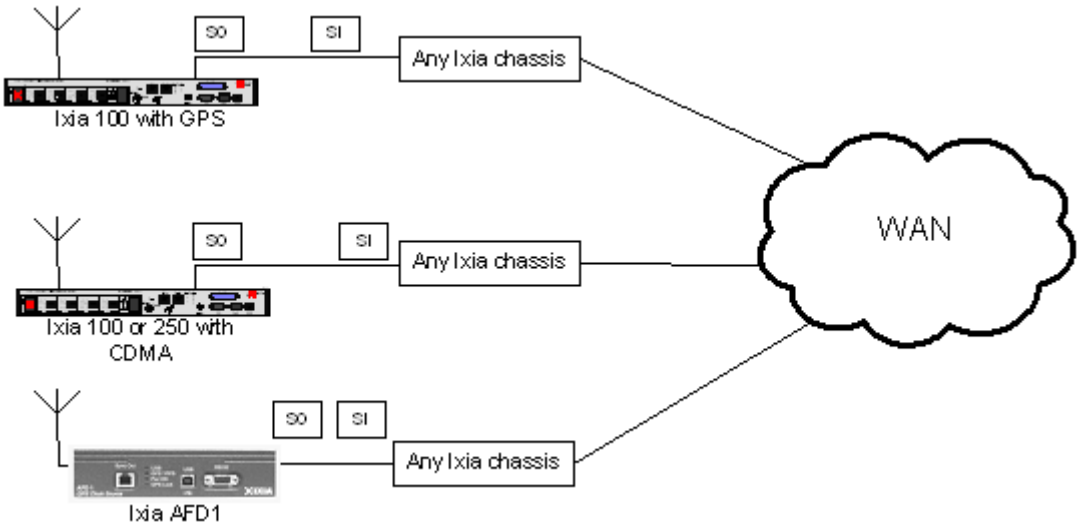
Table 2-2. Physical Chaining Timing Choices

Choice	Usage
Internal Sync (Synchronous)	If a chassis is used in a standalone manner or the master of a chassis chain, it may generate its own start signal. In general, there is insufficient timing accuracy between timing masters for measurements over any distance. This is also known as the Synchronous Timing mode.
Sync-In (SI)	If a chassis is a subordinate, either directly connected to the master chassis or further down the chain, it derives its timing from the previous chassis' Sync-Out (SO) signal.

Virtual Chaining

If two chassis are separated by any significant distance, a sync-out/sync-in cable cannot be used to connect them. In this case, either an Ixia Auxiliary Function Device (AFD1) or an Ixia 100 chassis with built-in Global Positioning Satellite (GPS), or an Ixia 100 or Ixia 250 with Code Division Multiple Access (CDMA) is used, one attached to each chassis through sync-out/sync-in cables, as shown in the following figure. The Ixia 100 maintains an accuracy of less than 150 nanoseconds when attached to a GPS antenna, or 100 microseconds when attached to a CDMA receiver, and provides chassis to chassis synchronization.

Figure 2-4. Virtual Chaining



To generate traffic for system latency testing, the Ixia 100 or Ixia 250 chassis can be used alone or in conjunction with another Ixia chassis, or the Ixia AFD1 (GPS receiver) can be used with any other Ixia chassis. The timing features available with these chassis are shown in Table 2-3 on page 2-7. A GPS antenna requires external mounting. Refer to Appendix C, *GPS Antenna Installation Requirements* for more information.

Table 2-3. Virtual Chaining Timing Choices

Choice	Usage
GPS	The Ixia 100 or ixia AFD1 requires connection to an external antenna to ‘capture’ multiple GPS satellites. It maintains an accuracy of less than 150 nano-seconds.
CDMA	The CDMA cellular network transmits an accurate time signal. CDMA (Code Division Multiple Access) cellular base-stations effectively act as GPS repeaters. The Ixia 100-CDMA or Ixia 250 receives the CDMA signals passively from an external antenna (you do not need to subscribe to any service) and decodes the embedded GMT time signal. Using this approach, the CDMA chassis can be time-synched to GMT. A CDMA antenna does not require external mounting.

The Sync-Out from a GPS or CDMA chassis is used to master a chassis chain at a specific geographic location. Since the Ixia 100 or Ixia 250 chassis has all other functions provided by the other Ixia chassis, it may also use independent timing when not used to synchronize with other chassis at other locations.

Note: CDMA reception depends on signal availability and may be impacted by cell location and chassis installation within the selected site. Consult your Ixia representative to determine the best solution for your installation.

For more information, including a formula for *Calculating Latency Accuracy for AFD1 (GPS)*, see Chapter 14, *Ixia GPS Auxiliary Function Device (AFD1)*.

Ixia Chassis Connections

A number of LEDs are available on the front panel of the Ixia 100 or Ixia 250, as described in Table 2-4 on page 2-8.

Table 2-4. IXIA 100 Front Panel LEDs

LED	Usage
Set Lock	Three LEDs indicate three separate status events: • 1: Indicates that the chassis is armed for a GPS sync event. • 2: Indicates that the antenna is correctly connected. • 3: Indicates that the GPS is tracking satellites.
Time Stamp	Three LEDs indicate the Stratum connection level. The Stratum indicates the accuracy the time stamp. The following list explains the significance of the number of LEDs lit: • 0: Indicates Stratum 4, within 100 us of absolute GMT. • 1: Indicates Stratum 3, within 10 us of absolute GMT. • 2: Indicates Stratum 2, within 1 us of absolute GMT. • 3: Indicates Stratum 1, within 100 ns of absolute GMT.
Shutdown	The chassis is in the process of being shut down.
Power	Power is applied to the chassis.

Similar information is available for the AFD1 GPS receiver in the Time Source tab of the Chassis Properties form (viewable through IxExplorer user interface).

Load Modules

Although each Ixia load module differs in particular capabilities, all modules share a common set of functions. Ixia load modules are generally categorized by network technology. The network technologies supported, along with names used to reference these technologies and more detailed information on load module differences, are available in the subsequent chapters of this manual.

Note: A load module can also be referred to as a *card*. The terms *load module* and *card* are used interchangeably in this manual.

The Load Module name prefix is used as the prefix to all load modules for that technology; for example, LM 100 in LM 100 TX. The IxExplorer name is used to label card and port types.

Some load modules are further labelled by the type of connector supported. Thus, a load module's name can be formed from a combination of its basic technology and the connector type. For example, LM 100 TX is the name of the 10/100 load module with RJ-45 connectors. An example for Packet Over SONET (POS) is the LMOC48c POS module, where no connector type is specified.

In addition, less expensive versions of several load modules are available. These are called Type-3 or Type-M modules, signified by an ending of '-3' or '-M' in the load module name and with a '-3'or '-M' suffix in the IxExplorer.

Newer boards also may have an 'L' before the last number in their part number, signifying the same limited functionality (example: LSM10GL1-01).

Some load modules can be configured with less than standard amount of memory. Modules configured with such memory have a notation as to the memory upgrade following the module name. For example, LM622MR-512.

Port Hardware

The ports on the Ixia load modules provide high-speed, transmit, capture, and statistics operation. The discussion which follows is broken down into a number of areas:

- *Types of Ports* on page 2-9: The different types of networking technology supported by Ixia load modules
- *Port Transmit Capabilities* on page 2-47: Facilities for generating data traffic
  - *Streams and Flows*: A set of packets, which may be grouped into bursts
  - *Bursts and the Inter-Burst Gap (IBG)*: A number of packets
  - *Packets and the Inter-Packet Gap (IPG)*: Individual frames/packets of data
- *Frame Data* on page 2-51: The construction of data within a frame/packet
- *Port Data Capture Capabilities* on page 2-66: Facilities for capturing data received on a port
- *Port Statistics Capabilities* on page 2-76: Facilities for obtaining statistics on each port

Types of Ports

The types of load module ports that Ixia offers are divided into these broad categories:

- *Ethernet*
- *Power over Ethernet*
- *10GE*
- *40GE and 100GE*
- *SONET/POS*
- *ATM*
- *BERT*

Only the currently available Ixia load modules are discussed in this chapter. Subsequent chapters in this manual discuss all supported load modules and their optional features.

Ethernet

Ethernet modules are provided with various feature combinations, as mentioned in the following list:

- Speed combinations: 10 Mbps, 100 Mbps, and 1000 Mbps
- Auto negotiation
- Pause control
- With and without on-board processors, also called Port CPUs (PCPUs). Load modules without processors only allow for very limited routing protocol emulation
- Power over Ethernet (Described in *Power over Ethernet* on page 2-10)
- External connections including the following:
    - RJ-45
    - MII
    - RMII - a custom Ixia connector
    - MT-RJ Fibre singlemode and multimode
    - SC multimode
    - GBIC singlemode and multimode

Power over Ethernet

The Power over Ethernet (PoE) load modules (PLM1000T4-PD and LSM1000POE4-02) are special purpose, 4-channel electronic loads. They are intended to be used in conjunction with Ixia ethernet traffic generator/analyzer load modules to test devices that conform to IEEE std 802.3af.

A PoE load module provides the hardware interface required to test the Power Sourcing Equipment (PSE) of a 802.3af compliant device by simulating a Powered Device (PD).

Power Sourcing Equipment (PSE)

A PSE is any equipment that provides the power to a single link Ethernet Network section. The PSE's main functions are to search the link section for a powered device (PD), optionally classify the PD, supply power to the link section (only if a PD is detected), monitor the power on the link section, and remove power when it is no longer requested or required.

There are two power sourcing methods for PoE—Alternative A and Alternative B.

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater, or midspan. A PSE that is coincident with the DTE/Repeater is an ‘Endpoint PSE.’ A PSE that is located within a link segment that is distinctly separate from and between the Media Dependent Interfaces (MDIs) is a ‘Midspan PSE.’

Endpoint PSEs may support either Alternative A, B, or both. Endpoint PSEs can be compatible with 10BASE-T, 100BASE-X, and/or 1000BASE-T.

Midspan PSEs must use Alternative B. Midspan PSEs are limited to operation with 10BASE-T and 100BASE-TX systems. Operation of Midspan PSEs on 1000BASE-T systems is beyond the scope of PoE.

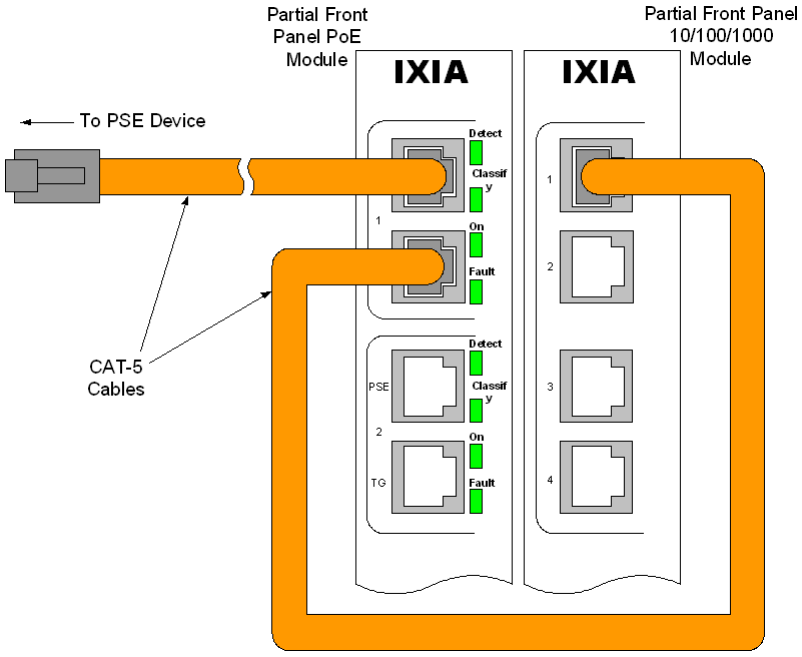
Powered Devices (PD)

A powered device either draws power or requests power by participating in the PD detection algorithm. A device that is capable of becoming a PD may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PSE.

One PoE Load Module emulates up to four PDs. The PoE Load Module (PLM) has eight RJ-45 interfaces—four of them used as PD-emulated ports, with each having its own corresponding interface that connects to a port on any Ixia 10/100/1000 copper-based Ethernet load module (includes LM100TX, all copper-based TXS, and Optixia load modules).

The following figure demonstrates how the PoE modules use an Ethernet card to transmit and receive data streams.

Figure 2-5. Data Traffic over PoE Set Up

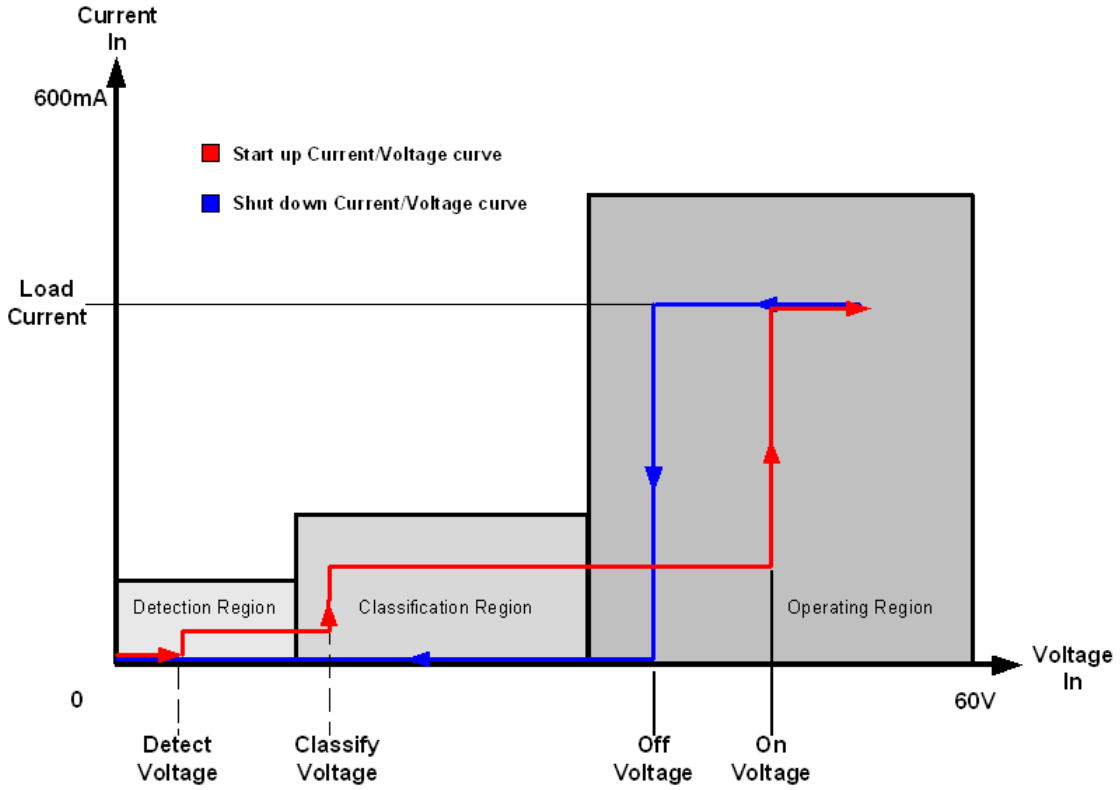


The emulated PD device can ‘piggy-back’ a signal from a different load module along the cable connected to the PSE from which it draws power. In this manner, the emulated PD can mimic a device that generates traffic, such as an IP phone.

Discovery Process

The main purpose for discovery is to prevent damage to existing Ethernet equipment. The Power Sourcing Equipment (PSE) examines the Ethernet cables by applying a small current-limited voltage to the cable and checking for the presence of a 25K ohm resistor in the remote Powered Device (PD). Only if the resistor is present, the full 48V is applied (and this is still current-limited to prevent damage to cables and equipment in fault conditions). The Powered Device must continue to draw a minimum current or the PSE removes the power and the discovery process begins again.

Figure 2-6. Discovery Process Voltage



There is also an optional extension to the discovery process where a PD may indicate to the PSE its maximum power requirements, called classification. Once there is power applied to the PD, normal transactions/data transfer occurs. During this period, the PD sends back a *maintain power signature* (MPS) to signal the PSE to continue to provide power.

PoE Acquisition Tests

During the course of testing with the PoE module, it may be necessary to measure the amplitude of the incoming current. The PoE module has the ability to measure amplitude versus time in following two ways:

- Time test: The amount of time that elapses between a *Start* and *Stop* incoming current measurement.
- Amplitude test: The amplitude of the current after a set amount of time from a *Start* incoming current setting.

In both scenarios, a Start trigger is set, indicating when the test should commence based on an incoming current value (in either DC Volts or DC Amps).

In a Time test, a Stop trigger is also set (in either DC Volts or DC Amps) indicating when the test is over. Once the Stop trigger is reached, the amount of time between the Start and Stop trigger is measured (in microseconds) and the result is reported.

In an amplitude test, an Amplitude Delay time is set (in microseconds), which is the amount of time to wait after the Start trigger is reached before ending the test. The amplitude at the end of the Amplitude Delay time is measured and is reported.

Both Start and Stop triggers must also have a defined Slope type, either positive or negative. A positive slope is equivalent to rising current, while a negative slope is equivalent to decreasing current. A current condition must agree with both the amplitude setting and the Slope type to satisfy the trigger condition.

An example of a Time test is shown in the following figure, and an example of an Amplitude test is shown in Figure 2-8.

Figure 2-7. PoE Time Acquisition Example

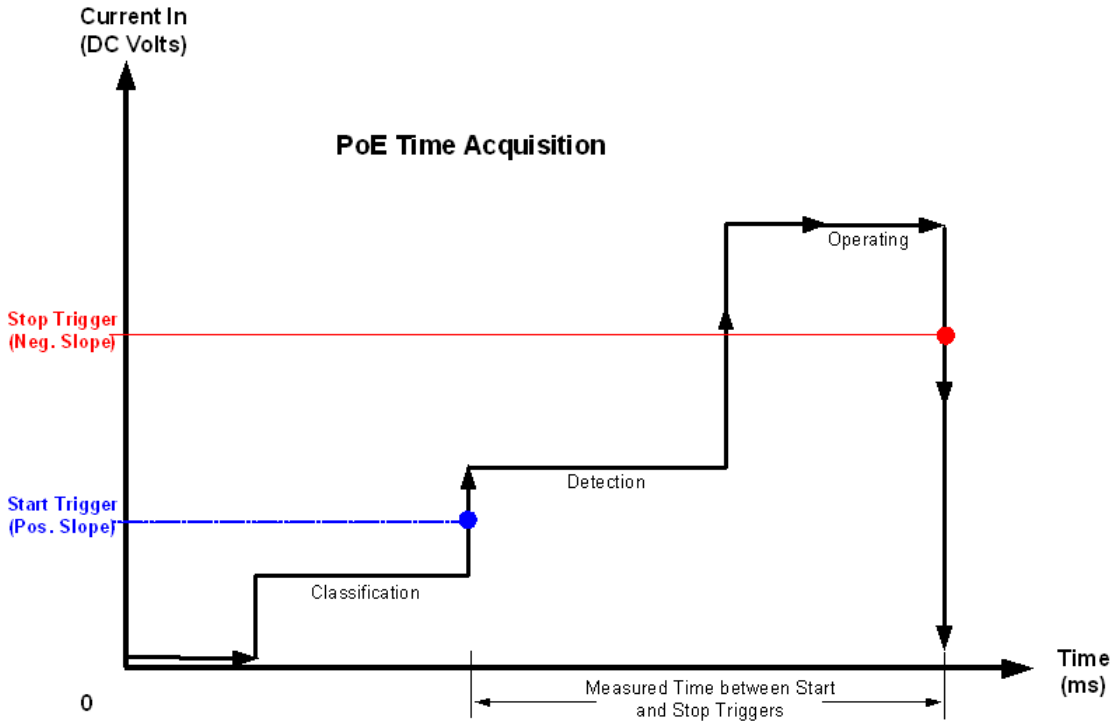
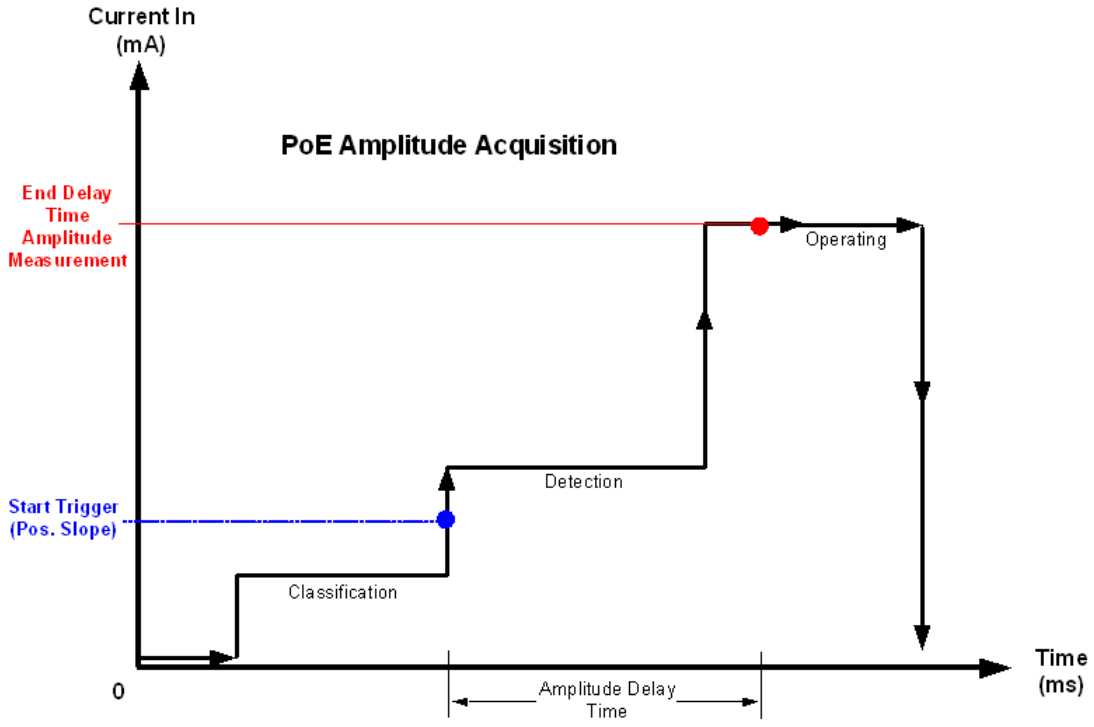


Figure 2-8. PoE Amplitude Acquisition Example



10GE

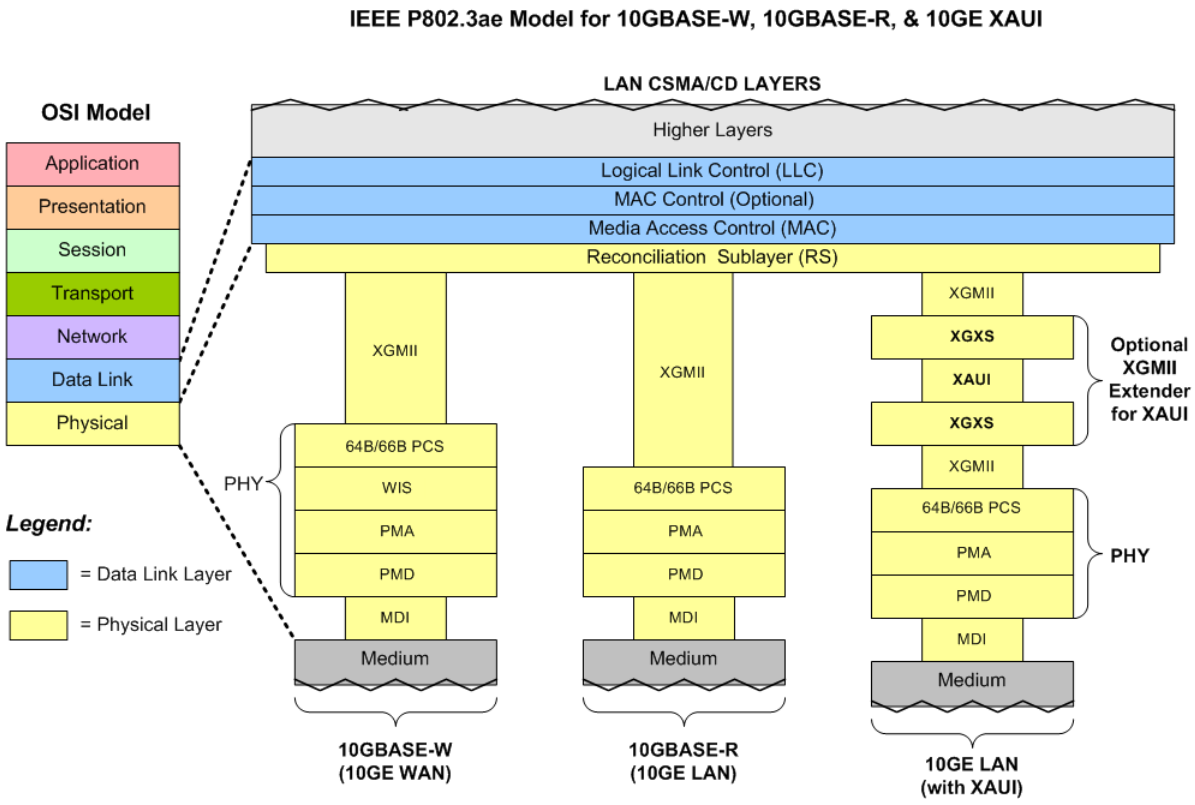
The 10 Gigabit Ethernet (10GE) family of load modules implements five of the seven IEEE 8.2.3ae compliant interfaces that run at 10 Gbit/second. Several of the load modules may also be software switched to OC192 operation.

The 10 GE load modules are provided with various feature combinations, as mentioned in the following list:

- Interfaces types: LAN, WAN, XAUI, and XENPAK
- Interface connectors: SC singlemode (LAN and WAN), SC multimode (LAN), LC singlemode/multimode, XFP, XAUI, and XENPAK
- Reach: Short, long, and extended
- Wavelengths: 850 nm, 1310 nm, 1550 nm

The relationship of the logical structures for the different 10 Gigabit types is shown in the diagram (adapted from the 802.3ae standard) in the following figure.

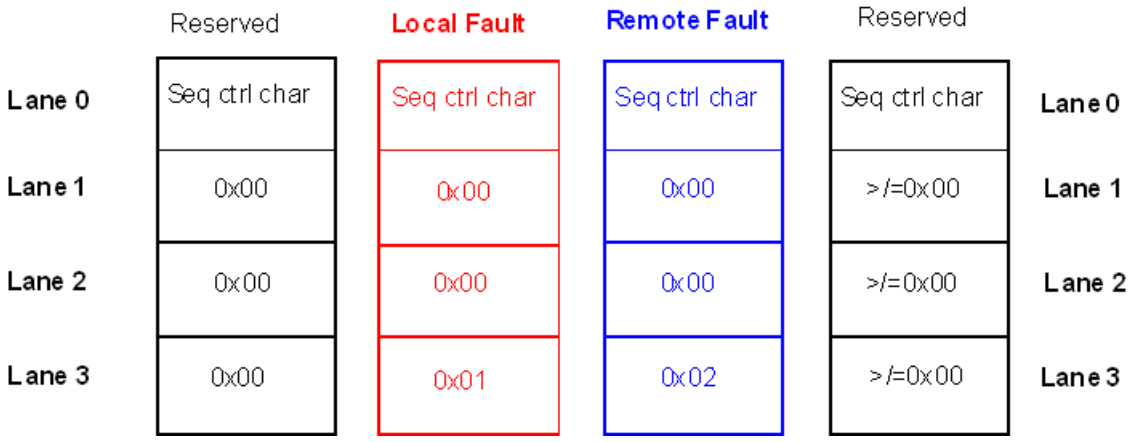
Figure 2-9. IEEE 802.3ae Draft—10 Gigabit Architecture



For 10GE XAUI and 10GE XENPAK modules, a Status message contains a 4-byte ordered set with a Sequence control character plus three data characters (in hex), distributed across the four lanes, as shown in the following figure. Four Sequence ordered sets are defined in IEEE 802.3ae, but only two of these—Local

Fault and Remote Fault—are currently in use; the other two are reserved for future use.

Figure 2-10. 10GE XAUI/XENPAK Sequence Ordered Sets

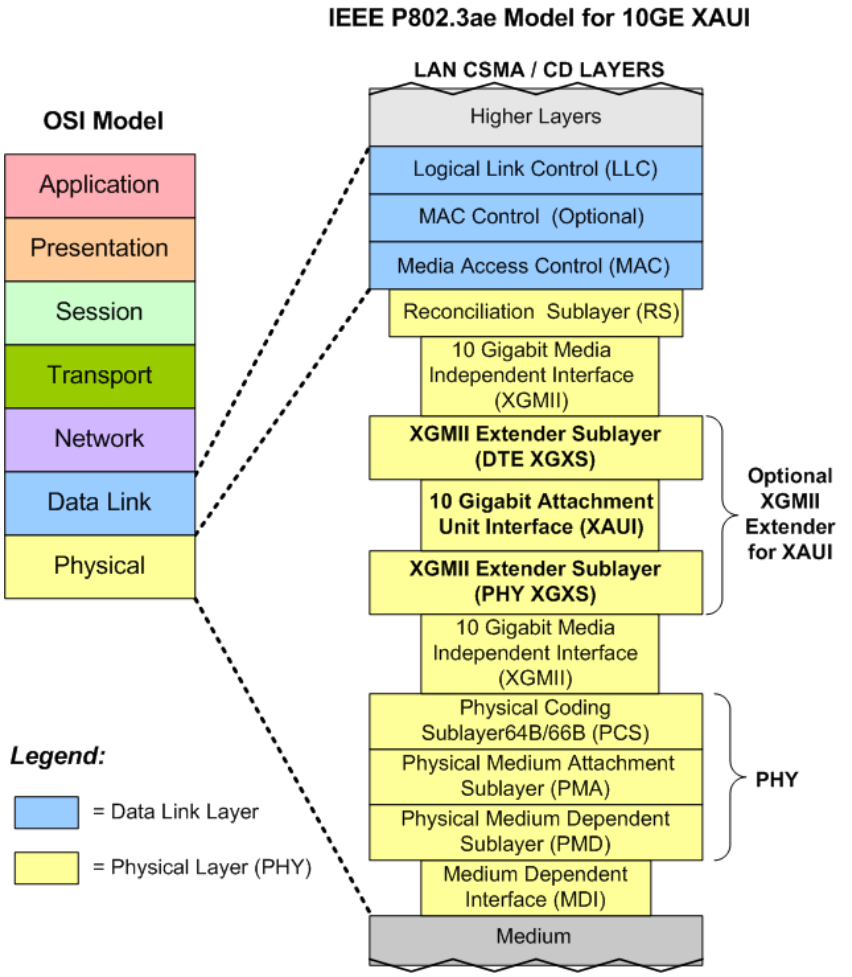


XAUI Interfaces

The 10 Gigabit XAUI interface has been defined in the IEEE draft specification P802.3ae by the 10 Gigabit Ethernet Task Force (10GEA). XAUI stands for 'X' (the Roman Numeral for 10, as in '10 Gigabit'), plus 'AUI' or Attachment Unit Interface originally defined for Ethernet.

The original Ethernet standard was defined in IEEE 802.3, and included MAC layer, frame size, and other 'standard' Ethernet characteristics. IEEE 802.3z defined the Gigabit standard. IEEE 802.3ae has been created to create a simplified version of SONET framing to carry native Ethernet-framed traffic over high-speed fiber networks. This new standard allows a smooth transition from 10 Gbps native Ethernet traffic to work with 9.6 Gbps for SONET at OC-192c rate over WAN and MAN links. The 10GE XAUI has a XAUI interface for connecting to another XAUI interface, such as on a DUT. A comparison of the IEEE P802.3ae model for XAUI and the OSI model is shown in the following figure.

Figure 2-11. IEEE P802.3ae Architecture for 10GE XAUI



Lane Skew

The Lane Skew feature provides the ability to independently delay one or more of the four XAUI lanes. The resolution of the skew is 3.2 nanoseconds (ns), which consists of 10 Unit Intervals (UIs), each of which is 320 picoseconds (ps). Each UI is equivalent to the amount of time required to transmit one XAUI bit at 3.125 Gbps.

Lane Skew allows a XAUI lane to be skewed by as much as 310 UI (99.2ns) with respect to the other three lanes. To effectively use this feature, the four lanes should be set to different skew values. Setting all four lanes to zero is equivalent to setting all four lanes to +80 UI. In both cases, the lanes are synchronous and there is no lane skew. When lane skewing is enabled, /A/, /K/, and /R/ codes are inserted into the data stream BEFORE the lanes are skewed. The principle behind lane skewing is shown in the diagrams in Figure 2-12 and Figure 2-13.

Figure 2-12. XAUI Lane Skewing—Lane Skew Disabled

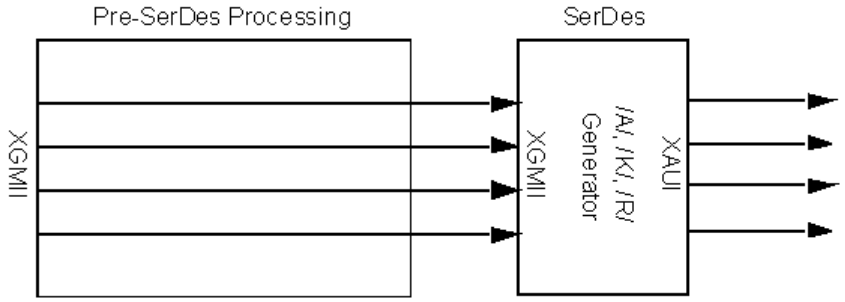
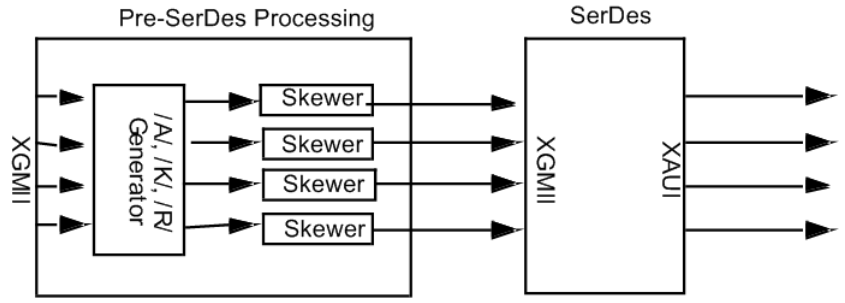


Figure 2-13. XAUI Lane Skewing—Lane Skew Enabled



Link Fault Signaling

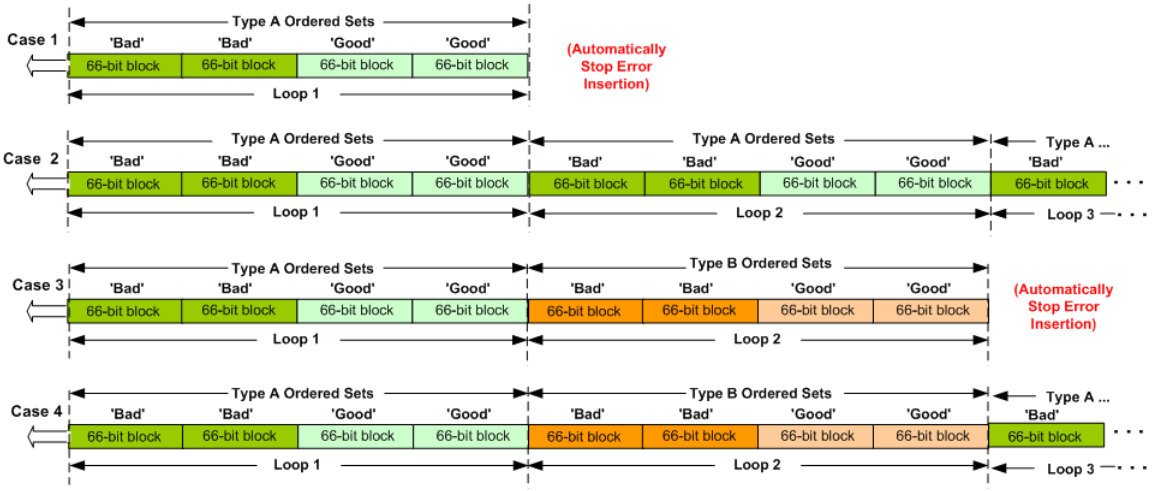
Link Fault Signaling is defined in Section 46 of the IEEE 802.3ae specification for 10 Gigabit Ethernet. When the feature is enabled, four statistics are added to the list in Statistic View for the port. One is for monitoring the Link Fault State; two for providing a count of the Local Faults and Remote Faults; and the last one is for indicating the state of error insertion, whether or not it is ongoing.

Link Fault Signaling originates with the PHY sending an indication of a local fault condition in the link being used as a path for MAC data. In the typical scenario, the Reconciliation Sublayer (RS) which had been receiving the data receives this Local Fault status, and then send a Remote Fault status to the RS which was sending the data. Upon receipt of this Remote Fault status message, the sending RS terminates transmission of MAC Data, sending only ‘Idle’ control characters until the link fault is resolved.

For the 10GE LAN and LAN-M serial modules, the Physical Coding Sublayer (PCS) of the PHY handles the transition from 64 bits to 66 bit ‘Blocks.’ The 64 bits of data are scrambled, and then a 2-bit synchronization (sync) header is attached before transmission. This process is reversed by the PHY at the receiving end.

Link Fault Signaling for the 10GE XAUI/XENPAK is handled differently across the four-lane XAUI optional XGMII extender layer, which uses 8B/10B encoding.

Figure 2-14. Examples of Link Fault Signaling Error Insertion



The examples in this figure are described in the following table:.

Table 2-5. Cases for Example

Case	Conditions
Case 1	Contiguous Bad Blocks = 2 (the minimum). Contiguous Good Blocks = 2 (the minimum). Send Type A ordered sets. Loop 1x.
Case 2	Contiguous Bad Blocks = 2 (the minimum). Contiguous Good Blocks = 2 (the minimum). Send Type A ordered sets. Loop continuously.
Case 3	Contiguous Bad Blocks = 2 (the minimum). Contiguous Good Blocks = 2 (the minimum). Send alternate ordered set types. Loop 1x.
Case 4	Contiguous Bad Blocks = 2 (the minimum). Contiguous Good Blocks = 2 (the minimum). Send alternate ordered set types. Loop continuously.

Link Alarm Status Interrupt (LASI)

The link alarm status is an active low output from the XENPAK module that is used to indicate a possible link problem as seen by the transceiver. Control registers are provided so that LASI may be programmed to assert only for specific fault conditions.

Efficient use of XENPAK and its specific registers requires an end-user system to recognize a connected transceiver as being of the XENPAK type. An Organizationally Unique Identifier (OUI) is used as the means of identifying a port as XENPAK, and also to communicate the device in which the XENPAK specific registers are located.

Ixia's XENPAK module allows for setting whether or not LASI monitoring is enabled, what register configurations to use, and the OUI. The XENPAK module can use the following registers:

- Rx Alarm Control (Register 0x9003): It can be programmed to assert only when specific receive path fault condition(s) are present.
- Tx Alarm Control (Register 0x9001): It can be programmed to assert only when specific transmit path fault condition(s) are present.
- LASI Control (Register 0x9002): A LASI control register that allows global masking of the Rx Alarm and Tx Alarm.

You can control the registers by setting a series of sixteen bits for each register. The register bits and their usage are described in the following tables.

Table 2-6. Rx Alarm Control

Bits	Description	Default
15 - 11	Reserved	0
10	Vendor Specific	N/A (vendor Setting)
9	WIS Local Fault Enable	1 (when implemented)
8 - 6	Vendor Specific	N/A (vendor Setting)
5	Receive Optical Power Fault Enable	1 (when implemented)
4	PMA/PMD Receiver Local Fault Enable	1 (when implemented)
3	PCS Receive Local Fault Enable	1
2 - 1	Vendor Specific	N/A (vendor Setting)
0	PHY XS Receive Local Fault Enable	1

Table 2-7. Tx Alarm Control

Bits	Description	Default
15 - 11	Reserved	0
10	Vendor Specific	N/A (vendor setting)
9	Laser Bias Current Fault Enable	1 (when implemented)

Table 2-7. Tx Alarm Control

Bits	Description	Default
8	Laser Temperature Fault Enable	1 (when implemented)
7	Laser Output Power Fault Enable	1 (when implemented)
6	Transmitter Fault Enable	1
5	Vendor Specific	N/A (vendor setting)
4	PMA/PMD Transmitter Local Fault Enable	1 (when implemented)
3	PCS Transmit Local Fault Enable	1
2 - 1	Vendor Specific	N/A (vendor setting)
0	PHY XS Transmit Local Fault Enable	1

Table 2-8. LASI Control

Bits	Description	Default
15 - 8	Reserved	0
7 - 3	Vendor Specific	0 (when implemented)
2	Rx Alarm Enable	0
1	Tx Alarm Enable	0
0	LS Alarm Enable	0

For more detailed information on LASI, see the online document *XENPAK MSA Rev. 3*.

40GE and 100GE

For theoretical information, refer to *40 Gigabit Ethernet and 100 Gigabit Ethernet Technology Overview White Paper*, published by Ethernet Allliance, November, 2008. This white paper may be obtained through the Internet.

http://www.ethernetalliance.org/images/40G_100G_Tech_overview.pdf

SONET/POS

SONET/POS modules are provided with various feature combinations:

- Different speeds: OC3, OC12, OC48, OC192, Fibre Channel, 2x Fibre Channel, and Gigabit Ethernet.

- Interfaces: SC singlemode and multimode (OC3, OC12, OC192), SC singlemode (OC48), no optical transceiver, SFP LC singlemode (Unframed BERT) and custom interface.
- Reach: long, intermediate and long.
- Wavelengths: 850nm, 1310nm and 1550nm.
- Local processor support. All SONET/POS load modules include a local processor, but the power of the processor and amount of memory varies.
- Variable clocking—OC48 only, see *Variable Rate Clocking* on page 2-22.
- Concatenated or channelized SONET operation, see *SONET Operation* on page 2-22.
- Error insertion, see *Error Insertion* on page 2-24.
- BERT: Bit Error Rate Testing both framed and unframed, see *BERT* on page 2-45.
- DCC: Data Communication Channel, see *DCC—Data Communications Channel* on page 2-25.
- RPR: Resilient Packet Ring, see *RPR—Resilient Packet Ring* on page 2-26.
- GFP: Generic Framing Procedure, see *GFP—Generic Framing Procedure* on page 2-29.
- PPP: Point to Point protocol, see *PPP Protocol Negotiation* on page 2-33.
- HDLC: High-Level Data Link Control, see *HDLC* on page 2-39.
- Frame Relay: see *Frame Relay* on page 2-39.
- DSCP: see *DSCP—Differentiated Services Code Point* on page 2-39.

Variable Rate Clocking

The OC48 VAR allows a variation of +/- 100 parts per million (ppm) from the clock source's nominal frequency, through a DC voltage input into the BNC jack marked 'DC IN' on the front panel. The frequency may be monitored through the BNC marked 'Freq Monitor.'

SONET Operation

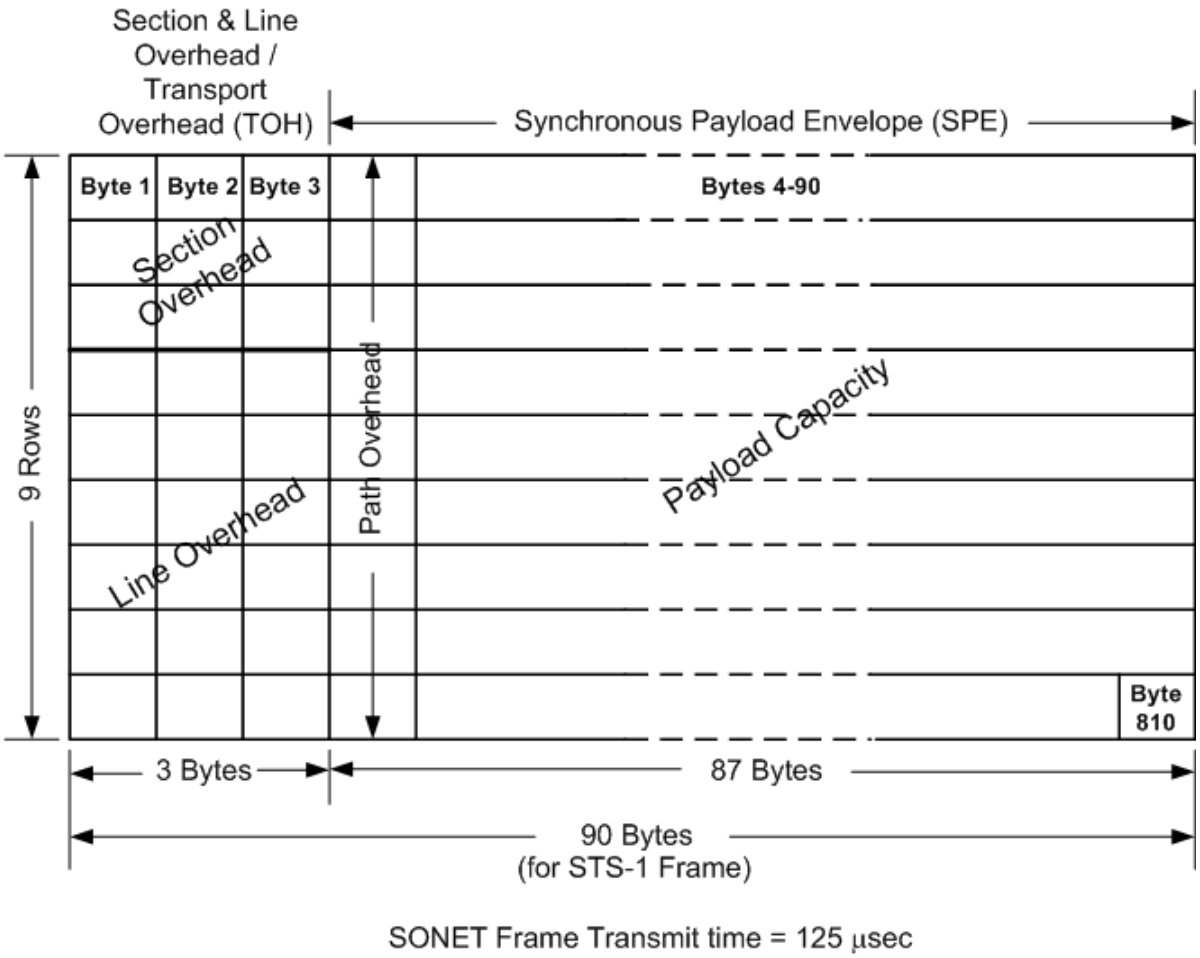
A Synchronous Optical NETwork/Synchronous Digital Hierarchy (SONET/SDH) frame is based on the Synchronous Transport Signal-1 (STS-1) frame, whose structure is shown in Figure 2-15 on page 2-23. Transmission of SONET Frames of this size correspond to the Optical Carrier level 1 (OC-1).

An OC-3c, consists of three OC-1/STS-1 frames multiplexed together at the octet level. OC-12c, OC-48c, and OC-192c, are formed from higher multiples of the basic OC-1 format. The suffix 'c' indicates that the basic frames are concatenated to form the larger frame.

Ixia supports both concatenated (with the 'c') and channelized (without the 'c') interfaces. Concatenated interfaces send and receive data in a single streams of

data. Channelized interfaces send and receive data in multiple independent streams.

Figure 2-15. Generated Frame Contents—SONET STS-1 Frame



The contents of the SONET STS-1 frame are described in Table 2-9 on page 2-23.

Table 2-9. SONET STS-1 Frame Contents

Section	Description
Section Overhead (SOH)	Consists of 9 bytes which include information relating to performance monitoring of the STS-n signal, and framing.
Line Overhead (LOH)	Consists of 18 bytes which include information relating to performance monitoring of the individual STS-1s, protection switching information, and line alarm indication signals.

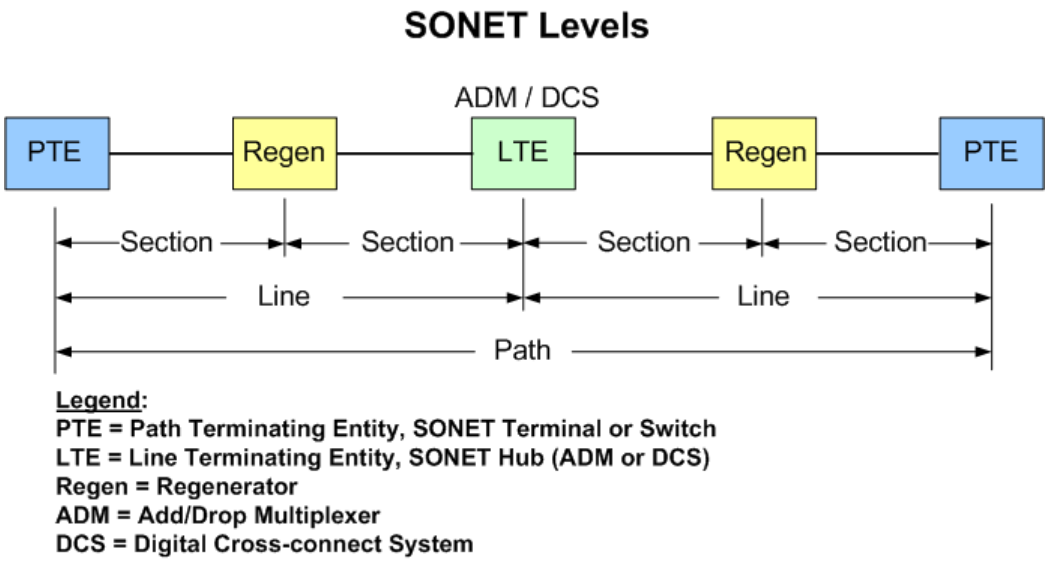
Table 2-9. SONET STS-1 Frame Contents

Section	Description
Transport Overhead (TOH)	Consists of a combination of the Section Overhead and Line Overhead sections of the STS-1 frame.
Path Overhead (POH)	Part of the Synchronous Payload Envelope (SPE), contains information on the contents of the SPE, and handles quality monitoring.
Synchronous Payload Envelope (SPE)	Contains the payload information, the packets which are being transmitted, and includes the Path Overhead bytes.
Payload Capacity	Part of the SPE, and contains the packets being transmitted.

The SONET STS-1 frame is transmitted at a rate of 51.84 Mbps, with 49.5 Mbps reserved for the frame payload. A SONET frame is transmitted in 125 microseconds, with the order of transmission of the starting with Row 1, Byte 1 at the upper left of the frame, and proceeding by row from top to bottom, and from left to right.

The section, line, and path overhead elements are related to the manner in which SONET frames are transmitted, as shown in Figure 2-16 on page 2-24.

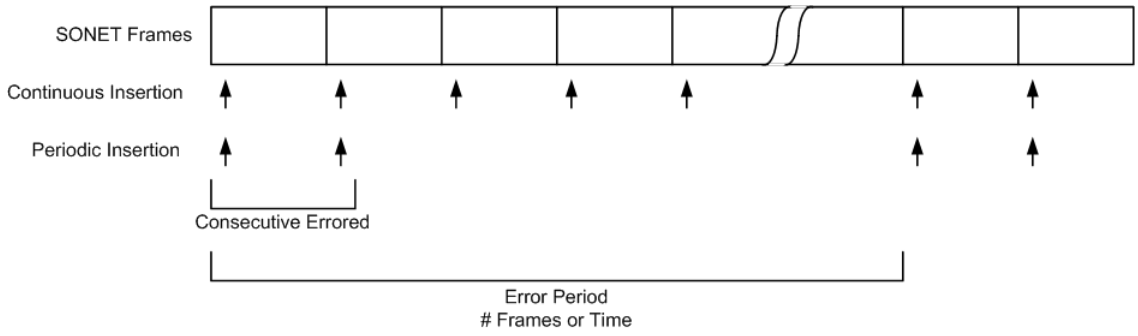
Figure 2-16. Example Diagram of SONET Levels and Network Elements



Error Insertion

A variety of deliberate errors may be inserted in SONET frames in the section, line or path areas of a frame. The errors which may be inserted vary by particular load module. Errors may be inserted continuously or periodically as shown in Figure 2-17 on page 2-25.

Figure 2-17. SONET Error Insertion



An error may be inserted in one of two manners:

- Continuous: Each SONET frame receives the error.
- Periodic: A number of errors are inserted in consecutive frames and the pattern is repeated based on a number of frames or a period of time. Predefined periods are available, or you may create your own predefined periods.

Each error may be individually inserted continuously or periodically. Errors may be inserted on a one time basis over a number of frames as well.

DCC—Data Communications Channel

The data communication channel is a feature of SONET networks which uses the DCC bytes in the transport overhead of each frame. This is used for control, monitoring and provisioning of SONET connections. Ixia ports treat the DCC as a data stream which 'piggy-backs' on the normal SONET stream. The DCC and normal (referred to as the SPE - Synchronous Payload Envelope) streams can be transmitted independently or at the same time.

A number of different techniques are available for transmitting DCC and SPE data, utilizing Ixia streams and flows (see *Streams and Flows* on page 2-47) and advanced stream scheduler (see *Advanced Streams* on page 2-48).

SRP—Spatial Reuse Protocol

The Spatial Reuse Protocol (SRP) was developed by Cisco for use with ring-based media. It derives its name from the spatial reuse properties of the packet handling procedure. This optical transport technology combines the bandwidth-efficient and service-rich capabilities of IP routing with the bandwidth-rich, self-healing capabilities of fiber rings to deliver fundamental cost and functionality advantages over existing solutions. In SRP mode, the usual POS header (PPP, and so forth) is replaced by the SRP header.

SRP networks use two counter-rotating rings. One Ixia port may be used to participate in one of the rings; two may be used to simultaneously participate in both rings. Ixia supports SRP on both OC48 and OC192 interfaces.

In SRP-mode, SRP packets can be captured and analyzed. The IxExplorer capture view displays packet analysis which understands SRP packets. The Ixia hardware also collects specific SRP related statistics and performs filtering based on SRP header contents.

Any of the following SRP packet types may be generated in a data stream, along with normal IPv4 traffic:

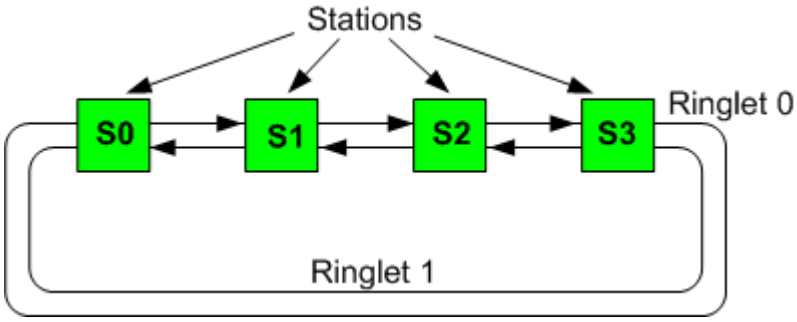
- SRP Discovery
- SRP ARP
- SRP IPS (Intelligent Protection Switching)

RPR—Resilient Packet Ring

Ixia's optional Resilient Packet Ring (RPR) implementation is available on the OC-48c and OC-192c POS load modules. RPR is a proposed industry standard for MAC Control on Metropolitan Area Networks (MANs), defined by IEEE P802.17. This feature provides a cost-effective method to optimize the transport of bursty traffic, such as IP, over existing ring topologies.

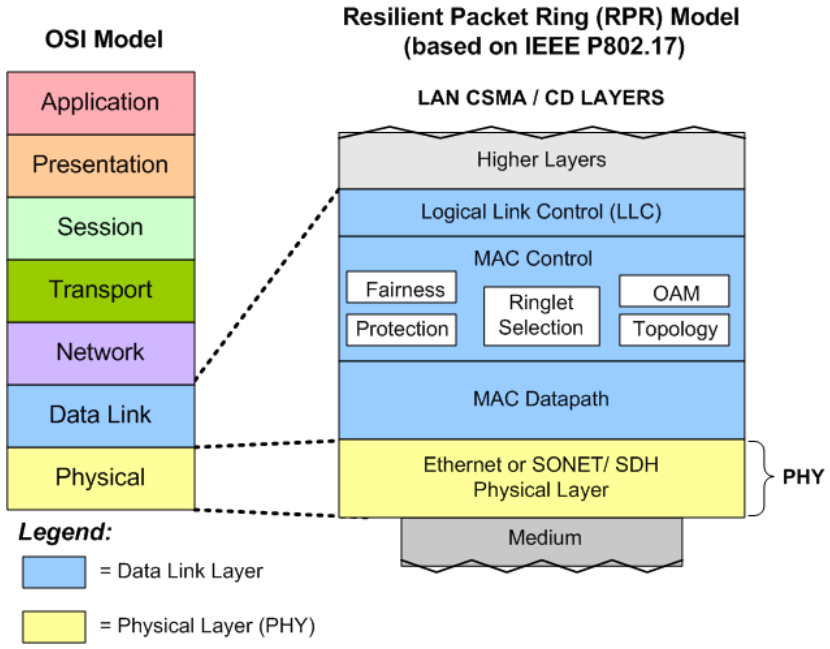
A diagram showing a simplified model of an RPR network is shown in Figure 2-18 on page 2-26. It is made up of two, counter-rotating 'ringlets,' with nodes called 'stations' supporting MAC Clients that exchange data and control information with remote peers on the ring. Up to 255 nodes can be supported on the ring structure.

Figure 2-18. RPR Ring Network Diagram



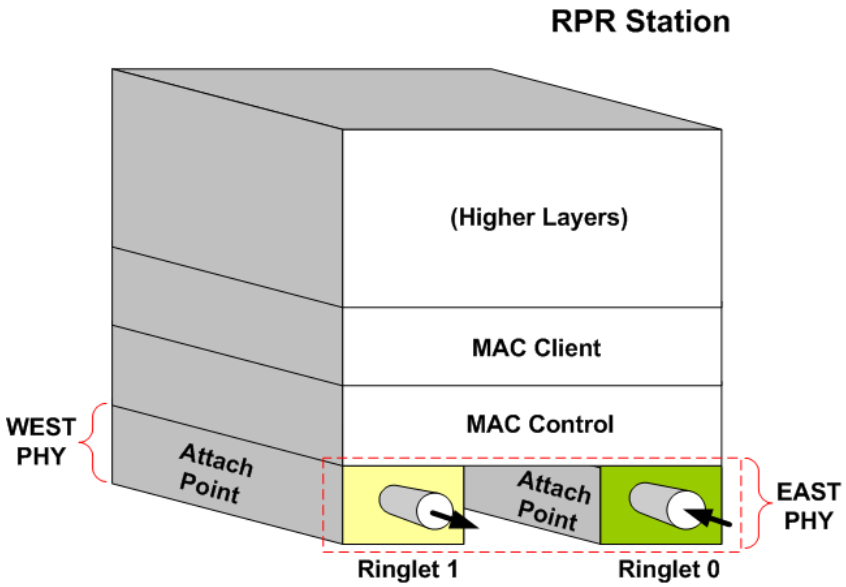
The RPR topology discovery is handled by a MAC sublayer, and a protection function maintains network connectivity in the event of a station or span failure. The structure of the RPR layers, compared to the OSI model, is illustrated in a diagram based on IEEE 802.17, shown in Figure 2-19 on page 2-27.

Figure 2-19. RPR Layers



A diagram of the layers associated with an RPR Station is shown in Figure 2-20 on page 2-27.

Figure 2-20. RPR Layer Diagram

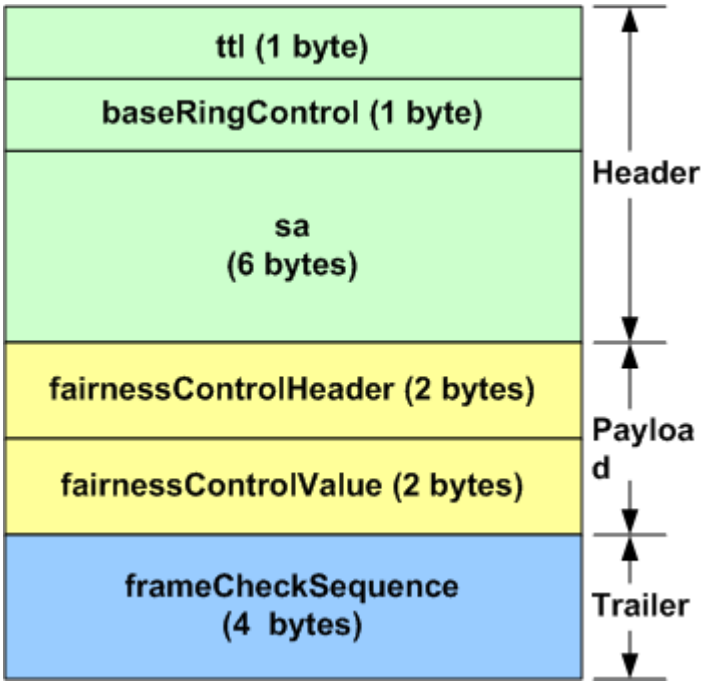


The Ixia implementation allows for the configuration and transmission of the following types of RPR frames:

- RPR Fairness Frames: The RPR Fairness Algorithm (FA) is used to manage congestion on the ringlets in an RPR network. Fairness frames are sent periodically to advertise bandwidth usage parameters to other nodes in the network to maintain weighted fair share distributions of bandwidth. The

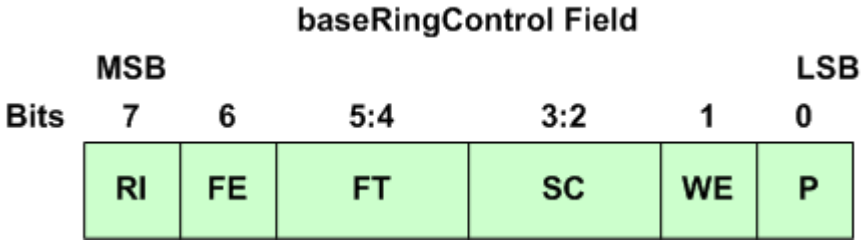
messages are sent in the direction opposite to the data flow, and therefore, on the other ringlet. A diagram of the RPR Fairness Frame, per IEEE 802.17/D2.1, is shown in Figure 2-21 on page 2-28.

Figure 2-21. RPR Fairness Frame Format



A diagram of the baseRingControl byte, part of the Ring Control header for all types of RPR frames, is shown in Figure 2-22 on page 2-28.

Figure 2-22. RPR baseRingControl Byte



- RPR Topology Discovery. Two types of messages are used:
  - RPR Topology Discovery Message: for the discovery of the physical topology.
  - RPR Topology Extended Status Message: for the transmission of additional information from a node concerning bandwidth and other configuration options. This format uses TLV (Type-Length-Value) options, including:
    - Weight
    - Total reserved bandwidth
    - Neighbor address

    - Individual reserved bandwidth
    - Station name
    - Vendor specific data
- RPR Protection Switching Message: used to support automatic, rapid switching of traffic in the presence of a ring failure.
- RPR Operations, Administration and Management (OAM). Three messages are supported:
    - Echo Request and Response messages
    - Flush Frames
    - Vendor specific message

GFP—Generic Framing Procedure

GFP provides a generic mechanism to adapt traffic from higher-layer client signals over a transport network. Currently, two modes of client signal adaptation are defined for GFP.

- A PDU-oriented adaptation mode, referred to as Frame-Mapped GFP (GFP-F, for traffic such as IP/PPP or Ethernet MAC).
- A block-code oriented adaptation mode, referred to as Transparent GFP (GFP-T, for traffic such as Fibre Channel or ESCON/SBCON).

In the Frame-Mapped adaptation mode, the Client/GFP adaptation function operates at the data link (or higher) layer of the client signal. Client PDU visibility is required, which is obtained when the client PDUs are received from either the data layer network or a bridge, switch, or router function in a transport network element.

For the Transparent adaptation mode, the Client/GFP adaptation function operates on the coded character stream, rather than on the incoming client PDUs. Processing of the incoming code word space for the client signal is required.

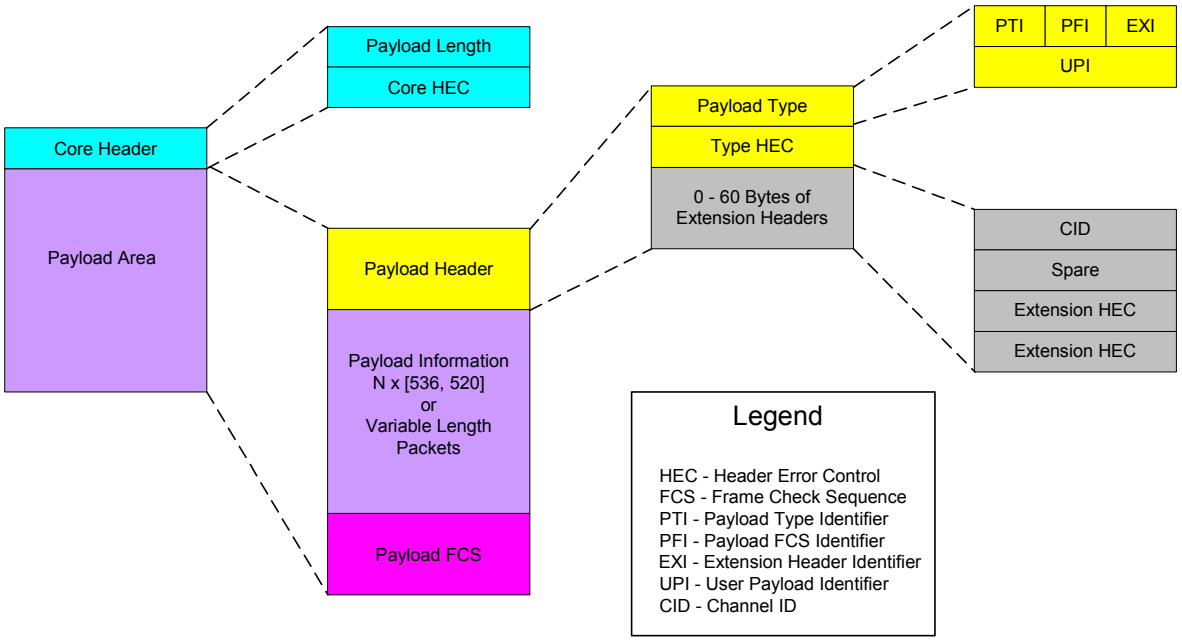
Two kinds of GFP frames are defined: GFP client frames and GFP control frames. GFP also supports a flexible (payload) header extension mechanism to facilitate the adaptation of GFP for use with diverse transport mechanisms.

GFP uses a modified version of the Header Error Check (HEC) algorithm to provide GFP frame delineation. The frame delineation algorithm used in GFP differs from HEC in two basic ways:

- The algorithm uses the PDU Length Indicator field of the GFP Core Header to find the end of the GFP frame.
- HEC field calculation uses a 16-bit polynomial and, consequently, generates a two-octet cHEC field.

A diagram of the format for a GFP frame is shown in Figure 2-23 on page 2-30.

Figure 2-23. GFP Frame Elements



The sections of the GFP frame are described in the following list:

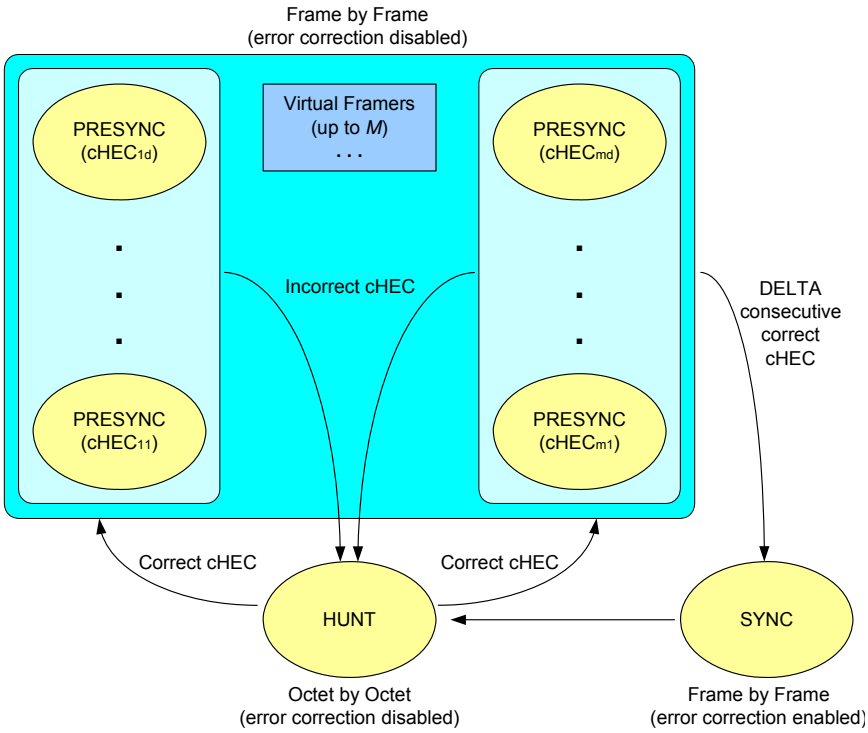
- Payload Length Indicator (PLI): The two-octet PLI field contains a binary number representing the number of octets in the GFP Payload Area. The absolute minimum value of the PLI field in a GFP client frame is 4 octets. PLI values 0-3 are reserved for GFP control frame usage.
- Core Header Error Control (cHEC): The two-octet Core Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the Core Header by enabling both single-bit error correction and multi-bit error detection.
- Type Header Error Control (tHEC): The two-octet Type Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the Type field by enabling both single-bit error correction and multi-bit error detection.
- Extension Header Error Control (eHEC): The two-octet Extension Header Error Control field contains a CRC-16 error control code that protects the integrity of the contents of the extension headers by enabling both single-bit error correction (optional) and multi-bit error detection.
- Connection Identification (CID): The CID is an 8-bit binary number used to indicate one of 256 communications channels at a GFP termination point.
- Payload: The GFP Payload Area, which consists of all octets in the GFP frame after the GFP Core Header, is used to convey higher layer specific protocol information. This variable length area may include from 4 to 65,535 octets. The GFP Payload Area consists of two common components:
  - A Payload Header and a Payload Information field
  - An optional Payload FCS (pFCS) field

Practical GFP MTU sizes for the GFP Payload Area are application specific.

- Frame Check Sequence (FCS): The GFP Payload FCS is an optional, four-octet long, frame check sequence. It contains a CRC-32 sequence that protects the contents of the GFP Payload Information field. A value of 1 in the PFI bit within the Type field identifies the presence of the payload FCS field.

GFP frame delineation is performed based on the correlation between the first two octets of the GFP frame and the embedded two-octet cHEC field. Figure 2-24 on page 2-31 shows the state diagram for the GFP frame delineation method.

Figure 2-24. GFP State Transitions



The state diagram works as follows:

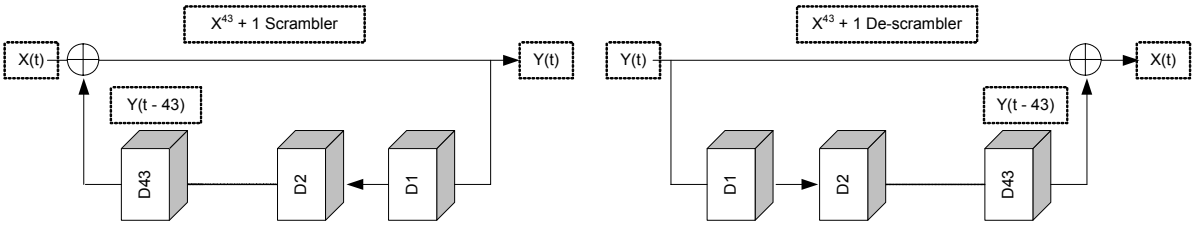
1. In the HUNT state, the GFP process performs frame delineation by searching octets for a correctly formatted Core Header over the last received sequence of four octets. Once a correct cHEC match is detected in the candidate Payload Length Indicator (PLI) and cHEC fields, a candidate GFP frame is identified and the receive process enters the PRESYNC state.
2. In the PRESYNC state, the GFP process performs frame delineation by checking frames for a correct cHEC match in the presumed Core Header of the next candidate GFP frame. The PLI field in the Core Header of the preceding GFP frame is used to find the beginning of the next candidate GFP frame. The process repeats until a set number of consecutive correct cHECs are confirmed, at which point the process enters the SYNC state. If an incorrect cHEC is detected, the process returns to the HUNT state.

3. In the SYNC state, the GFP process performs frame delineation by checking for a correct cHEC match on the next candidate GFP frame. The PLI field in the Core Header of the preceding GFP frame is used to find the beginning of the next candidate GFP frame. Frame delineation is lost whenever multiple bit errors are detected in the Core Header by the cHEC. In this case, a GFP Loss of Frame Delineation event is declared, the framing process returns to the HUNT state, and a client Server Signal Failure (SSF) is indicated to the client adaptation process.
4. Idle GFP frames participate in the delineation process and are then discarded.

Robustness against false delineation in the resynchronization process depends on the value of DELTA. A value of DELTA = 1 is suggested. Frame delineation acquisition speed can be improved by the implementation of multiple 'virtual framers,' whereby the GFP process remains in the HUNT state and a separate PRESYNC substate is spawned for each candidate GFP frame detected in the incoming octet stream.

Scrambling of the GFP Payload Area is required to provide security against payload information replicating scrambling word (or its inverse) from a frame synchronous scrambler (such as those used in the SDH RS layer or in an OTN OPUk channel). Figure 2-25 on page 2-32 illustrates the scrambler and descrambler processes.

Figure 2-25. GFP Scrambling



All octets in the GFP Payload Area are scrambled using a $x^{43} + 1$ self-synchronous scrambler. Scrambling is done in network bit order.

At the source adaptation process, scrambling is enabled starting at the first transmitted octet after the cHEC field, and is disabled after the last transmitted octet of the GFP frame. When the scrambler or descrambler is disabled, its state is retained. Hence, the scrambler or descrambler state at the beginning of a GFP frame Payload Area is, thus, the last 43 Payload Area bits of the GFP frame transmitted in that channel immediately before the current GFP frame.

The activation of the sink adaptation process descrambler also depends on the present state of the cHEC check algorithm:

- In the HUNT and PRESYNC states, the descrambler is disabled.
- In the SYNC state, the descrambler is enabled only for the octets between the cHEC field and the end of the candidate GFP frame.

CDL— Converged Data Link

10GE LAN, 10GE XAUI, 10GE XENPAK, 10GE WAN, and 10GE WAN UNIPHY modules all support the Cisco CDL preamble format.

The Converged Data Link (CDL) specification was developed to provide a standard method of implementing operation, administration, maintenance, and provisioning (OAM&P) in Ethernet packet-based optical networks without using a SONET/SDH layer.

PPP Protocol Negotiation

The Point-to-Point Protocol (PPP) is widely used to establish, configure and monitor peer-to-peer communication links. A PPP session is established in a number of steps, with each step completing before the next one starts. The steps, or layers, are:

1. Physical: a physical layer link is established.
2. Link Control Protocol (LCP): establishes the basic communications parameters for the line, including the Maximum Receive Unit (MRU), type of authentication to be used and type of compression to be used.
3. Link quality determination and authentication. These are optional processes. Quality determination is the responsibility of PPP Link Quality Monitoring (LQM) Protocol. Once initiated, this process may continue throughout the life of the link. Authentication is performed at this stage only. There are multiple protocols which may be employed in this process; the most common of these are PAP and CHAP.
4. Network Control Protocol (NCP): establishes which network protocols (such as IP, OSI, MPLS) are to be carried over the link and the parameters associated with the protocols. The protocols which support this NCP negotiation are called IPCP, OSINLCP, and MPLSCP, respectively.
5. Network traffic and sustaining PPP control. The link has been established and traffic corresponding to previously negotiated network protocols may now flow. Also, PPP control traffic may continue to flow, as may be required by LQM, PPP keepalive operations, and so forth.

All implementations of PPP must support the Link Control Protocol (LCP), which negotiates the fundamental characteristics of the data link and constitutes the first exchange of information over an opening link. Physical link characteristics (media type, transfer rate, and so forth) are not controlled by PPP.

The Ixia PPP implementation supports LCP, IPCP, MPLSCP, and OSINLCP. When PPP is enabled on a given port, LCP and at least one of the NCPs must complete successfully over that port before it is administratively ‘up’ and therefore be ready for general traffic to flow.

Each Ixia POS port implements a subset of the LCP, LQM, and NCP protocols. Each of the protocols is of the same basic format. For any connection, separate negotiations are performed for each direction. Each party sends a *Configure-*

Request message to the other, with options and parameters proposing some form of configuration. The receiving party may respond with one of three messages:

- *Configure-Reject*: The receiving party does not recognize or prohibits one or more of the suggested options. It returns the problematic options to the sender.
- *Configure-NAK*: The receiving party understands all of the options, but finds one or more of the associated parameters unacceptable. It returns the problematic options, with alternative parameters, to the sender.
- *Configure-ACK*: The receiving party finds the options and parameters acceptable.

For the *Configure-Reject* and *Configure-NAK* requests, the sending party is expected to reply with an alternative *Configure-Request.*

The Ixia port may be configured to immediately start negotiating after the physical link comes up, or passively wait for the peer to start the negotiation. Ixia ports both sends and responds to PPP keepalive messages called echo requests.

LCP—Link Control Protocol Options

The following sections outline the parameters associated with the Link Control Protocol. LCP includes a number of possible command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link.

Numerous RFCs are associated with LCP, but the most important RFCs are RFC 1661 and RFC 1662. The HDLC/PPP header sequence for LCP is FF 03 C0 21.

During the LCP phase of negotiation, the Ixia port makes available the following options:

- Maximum Receive Unit: This LCP parameter (actually the set of Maximum Receive Unit (MRU) and Maximum Transmit Unit (MTU)) determines the maximum allowed size of any frame sent across the link subsequent to LCP completion. To be fully standards-compliant, an implementation must not send a frame of length greater than its MTU + 4 bytes + CRC length. For instance, if the negotiated MTU for a port is 2000 and 32 bit CRC is in use, no frame larger than 2008 bytes should ever be sent out that port. Packets that are larger are expected to be fragmented before transmitting or to be dropped. The Ixia port's MTU is the peer's MRU following LCP negotiation. Strictly speaking, the receiving side can assume that frames received is not greater than the MRU. In practice, however, an implementation should be capable of accepting larger frames. If a peer rejects this option altogether, the negotiated setting defaults to 1,500. Regardless of the negotiated MRU, all implementations must be capable of accepting frames with an information field of at least 1,500 bytes.

  For the transmit direction portion of the negotiation, the peer sends the Ixia port its configuration request. The Ixia port accepts and acknowledges the peer's requested MRU as long as it is less than or equal to the specified

user's desired transmit value (but greater than 26). For the receive direction portion of the negotiation, the Ixia port sends a configuration request based on the user's desired value. Generally, the Ixia port accepts what the peer desires (if it acknowledges the request, then the user value is used, or if the peer sends a *Configure-Nak* with another value the Ixia port uses that value as long as it is valid). This approach is used to maximize the probability of successful negotiation.

- Asynchronous Control Character Map: ACCM is only really pertinent to *asynchronous* links. On asynchronous lines, certain characters sent over the wire can have special meaning to one or more receiving entities. For instance, common implementations of the widely used XON/XOFF flow control protocol assign the ASCII DC3 character (0x13) to XOFF. On such a link, an embedded data byte that happens to have the value 0x13 would be misinterpreted by a receiver as an XOFF command, and cause suspension of reception. To avoid this problem, the 0x13 character embedded in the data could be sent through an 'escape sequence' which consists of preceding the data character with a dedicated tag character and modifying the data character itself.

  The Asynchronous Control Character Map (ACCM) LCP parameter allows independent designation of each character in the range 0x00 thru 0x1F as a control character. A control character is sent/received with a preceding 'control-escape' character (0x7D). When the 0x7D is seen in the received data stream, the 0x7D is dropped and the next character is exclusive-or'd with 0x20 to get the original transmitted character. ACCM negotiation consists of exchanging masks between peers to reach an agreement as to which characters are treated as special control characters on transmission and reception. For example, sending a mask of 0xFFFFFFFF means all characters in the range 0x00 thru 0x1F are sent with escape sequences; a mask of 0 means no special handling, so all characters are arbitrary data.

  Packet over SONET is an octet-synchronous medium. If the link is direct between POS peers, neither side should be generating control-escapes. (Exceptions to this are bytes 0x7D and 0x7E: the former is the special control escape character itself; the latter is the start/end frame marker. Escaping of these two characters is generally handled directly by physical layer hardware). On links in which there is some kind of intermediate asynchronous media, it is required that whatever device performs the asynchronous to synchronous conversion must also take care of any special character handling, isolating this from any POS port. See RFC 1662, sections 4.1 and 6.

  If ACCM negotiation is enabled, the Ixia port advertises an ACCM mask of 0 to its peer in its LCP configuration request. The Ixia port accept whatever the peer puts forth, but does not act on the results. Regardless of the final negotiated settings for receive and transmit ACCM, the Ixia port does not send escape control sequences nor does it expect to receive them. This is the nature of a synchronous PPP medium, such as POS.

- Magic Number: A magic number is a 32-bit value, ideally numerically random, which is placed in certain PPP control packets. Magic numbers aid in detection of looped links. If a received PPP packet that includes a magic number matches a previously transmitted packet, including magic number, the link is probably looped.

  IxExplorer and the Tcl APIs allow global enable/disable of magic number negotiation. If the 'Use Magic Number' feature is enabled, the Ixia port does not request magic number of its peer and rejects the option if the peer requests it. If the check box is selected, the port attempts to negotiate magic number. The result of the bi-directional negotiation process is displayed in the fields for transmit and receive: an indication of whether magic number is enabled is written in the field for the corresponding direction.

NCP—Network Control Protocols

- IPCP: Internet Protocol Control Protocol Options for IPV4. IPCP includes three command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link.

  The sender of this *Configure-Request* may either include its own IP address, to provide this information to its remote peer, or may send all 0.0.0.0 as an IP address, which requests that the remote peer assign an IP address for the local node. The receiver may refuse the requested IP address and attempt to specify one for the peer to use by using a *Configure-NAK* response to the request with a specification of a different address.

  The Ixia implementation provides minimal configuration of this parameter. You must specify the local IP address of the unit and the peer must provide its own IP address. The Ixia port accepts any IP address the peer wishes to use as long as it is a valid address (for example, not all 0's). The Ixia port expects the peer to accept its address. If, however, the peer specifies a different address for use, the port acknowledges that address but not actually notify you that this has happened. The Ixia port accepts a situation in which local and peer addresses are the same following negotiation.

- IPv6CP: Internet Protocol Control Protocol Options for IPv6. IPv6CP includes three command types, which are assigned option numbers in the pertinent RFCs. Note that PPP parameters are typically independently negotiated for each direction on the link.

  A PPP peer may determine its IPv6 interface address by one or three methods:

  - Generate its own address.
  - Suggest its own address to its peer, but allow the peer to override that value.
  - Require that the peer designate an address.

In any of these cases, the *Configure-Request* must contain a tentative interface-identifier to send to the peer that is both unique to the link and if possible consistently reproducible.

The Ixia PPP implementation of IPv6CP is such that the negotiation mode of the local endpoint may be configured in one of three modes:

- Local may: the local peer may suggest an Interface Identifier (IID), but most allow a *Configure-NAK* with an alternate address to override its setting.
- Local must: the local peer must set the IID, which the peer must accept.
- Peer must: the peer must supply the IID. This is accomplished by sending an all zero tentative IID.

The peer endpoint may be configured in one of three modes:

- Peer may: the remote peer may suggest an IID, but most allow a *Configure-NAK* with an alternate address to override its setting.
- Peer must: the remote peer must set the IID, which the local peer accepts.
- Local must: the local peer must supply the IID.

One IID can be sent in each Configuration-Request. A zero value may be sent, in which case, the peer may send an IID in its response. Either node on the link can provide the valid, non-zero IID values for itself and its peer.

The tentative, or assigned IID in the *Peer - Local Must* case, may be assigned from one of four sources:

- Last Negotiated: the last negotiated interface-identifier.
- MAC Based: an address derived from the port's MAC address.
- IPv6: an IPv6 format address.
- Random: a randomly generated value.

See IPv6 Interface Identifiers as follows for more information.

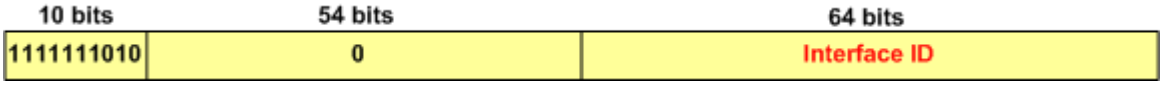
- OSI Network Layer Control Protocol (OSINLCP): A single option is provided for this NCP protocol. If a non-zero value for alignment has been negotiated, subsequent ISO traffic (for example, IS-IS) arrives with or be sent with 1 to 3 zero pads inserted after the protocol header as per RFC 1377.
- MPLS Network Control Protocol (MPLSCP): No options are currently available for this protocol setup.

IPv6 Interface Identifiers (IIDs)

IIDs comprise part of an IPv6 address, as shown in Figure 2-26 on page 2-38 for a link-local IPv6 address.

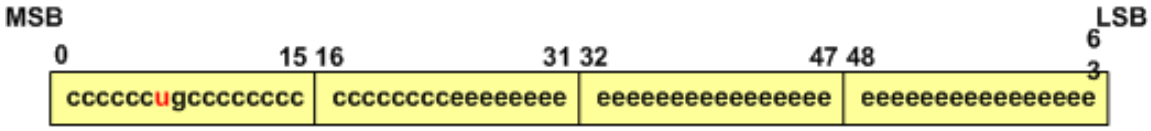
Note: The IPv6 Interface Identifier is equivalent to EUI-64 Id in the Protocol Interfaces window.

Figure 2-26. IPv6 Address Format—Link-Local Address



The IPv6 Interface Identifier is derived from the 48-bit IEEE 802 MAC address or the 64-bit IEEE EUI-64 identifier. The EUI-64 is the extended unique identifier formed from the 24-bit company ID assigned by the IEEE Registration Authority, plus a 40-bit company-assigned extension identifier, as shown in Figure 2-27 on page 2-38

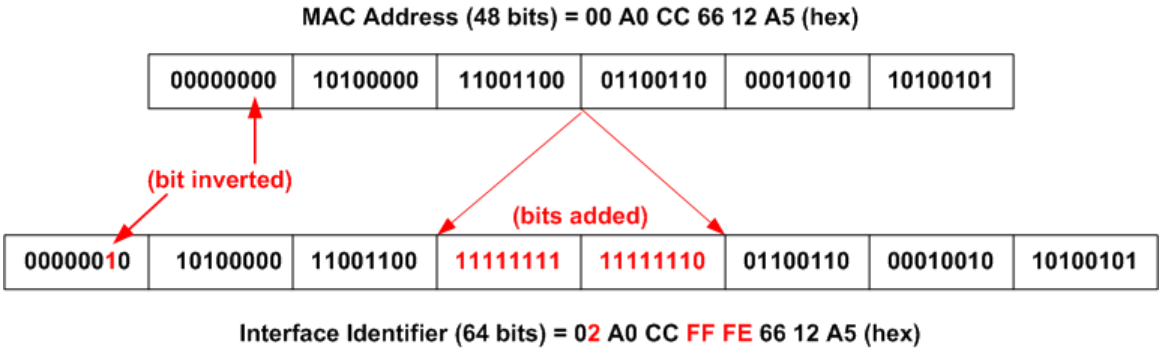
Figure 2-27. IEEE EUI-64 Format



Legend:
c = assigned company ID bits
u = universal/local bit
g = group/individual bit
e = company-assigned extension identifier bit

To create the Modified EUI-64 Interface Identifier, the value of the universal/local bit is inverted from '0' (which indicates global scope in the company ID) to '1' (which indicates global scope in the IPv6 Identifier). For Ethernet, the 48-bit MAC address may be encapsulated to form the IPv6 Identifier. In this case, two bytes 'FF FE' are inserted between the company ID and the vendor-supplied ID, and the universal/local bit is set to '1' to indicate global scope. An example of an Interface Identifier based on a MAC address is shown in Figure 2-28 on page 2-39.

Figure 2-28. Example—Encapsulated MAC in IPv6 Interface Identifier



Retry Parameters

During the process of negotiation, the port uses three Retry parameters. RFC 1661 specifies the interpretation for all of the parameters.

HDLC

Both standard and Cisco proprietary forms of HDLC (High-level Data Link Control) are supported.

Frame Relay

Packets may be wrapped in frame relay headers. The DLCI (Data Link Connection Identifier) may be set to a fixed value or varied algorithmically.

DSCP—Differentiated Services Code Point

Differentiated Services (DiffServ) is a model in which traffic is treated by intermediate systems with relative priorities based on the type of services (ToS) field. Defined in RFC 2474 and RFC 2475, the DiffServ standard supersedes the original specification for defining packet priority described in RFC 791. DiffServ increases the number of definable priority levels by reallocating bits of an IP packet for priority marking.

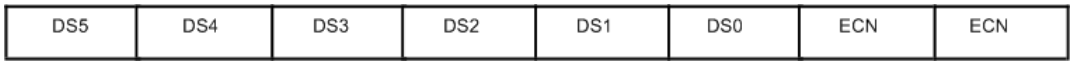
The DiffServ architecture defines the DiffServ (DS) field, which supersedes the ToS field in IPv4 to make Per-Hop Behavior (PHB) decisions about packet classification and traffic conditioning functions, such as metering, marking, shaping, and policing.

Based on DSCP or IP precedence, traffic can be put into a particular service class. Packets within a service class are treated the same way.

The six most significant bits of the DiffServ field are called the Differential Services Code Point (DSCP).

The DiffServ fields in the packet are organized as shown in Figure 2-29 on page 2-40. These fields replace the TOS fields in the IP packet header.

Figure 2-29. DiffServ Fields



The DiffServ standard utilizes the same precedence bits (the most significant bits are DS5, DS4, and DS3) as TOS for priority setting, but further clarifies the definitions, offering finer granularity through the use of the next three bits in the DSCP. DiffServ reorganizes and renames the precedence levels (still defined by the three most significant bits of the DSCP) into these categories (the levels are explained in greater detail in this document). Figure 2-10 on page 2-40 shows the eight categories.

Table 2-10. DSCP Categories

Precedence Level	Description
7	Stays the same (link layer and routing protocol keep alive)
6	Stays the same (used for IP routing protocols)
5	Express Forwarding (EF)
4	Class 4
3	Class 3
2	Class 2
1	Class 1
0	Best Effort

With this system, a device prioritizes traffic by class first. Then it differentiates and prioritizes same-class traffic, taking the drop probability into account.

The DiffServ standard does not specify a precise definition of ‘low,’ ‘medium,’ and ‘high’ drop probability. Not all devices recognize the DiffServ (DS2 and DS1) settings; and even when these settings are recognized, they do not necessarily trigger the same PHB forwarding action at each network node. Each node implements its own response based on how it is configured.

Assured Forwarding (AF) PHB group is a means for a provider DS domain to offer different levels of forwarding assurances for IP packets received from a customer DS domain. Four AF classes are defined, where each AF class is in each DS node allocated a certain amount of forwarding resources (buffer space and bandwidth).

Classes 1 to 4 are referred to as AF classes. The following table illustrates the DSCP coding for specifying the AF class with the probability. Bits DS5, DS4,

and DS3 define the class, while bits DS2 and DS1 specify the drop probability. Bit DS0 is always zero.

Table 2-11. Drop Precedence for Classes

Drop	Class 1	Class 2	Class 3	Class 4
Low	001010 AF11 DSCP 10	010010 AF21 DSCP 18	011010 AF31 DSCP 26	100010 AF41 DSCP 34
Medium	001100 AF12 DSCP 12	010100 AF 22 DSCP 20	011100 AF32 DSCP 28	100100 AF42 DSCP 36
High	001110 AF13 DSCP 14	010110 AF23 DSCP 22	011110 AF33 DSCP 30	100110 AF43 DSCP 38

ATM

The ATM load module enables high performance testing of routers and broadband aggregation devices such as DSLAMs and PPPoE termination systems.

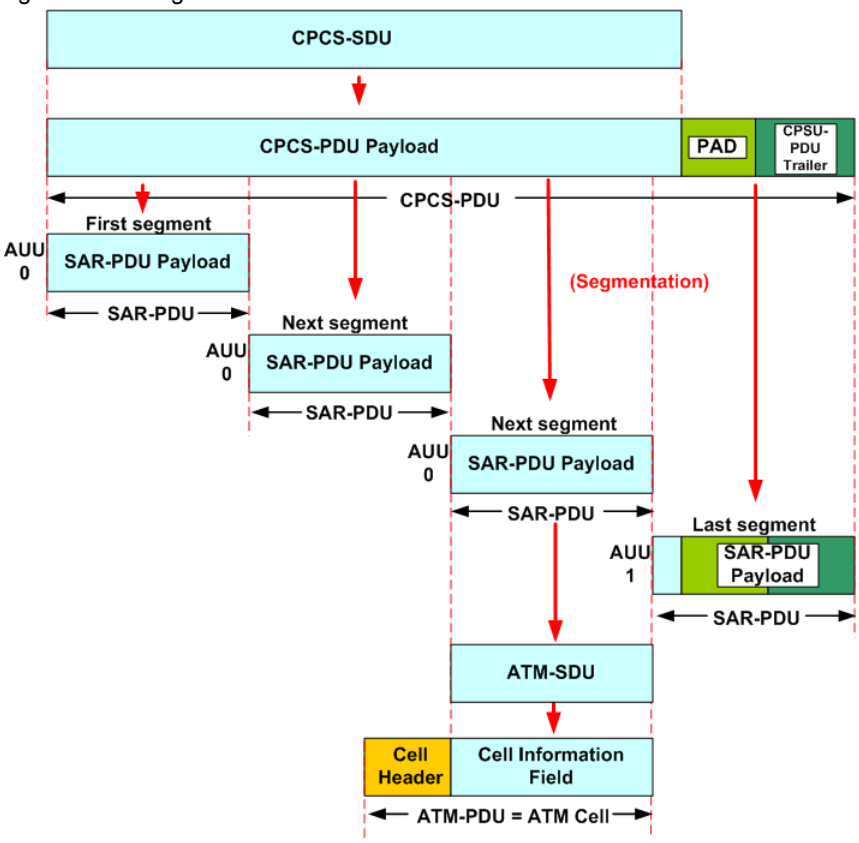
The ATM module is provided with various feature combinations:

- Interfaces: pluggable PHYs:
  - 1310nm multimode optics with dual -SC connectors
  - SFP socket
- Speeds: OC3 and OC12
- Encapsulations:
  - LLC/SNAP
  - LLC/NLPID
  - LLC Bridged Ethernet
  - LLC Bridged Ethernet without FCS
  - VC Mux Routed
  - VC Mux Bridged Ethernet
  - VC Mux Bridged Ethernet without FCS
- Multiple independent data streams

ATM is a point-to-point, connection-oriented protocol that carries traffic over ‘virtual connections/circuits’ (VCs), in contrast to Ethernet connectionless LAN traffic. ATM traffic is segmented into 53-byte cells (with a 48-byte payload), and allows traffic from different Virtual Circuits to be interleaved (multiplexed). Ixia’s ATM module allows up to 4096 transmit streams per port, shared across up to 15 interleaved VCs.

To allow the use of a larger, more convenient payload size, such as that for Ethernet frames, ATM Adaptation Layer 5 (AAL5) was developed. It is defined in ITU-T Recommendation I.363.5, and applies to the Broadband Integrated Services Digital Network (B-ISDN). It maps the ATM layer to higher layers. The Common Part Convergence Sublayer-Service Data Unit (CPSU-SDU) described in this document can be considered an IP or Ethernet packet. The entire CPSU-PDU (CPCS-SDU plus PAD and trailer) is segmented into sections which are sent as the payload of ATM cells, as shown in Figure 2-30 on page 2-42, based on ITU-T I.363.5.

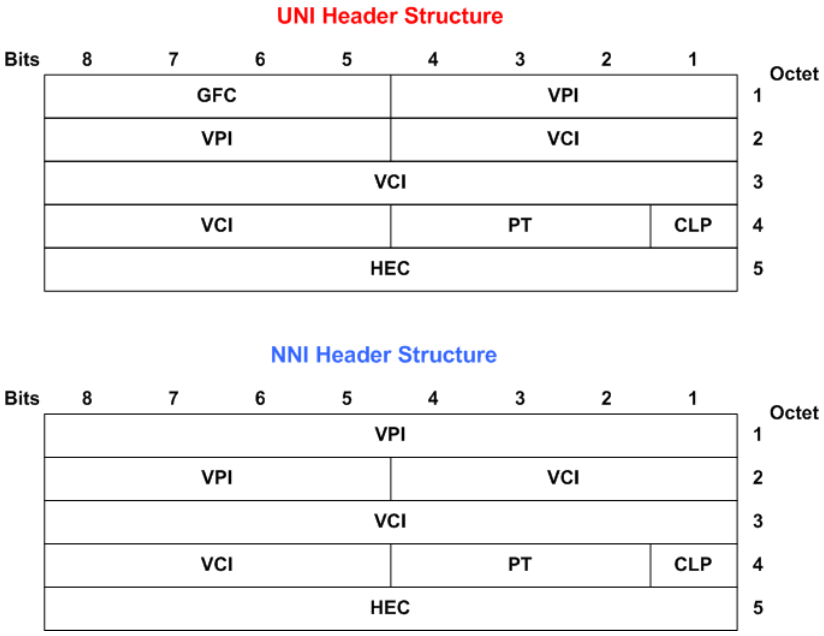
Figure 2-30. Segmentation into ATM Cells



The Interface Type can be set to UNI (User-to-Network Interface) format or NNI (Network-to-Node Interface aka Network-to-Network Interface) format. The 5-

byte ATM cell header is different for each of the two interfaces, as shown in Figure 2-31 on page 2-43.

Figure 2-31. ATM Cell Header for UNI and NNI

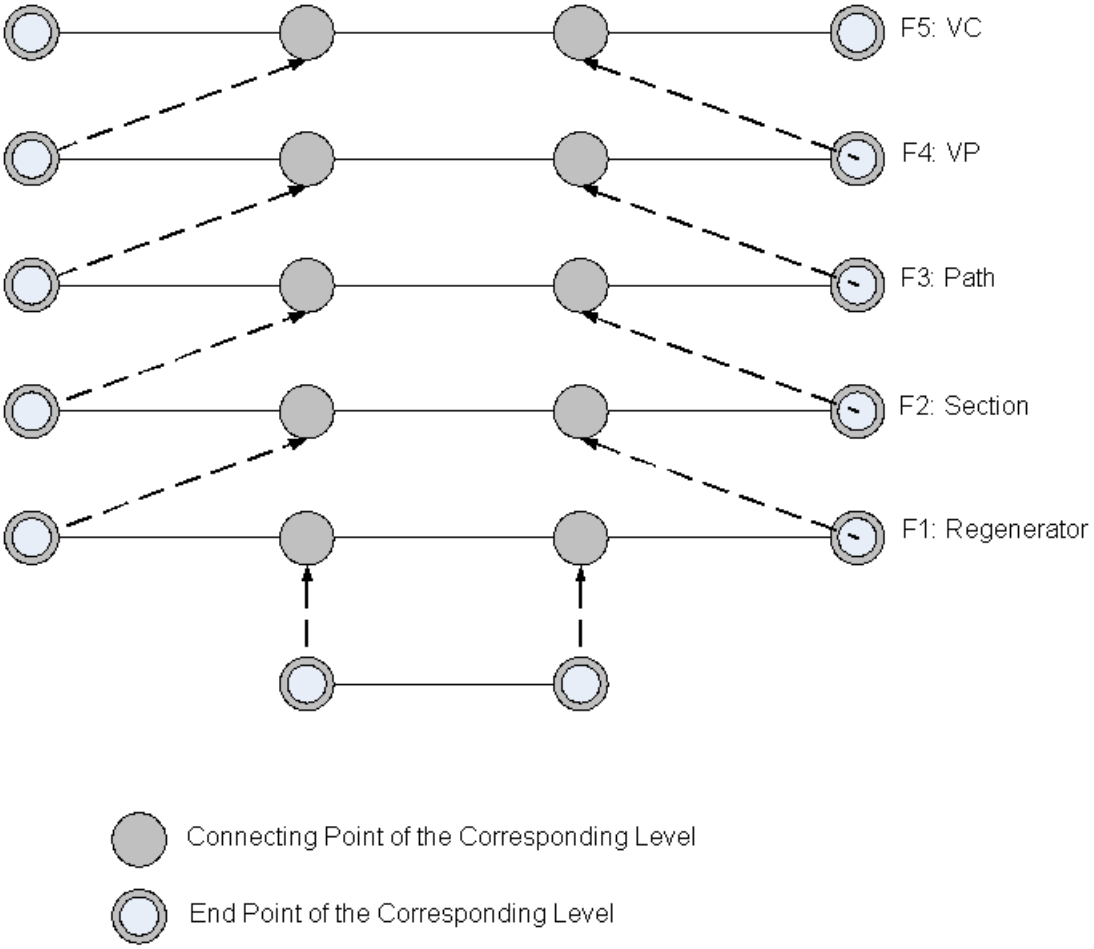


ATM OAM Cells

OAM cells are used for operation, administration, and maintenance of ATM networks. They operate on ATM's physical layer and are not recognized by higher layers. Operation, Administration, and Maintenance (OAM) performs standard loopback (end-to-end or segment) and fault detection and notification Alarm Indication Signal (AIS) and Remote Defect Identification (RDI) for each connection. It also maintains a group of timers for the OAM functions. When there is an OAM state change such as loopback failure, OAM software notifies the connection management software.

The ITU-T considers an ATM network to consist of five flow levels. These levels are illustrated in Figure 2-32 on page 2-44.

Figure 2-32. Maintenance Levels



The lower three flow levels are specific to the nature of the physical connection. The ITU-T recommendation briefly describes the relationship between the physical layer OAM capabilities and the ATM layer OAM.

From an ATM viewpoint, the most important flows are known as the F4 and F5 flows. The F4 flow is at the virtual path (VP) level. The F5 flow is at the virtual channel (VC) level. When OAM is enabled on an F4 or F5 flow, special OAM cells are inserted into the user traffic.

Four types of OAM cells are defined to support the management of VP/VC connections:

- Fault Management OAM cells. These OAM cells are used to indicate failure conditions. They can be used to indicate a discontinuity in VP/VC connection or may be used to perform checks on connections to isolate problems.
- Performance Management OAM cells. These cells are used to monitor performance (QoS) parameters such as cell block ratio, cell loss ratio and incorrectly inserted cells on VP/VC connections.

- Activation-deactivation OAM cells. These OAM cells are used to activate and deactivate the generation and processing of OAM cells, specifically continuity check (CC) and performance management (PM) cells.
- System management OAM cells. These OAM cells can be used to maintain and control various functions between end-user equipment.Their content is not specified by I.610, and they are limited to end-to-end flows.

The general format of an OAM cell is shown in Figure 2-33 on page 2-45.

Figure 2-33. OAM Cell Format

The header indicates which VCC or VPC an OAM cell belongs to. The cell payload is divided into five fields. The OAM-type and Function-type fields are used to distinguish the type of OAM cell. The Function Specific field contains information pertinent to that cell type. A 10 bit Cyclic Redundancy Check (CRC) is at the end of all OAM cells. This error detection code is used to ensure that management systems do not make erroneous decisions based on corrupted OAM cell information.

Ixia ATM modules allows to configure Fault Management and Activation/Deactivation OAM Cells.

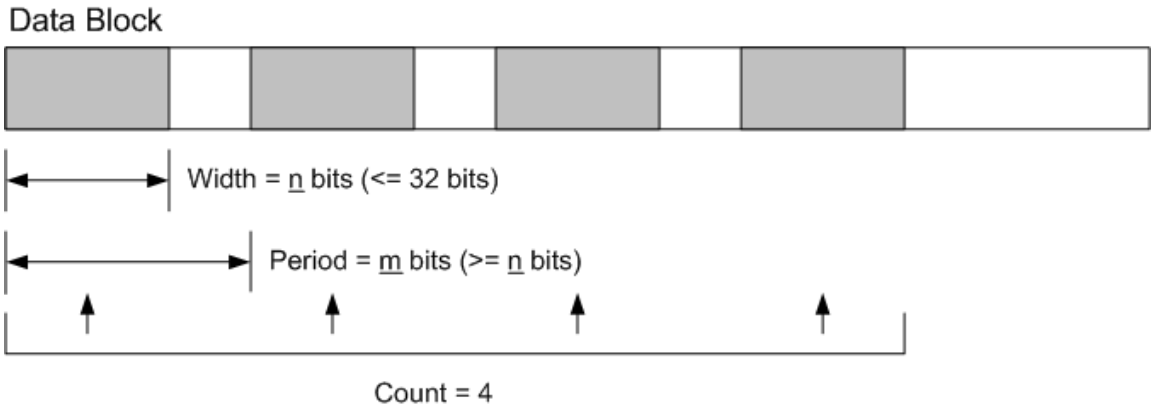
BERT

Bit Error Rate Test (BERT) load modules are packaged as both an option to OC48, POS, and 10GE load modules and as BERT-only load modules. As opposed to all other types of testing performed by Ixia hardware and software, BERT tests operate at the physical layer, also referred to as OSI Layer 1. POS frames are constructed using specific pseudo-random patterns, with or without inserted errors. The receive circuitry locks on to the received pattern and checks for errors in those patterns.

Both unframed and framed BERT testing is available. Framed testing can be performed in both concatenated and channelized modes with some load modules.

The patterns inserted within the POS frames are based on the ITU-T O.151 specification. They consist of repeatable, pseudo-random data patterns of different bit-lengths which are designed to test error and jitter conditions. Other constant and user-defined patterns may also be applied. Furthermore, you may control the addition of deliberate errors to the data pattern. The inserted errors are limited to 32-bits in length and may be interspersed with non-errored patterns and repeated for a count. This is illustrated in Figure 2-34 on page 2-46. In the figure, an error pattern of *n* bits occurs every *m* bits for a count of 4. This error is inserted at the beginning of each POS data block within a frame.

Figure 2-34. BERT Inserted Error Pattern

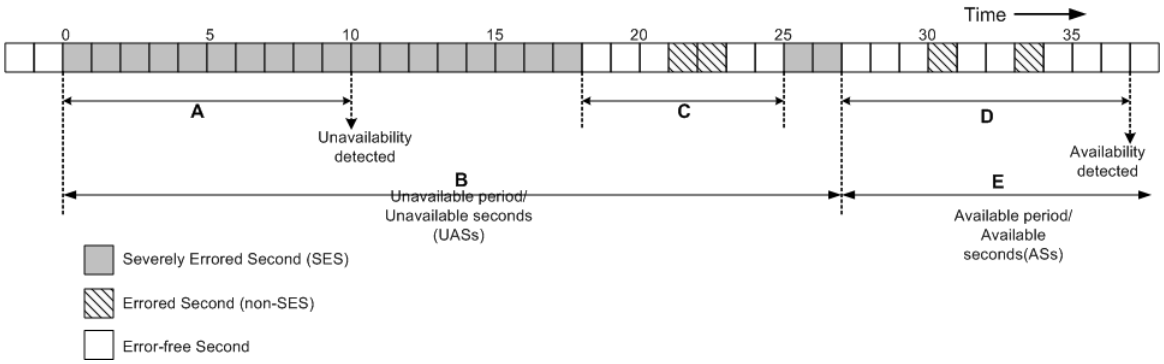


Errors in received BERT traffic are visible through the measured statistics, which are based on readings at one-second intervals. The statistics related to BERT are described in the *Available Statistics* appendix associated with the *Ixia Hardware Guide* and some other manuals.

Available/Unavailable Seconds

Reception of POS signals can be divided into two types of periods, depending on the current state—'Available' or 'Unavailable,'—as shown in Figure 2-35 on page 2-46. The seconds occurring during an unavailable period are termed Unavailable Seconds (UAS); those occurring during an available period are termed Available Seconds (AS).

Figure 2-35. BERT—Unavailable/Available Periods



These periods are defined by the error condition of the data stream. When 10 consecutive SESs (A in the figure) are received, the receiving interface triggers an Unavailable Period. The period remains in the Unavailable state (B in the figure), until a string of 10 consecutive non-SESs is received (D in the figure), and the beginning of the Available state is triggered. The string of consecutive non-SESs in C in the figure was less than 10 seconds, which was insufficient to trigger a change to the Available state.

Port Transmit Capabilities

The Ixia module ports format data to be transmitted in a hierarchy of structures:

- *Streams and Flows*—A set of related packet bursts
  - *Bursts and the Inter-Burst Gap (IBG)*—A repetition of packets
    - *Packets and the Inter-Packet Gap (IPG)*—Individual packets/ frames

Timing of transmitted data is performed by the use of inter-stream, -burst, and -packet gaps. Ethernet modules use all three types of gaps, programmed to the resolution of their internal clocks. POS modules gaps are implemented by use of empty frames and the resolution of the gap is limited to a multiple of such frames. ATM modules do not use inter-stream or inter-packet gaps, and instead control the transmission rate through empty frames. The three types of gaps are discussed in:

- *Streams and the Inter-Stream Gap (ISG) on page 2-50*
- *Bursts and the Inter-Burst Gap (IBG) on page 2-50*
- *Packets and the Inter-Packet Gap (IPG) on page 2-51*

The percentage of line rate usage for ports is determined using the following formula:

```
(packet size + 12 byte IPG + requested preamble)/
(packet size + requested IPG + requested preamble) * 100
```

Streams and Flows

The Ixia system uses sophisticated models for the programming of data to be transmitted. There are two general modes of scheduling data packets for transmission:

- Sequential: The first configured stream in a set of streams is transmitted completely before the next one is sent, and so on, until all of the configured streams have been transmitted. Two types are available:
  - *Packet Streams*
  - *Packet Flows* (available on certain modules)
- Interleaved: The individual packets in the streams are multiplexed into a single stream, such that the total packet rate is the sum of the packet rates for each of the streams. One type is available:
  - *Advanced Streams* (Advanced Stream Scheduler feature)

ATM modules support up to 15 independent stream queues, each of which may contain multiple streams. Up to 4096 total streams may be defined. See *Stream Queues* on page 2-49.

Packet Streams

This sequential transmission model is supported by the Ixia load modules, where dedicated hardware can be used to generate up to 255 *Packet Streams* ‘on-the-

fly,' with each stream consisting of up to 16 million bursts of up to 16 million packets each. Transmission of the entire set of packet streams may be repeated continuously for an indefinite period, or repeated only for a user-specified count. The variability of the data within the packets is necessarily generated algorithmically by the hardware transmit engine.

Note: Streams consisting of only one packet are not transmited at wire speed. Also, streams set to random frame size generation does not have accurate IP checksum information. See the *IxExplorer Users Guide*, Chapter 4, *Stream and Flow Control*, for more information on creating streams.

Packet Flows

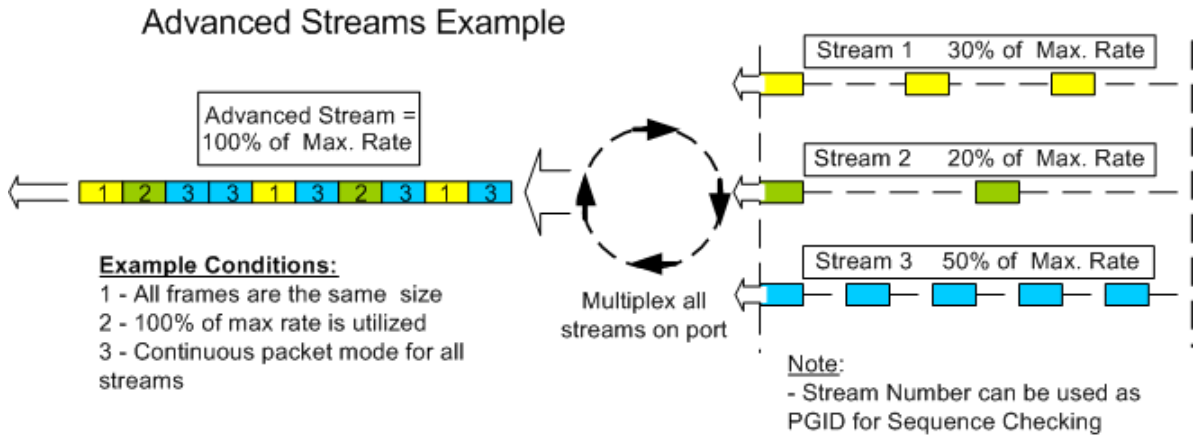
A second sequential data transmission model is supported by software for any Ixia port which supports *Packet Flows*. An individual packet flow can consist of from 1 to 15,872 packets. For packet flows consisting of only one unique packet each, a maximum of 15,872 individual flows can be transmitted. Because the packets in each of the packet flows is created by the software, including *User Defined Fields (UDF)* and checksums, and then stored in memory in advance of data transmission, there can be more unique types of packets than is possible with streams. Continuous transmission cannot be selected for flows, but by using a return loop, the flows can be retransmitted for a user-defined count.

Packet streams, which can contain larger amounts of data, are based on only one packet configuration per stream. In contrast, many packet flows can be configured for a single data transmission, where each flow consists of packets with a configuration unique to that flow. Some load modules permit saving/loading of packet flows.

Advanced Streams

A third type of stream configuration is called *Advanced Streams,* which involves interleaving of all defined streams for a port into a single, multiplexed stream. Each stream is assigned a percentage of the maximum rate. The frames of the streams are multiplexed so that each stream's long-term percentage of the total transmitted data rate is as assigned. When the sum of all of the streams is less than 100% of the data rate, idle bytes are automatically inserted into the multiplexed stream, as appropriate.

Figure 2-36. Example of Advanced Stream Generation



Stream Queues

Stream queues allow standard packet streams to be grouped together. Up to 15 stream queues may be defined, each containing any number of streams so long as the total number of streams in all queues for a port does not exceed 4,096. Each queue is assigned a percentage of the total and traffic is mixed as in advanced streams. Each queue may represent any number of VPI/VCI pairs; the VPI/VCI pairs may also be generated algorithmically.

Basic Stream Operation

When multiple transmit modes are available, the *transmit mode* for each port must be set by you to indicate whether it uses streams, flows, or advanced stream scheduling. The programming of sequential streams or flows is according to the same programming model, with a few exceptions related to continuous bursts of packets. Since the model is identical in both cases, we refer to both streams and flows as ‘streams’ while discussing programming.

There are three basic types of sequential streams:

- Continuous Packet: A continuous stream of packets. The packets are not necessarily identical; their contents may vary significantly. (Not available for packet flows.)
- Continuous Burst: A set of counted packets within a burst; the burst is repeated continuously. (Not available for packet flows.)
- Counted Burst (non-continuous): A user-specified number of bursts per stream, where each burst contains a counted number of packets.

Each non-continuous stream is related to the next stream by one of four modes:

- Stop after this stream: Data transmission stops after the completion of the current stream. (For example, after transmission of a stream consisting of 10 bursts of 100 packets each.)

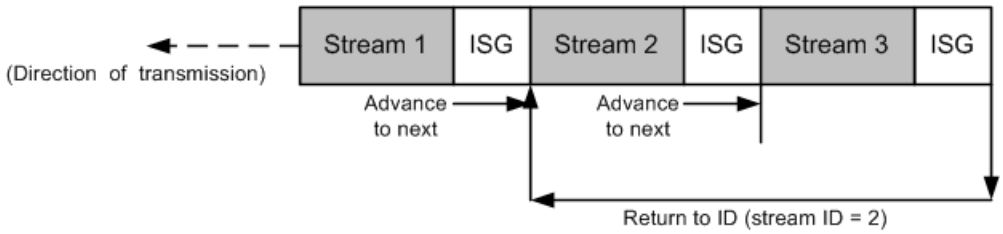
- Advance to Next: Data transmission continues on to the next stream after the completion of the current stream.
- Return to ID: After the completion of the current stream, a previous stream (designated by its Stream ID) is retransmitted once, and then transmission stops.
- Return to ID for Count: After the completion of the current stream, a previous stream (designated by its Stream ID) is retransmitted for the user-specified number of times (count), and then transmission stops.

If a Continuous Packet or Continuous Burst stream is used, it becomes the last stream to be applied and data transmission continues until a Stop Transmit operation is performed.

Streams and the Inter-Stream Gap (ISG)

A programmable Inter-Stream Gap (ISG) can be applied after each stream, as pictured in Figure 2-37 on page 2-50.

Figure 2-37. Inter-Stream Gap (ISG)

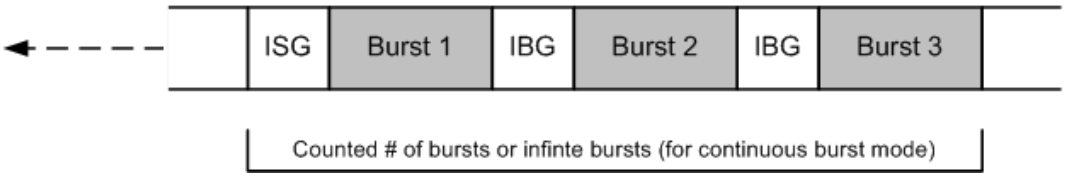


The size and resolution of the Inter-Stream Gaps depends on the particular Ixia module in use. For all modules except 10 Gigabit Ethernet modules, the stream uses the parameters set in the following stream. In 10 Gigabit Ethernet modules, it uses the parameters set in the preceding stream. There are no ISGs before Advanced Scheduler Streams. For non-Ethernet modules, the ISG is implemented by use of empty frames and the resolution of the ISG is limited to a multiple of such frames.

Bursts and the Inter-Burst Gap (IBG)

Bursts are sets of a specified number of packets, separated by programmed gaps between the sets. For Ethernet modules, Inter-Burst Gaps (IBG) are inserted between the sets. For POS modules, bursts of packets are separated by Burst Gaps. ATM modules do not insert IBGs. The size and resolution of these gaps depends on the type of Ixia load module in use. The placement of Inter-Burst Gaps is shown in Figure 2-38 on page 2-51.

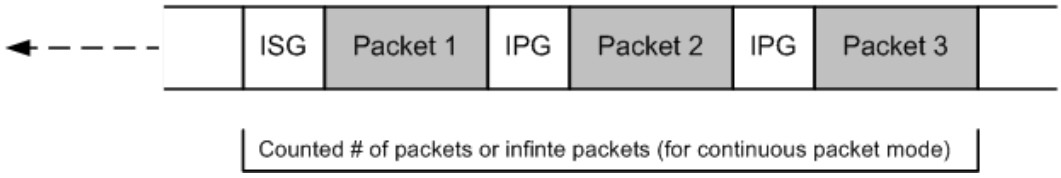
Figure 2-38. Inter-Burst Gap (IBG)/Burst Gap



Packets and the Inter-Packet Gap (IPG)

Streams may contain a counted number of frames, or a continuous set of frames when Continuous Packet mode is used. Frames are separated by programmable Inter-Packet Gaps (IPGs), sometimes referred to as Inter-Frame Gaps (IFGs). The size and resolution of the Inter-Packet Gaps depends on the particular Ixia module in use. For non-Ethernet modules, the ISG is implemented by use of empty frames and the resolution of the IPG is limited to a multiple of such frames. ATM modules do not insert IBGs.The placement of Inter-Packet Gaps is shown in Figure 2-39 on page 2-51.

Figure 2-39. Inter-Packet Gap (IPG)



Frame Data

The contents of every frame and packet are programmable in terms of structure and data content. The programmable fields are:

- Preamble or Header contents
  - Ethernet modules: Preamble Size: The size and resolution depends on the particular Ixia load module used.
  - POS modules: Minimum Flag and Header contents: The minimum number of flag fields to precede the packet within the POS frame and the type of encapsulation/signalling.
  - ATM modules: Header contents.
- Frame size: The size and resolution depends on the particular Ixia load module used.
- Destination and Source MAC Addresses (Ethernet only): Allows the MAC addresses to be set to constants, vary randomly, or increment/decrement using a mask.

- Data generators: Five different data generators are available. These generators are listed as follows, in order of increasing priority (from top to bottom). The values from generators located lower in this list override data from those higher in the list.
  - Protocol-related data: Formatted to correspond to particular data link, transport, and protocol conventions.
    - Data link layer controls for Ethernet allow for Ethernet II/SNAP, 802.3 Raw and 802.3 IPX formatting, with support for VLANs, MPLS, and Cisco-proprietary ISL. VLANs are described in *Virtual LANs* on page 2-52
    - Protocol-specific data for formatting IPv4, IPv6, and IPX packets (such as Source and Destination IP addresses), as well as Layer 4 transport protocol headers (TCP/IP, IGMP, and so on) are also supported. IPv4/IPv6 and IPv6/IPv4 tunneling is also supported.
    - IP Source and Destination addresses may be incremented or decremented using a network mask.
  - Data Patterns: Can be one of three types: predefined patterns up to 8K bytes in length, randomly generated data, algorithmically generated data, industry standard (such as CJPAT and CRPAT) or user-specified.
  - User Defined Fields (UDFs): A number of 32-bit counters. For some modules the counters can each be flexibly configured as multiple 8, 16, 24, and 32-bit counters. Each counter may independently increment or decrement using a mask. These are further described in *User Defined Fields (UDF)* on page 2-55.
  - Frame Identity Record (FIR): An identity record stored at the end of the packet. The information is very useful for determining the source of transmitted data found in capture buffers.
  - Frame Check Sequence (FCS): The checksum for a packet may be omitted, formatted correctly, or have deliberate errors inserted. Deliberate errors include incorrect checksum, dribble errors, and alignment errors.

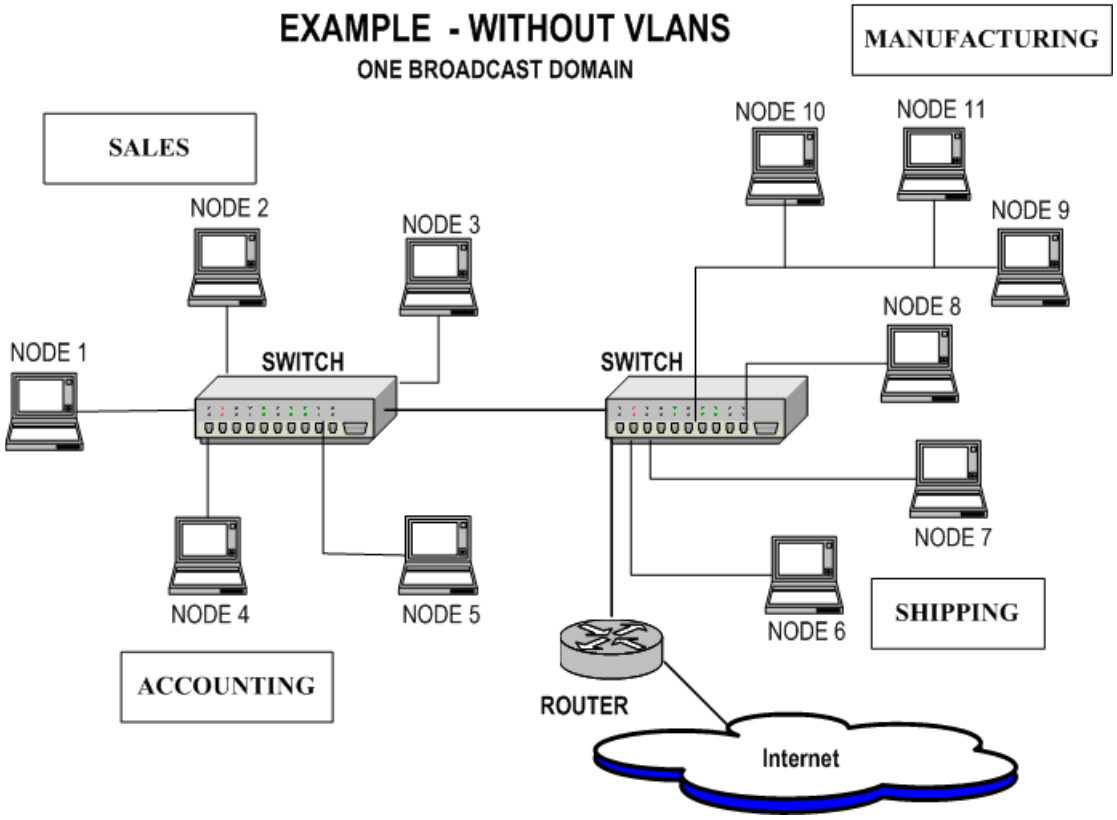
Virtual LANs

Virtual LANs (VLANs) are defined in IEEE 802.1Q, and can be used to create subdomains without the use of IP subnets. The IEEE 802.1Q specification uses the explicit VLAN tagging method and port-based VLAN membership. Explicit tagging involves the insertion of a tag header in the frame by the first switch that the frame encounters. This tag header indicates which VLAN the packet belongs to. A frame can belong to only one VLAN.

VLAN tag headers are inserted into the frames, following the source MAC address. A maximum of 4094 VLANs can be supported, based on the length of the 12-bit VLAN ID. The VID value is used to map the frame into a specific VLAN. VLAN IDs 0 and FFF are reserved. VID = 0 indicates the null VLAN ID, which means that the tag header contains only user priority information.

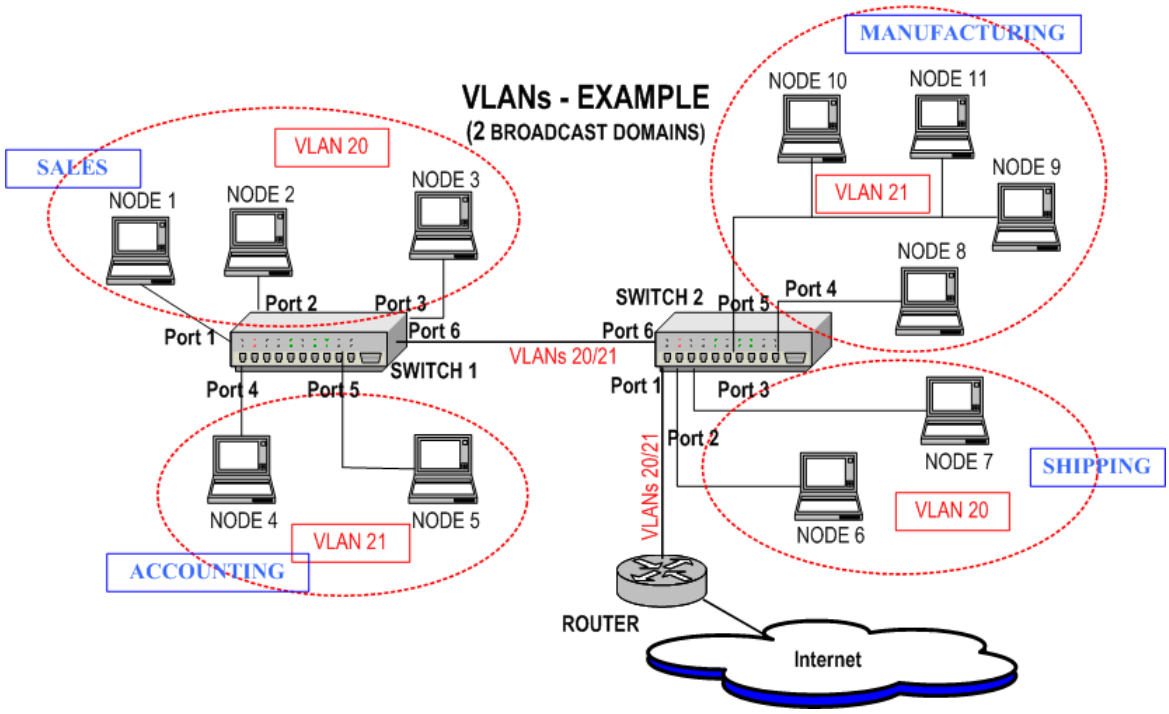
An example of Layer 2 broadcast domain without VLANs is shown in Figure 2-40 on page 2-53.

Figure 2-40. Example of Broadcast Domain Without VLANs



In the example above, a company has four departments (Sales, and so forth) which are in one switched broadcast domain. Broadcasts are flooded to all of the devices in the domain. A router sends/receives Internet traffic. In Figure 2-41 on page 2-54, the departments have been grouped into two separate VLANs, cutting down on the amount of broadcast traffic. For example, VLAN 20 contains Ports 1, 2, 3, and 6 on Switch 1, and Ports 1, 2, 3, and 6 on Switch 2. VLAN 21 contains Ports 4, 5, and 6 on Switch 1, and Ports 1, 4, 5, and 6 on Switch 2.

Figure 2-41. Example of VLANs



With the new network design, switch ports and attached nodes are assigned to VLANs. Frames are tagged with their VLAN ID as they leave the switch, en route to the second switch. The VLAN ID indicates to the second switch which ports to send the frame to. The VLAN tag is removed as the frame exits a port belonging to that VLAN, on its way to the attached node. With VLANs, bandwidth is conserved, and security is improved. Communication between the VLANs is handled by the existing Layer 3 router.

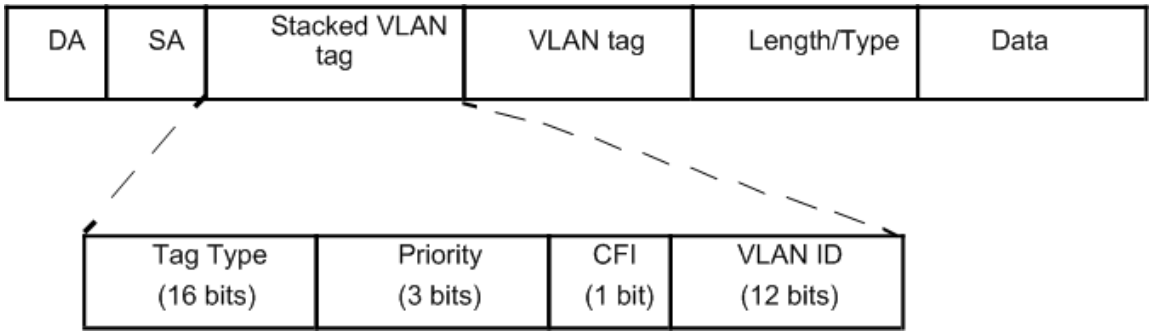
Stacked VLANs (Q in Q)

VLAN Stacking refers to a mechanism where one VLAN (Virtual Local Area Network) may be encapsulated within another VLAN. This allows a carrier to partition the network among several networks, while allowing each network to still utilize VLANs to their full extent. Without VLAN stacking, if one network provisioned an end user into ‘VLAN 1,’ and another network provisioned one of their end users into ‘VLAN 1,’ the two end users would be able to see each other on the network.

VLAN stacking solves this problem by embedding each instance of the 802.1Q VLAN protocol into a second tier of VLANs. The first network is assigned a ‘Backbone VLAN,’ and within that Backbone VLAN a unique instance of 802.1Q VLAN tags may be used to provide that network with up to 4096 VLAN identifiers. The second network is assigned a different Backbone VLAN, within which another unique instance of 802.1Q VLAN tags is available.

Figure 2-42 on page 2-55 demonstrates an example packet of a stacked VLAN.

Figure 2-42. Stacked VLAN Header Information



User Defined Fields (UDF)

Seven different types of UDFs are available, depending on the load module type. The types of UDFs that are supported by particular port types is detailed in Chapter 1, *Platform and Reference Overview*. Not all features supported by a port type are available on all UDFs; whether a particular UDF type is supported on a particular UDF can be ascertained by looking at the UDF with IxExplorer or programatically using the Tcl API. These types are:

- *Counter Mode UDF*
- *Random Mode UDF*
- *Value List Mode UDF*
- *Range List Mode UDF*
- *Nested Counter Mode UDF*
- *IPv4 Mode UDF*
- *Table Mode UDF*

Some features are common across all UDFs:

- Counter Type: The size of the counter is available in two modes:
  - A single counter with a length of 8, 16, 24 or 32 bits, or
  - A 32-bit value that may be divided into one to four 8 to 32 bit counters in any order. For example, 8x8x8x8 (four 8-bit counters), 8x16 (an 8-bit counter followed by a 16 bit counter), or 24x8 (a 24-bit counter followed by an 8-bit counter). In this case, each of the up to four counters may be independently controlled as described in *Counter Mode UDF*.
- Offset: The offset from the beginning of the packet to the start of the counter.
- Init val: The initial value given to the counter.
- Cascade: Sets the initial value for the counter, in one of two ways:
  - From the last value for this stream: The counter continues from the last value generated by this UDF for this stream. The first value for

the counter is set from the *Init val* setting. This type of cascade is sometimes referred to as *Cascade From Self*.

- From the last value on the previous cascade stream: The counter continues from the last value generated by the last executed stream using this UDF that is also in this cascade mode. The first value for the first UDF is set from the *Init val* setting. This type of cascade is sometimes referred to as *Cascade From Previous Stream*.

- Masking: The bit masking operation allows certain bits to maintain constant values, while varying other values. In the IxExplorer GUI, a bit mask is represented as a string of characters, one character per counter bit. For example, a possible *Bit Mask* setting for an 8-bit counter might be:

  ```
  0110XXXX
  ```

  The '0's and '1's represent fixed values after the mask value, while the 'X's are bits which vary as a result of the increment, decrement or random value option.

  In the TCL/C++ APIs, the *Bit Mask* value is split into two variables:

  - *maskSelect*: Indicates which bits of the counter are fixed in value, and
  - *maskval*: Indicates the fixed value for any of the bits set in *maskSelect*.

In all of the UDF figures, the generated counter value is shaded. The parameters are shown in ovals (blue in the online version).

Counter Mode UDF

The counter mode UDF features the ability of a counter (up to four on some load modules) to count up or down or to use random values. Certain bits of the counter may be held at fixed values using a mask. The parameters that affect the counter's operation are shown in Table 2-12 on page 2-56.

Table 2-12. Counter Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Counter Type	countertype
Offset	offset
Init Value	initval
Set from Init Value Continue from last value for this stream Cascade continue	cascadeType enableCascade
Random*	random
Continuously Counting	continuousCount
Step	step
Repeat Count	repeat

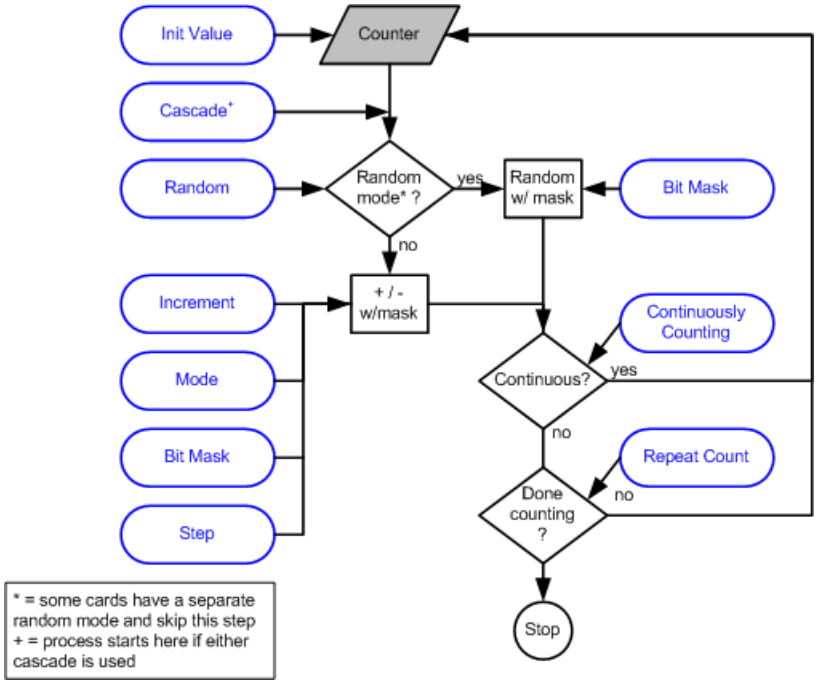
Table 2-12. Counter Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Mode	updown
Bit Mask	maskval maskselect

* some card types include random mode as part of the counter mode and others use them as a separate mode.

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfCounterMode (0)*. The operation of counter mode is described in the flowchart shown in Figure 2-43 on page 2-57.

Figure 2-43. UDF Counter Mode Operation



Random Mode UDF

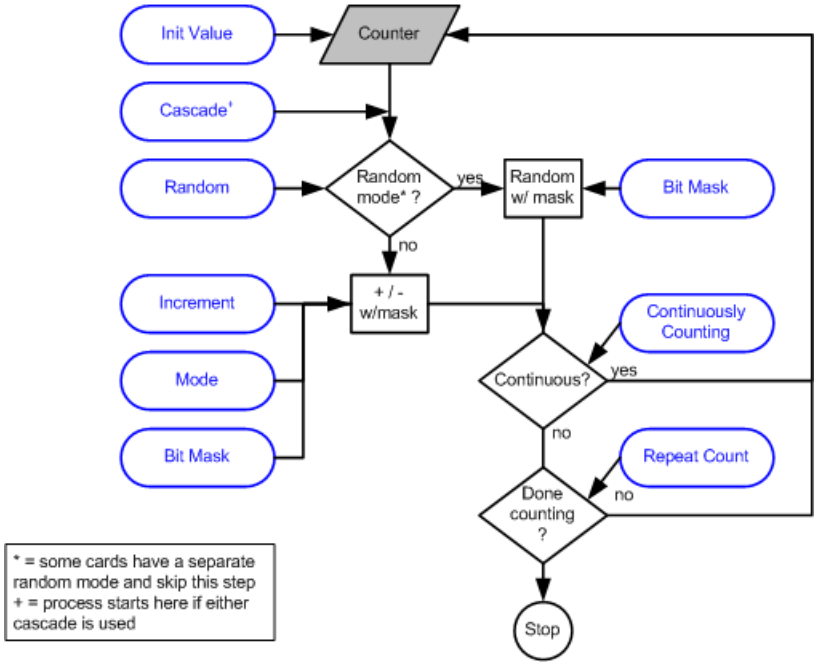
The random mode UDF features a counter whose values are randomly generated, but may be masked. Cascading modes do not apply to random mode UDFs. The parameters that affect the counter's operation are shown in Table 2-13 on page 2-57.

Table 2-13. Random Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Offset	offset
Bit Mask	maskval maskselect

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfRandomMode (1)*. The operation of random mode is described in the flowchart shown in Figure 2-44 on page 2-58.

Figure 2-44. UDF Random Mode Operation



Value List Mode UDF

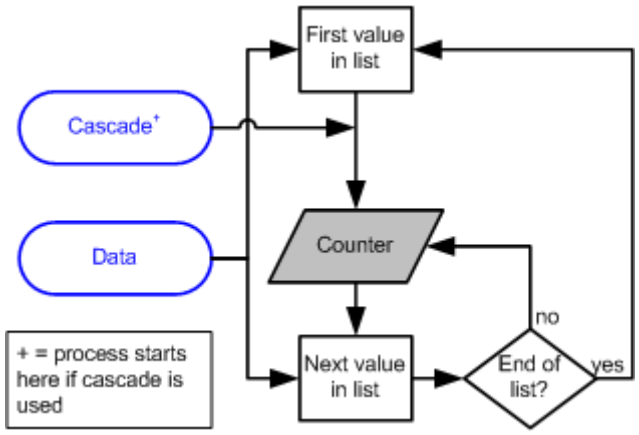
The value list mode UDF features a counter whose values successively retrieved from a table of values. Cascading modes do not apply to value list mode UDFs. The parameters that affect the counter's operation are shown in Table 2-14 on page 2-58.

Table 2-14. Value List Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Data	valueList
Set from Init Value Continue from last value for this stream	cascadeType enableCascade

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfValueListMode (2)*. The operation of value list mode is described in the flowchart shown in Figure 2-45 on page 2-59.

Figure 2-45. UDF Value List Mode Operation



Range List Mode UDF

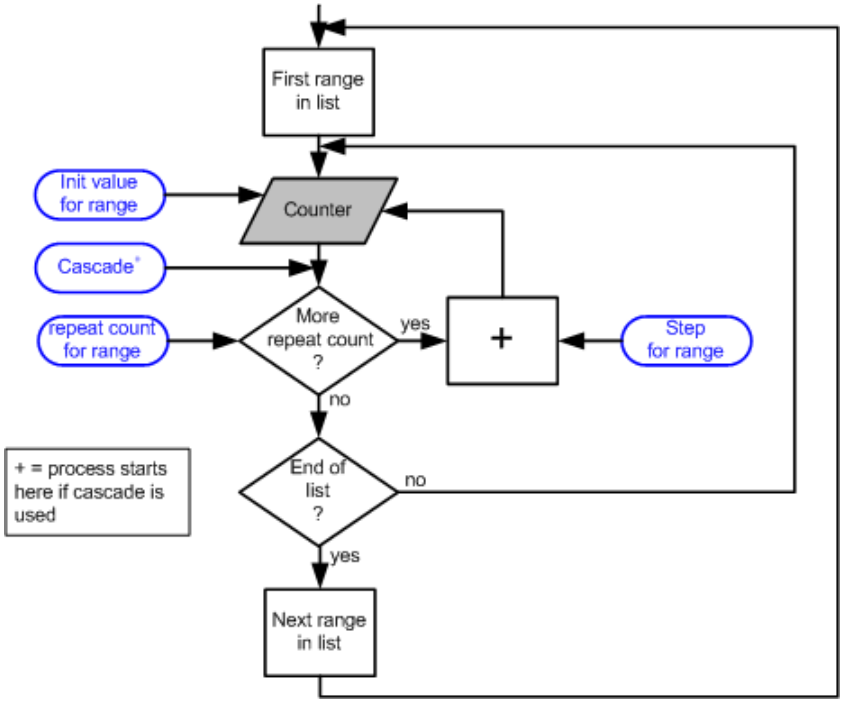
The range list mode UDF features a counter whose values are generated from a list of value ranges. Each range has an initial value, repeat count, and step value. Cascading modes do not apply to range list mode UDFs. The parameters that affect the counter's operation are shown in Table 2-15 on page 2-59.

Table 2-15. Range List Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Repeat Count	repeat
Step	step
Set from Init Value Continue from last value for this stream	cascadeType enableCascade

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfRangeListMode (4).* The *initval*, *repeat,* and *step* values are added into the *udf* command by the *addRange* sub-command. The operation of range list mode is described in the flowchart shown in Figure 2-46 on page 2-60.

Figure 2-46. UDF Range List Mode Operation



Nested Counter Mode UDF

The nested counter mode UDF features a counter whose values are generated from three nested loops:

1. A given value may be repeated a number of times.
2. That value is incremented and step 1 is repeated for a count. This is called the *inner loop*.
3. That value is incremented and steps 1 and 2 repeated continuously for a count. This is called the *outer loop*.

The parameters that affect the nested counter's operation are shown in Table 2-16 on page 2-60.

Table 2-16. Nested Counter Mode UDF Parameters

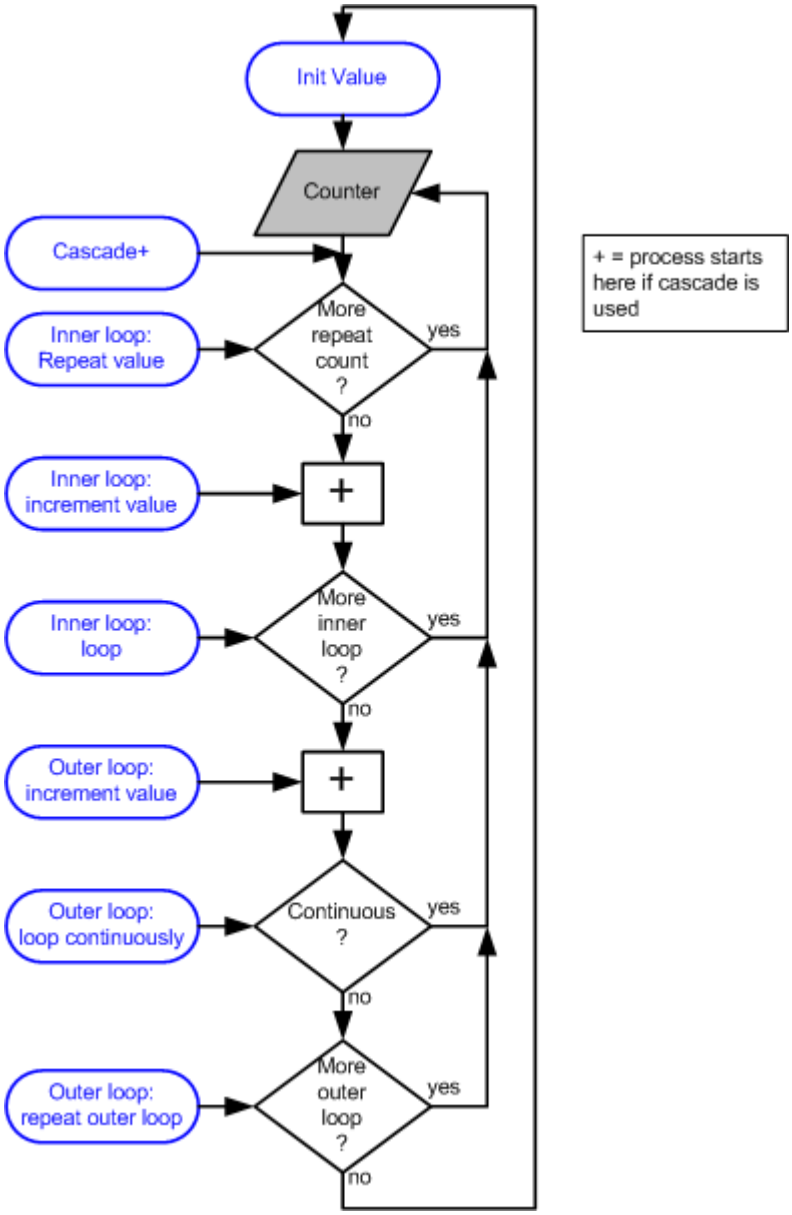
IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Inner Loop: Repeat value	innerRepeat
Inner Loop: increment value	innerStep
Inner Loop: loop	innerLoop
Outer Loop:increment value	step

Table 2-16. Nested Counter Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Outer Loop: loop continuously	continuousCount
Outer Loop: repeat outer loop	repeat
Set from Init Value Continue from last value for this stream	cascadeType enableCascade

In the TCL APIs the value of the *counterMode* variable in the *udf* command should be set to *udfNestedCouterMode (3)*. The operation of range list mode is described in the flowchart shown in Figure 2-46 on page 2-60.

Figure 2-47. UDF Nested Counter Mode Operation



IPv4 Mode UDF

The IPv4 counter mode UDF features a counter designed to be used with IPv4 addresses. The process is:

1. A given value may be repeated a number of times. Values with all ‘1’s and ‘0’s in a particular part of the value may be skipped so as to avoid broadcast addresses. The number of low order bits to check for ‘0’s and ‘1’s can be set.
2. That value is incremented and step 1 is repeated continuously or for a count.

The parameters that affect the counter’s operation are shown in Table 2-17 on page 2-62.

Table 2-17. IPv4 Mode UDF parameters

IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Loop: Repeat value	innerRepeat
Loop: increment by	innerStep
Repeat Loop: Continuously	continuousCount
Repeat Loop: times	repeat
Skip all zeros and ones	enableSkipZerosAndOnes
masked with	skipMaskBits
Set from Init Value Continue from last value for this stream	cascadeType enableCascade

The operation of IPv4 mode is described in the flowchart shown in Figure 2-46 on page 2-60.

Figure 2-48. UDF IPv4 Mode Operation

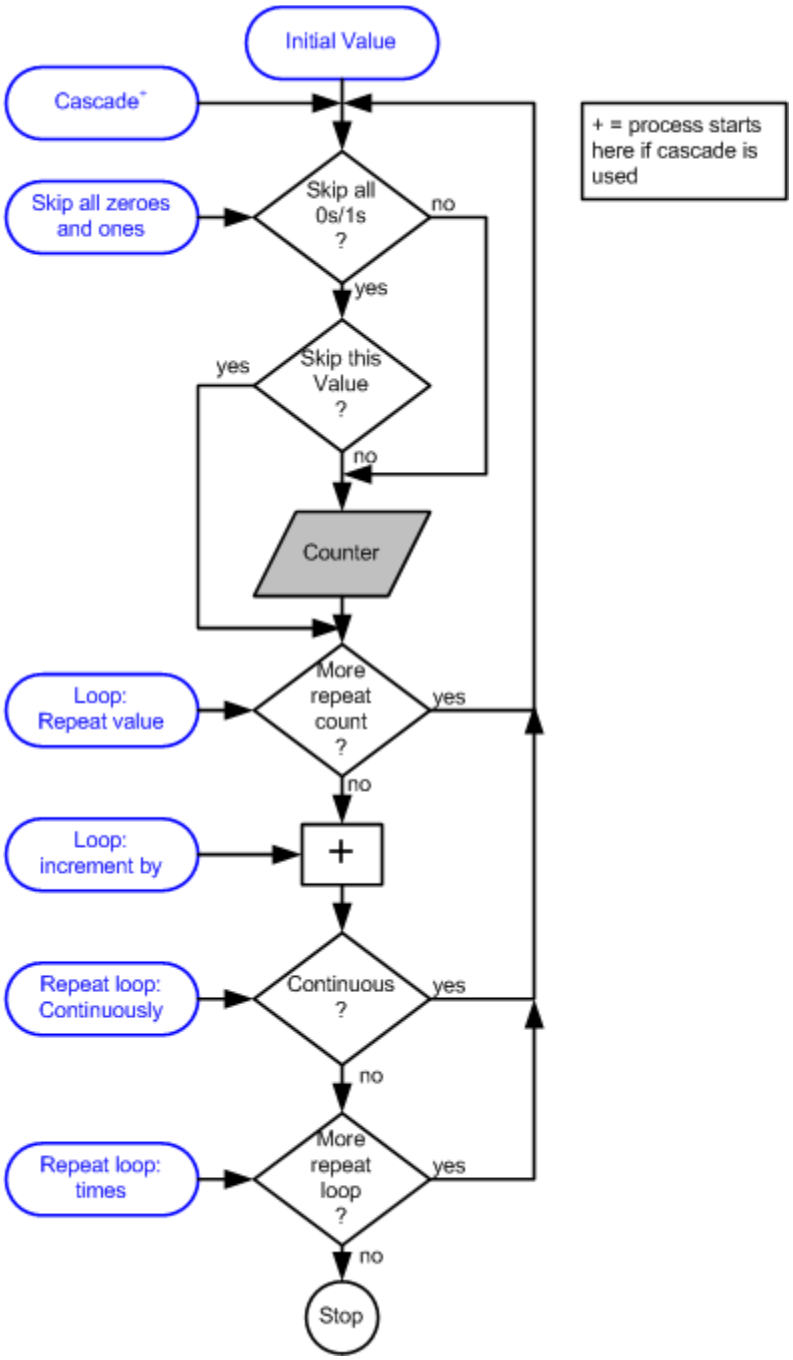
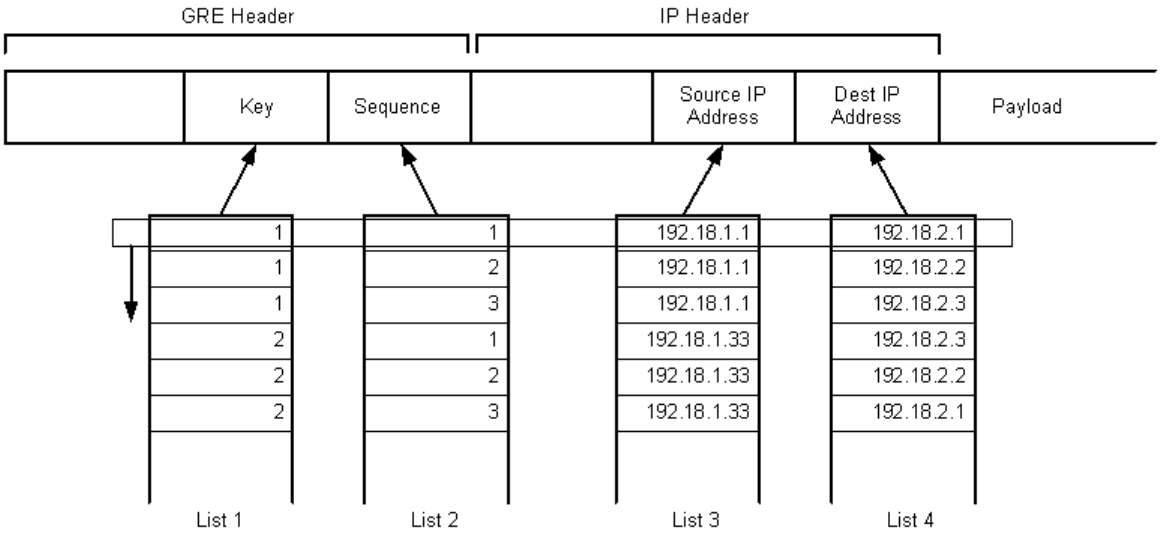


Table Mode UDF

Table UDFs allows to specify a number of lists of values to be placed at designated offsets within a stream. Each list consists of an Offset, a Size, and a list of values.

Figure 2-49 on page 2-64 illustrates the basic operation of the Table UDFs using a GRE encapsulated packet as an example. Four of the fields in the packets need to be modified on a packet by packet basis—the key and sequence GRE fields and the source and destination IP addresses in the IP header. The Table UDF provides a means by which lists are developed for each of these fields and the list is associated with an offset and size within the packet. During stream generation, all lists are applied at the same time in lock step.

Figure 2-49. Table UDF Mode



A Table UDF is applied before, and can be combined with, the standard UDF fields already available on ports. By combining these two features you can model multiple flows using the powerful combination of a value list group for flow identity fields and UDFs for protocol related timestamp/sequence fields.

Table Mode UDF has a limitation compared to the other UDFs. Specifically, Table Mode behaves differently when Random Data payload is enabled for the frame.

Most UDFs are attached to the frame after the Random Data is placed in the frame; the UDFs ‘overlay’on top of the random data. The Table Mode UDF data, however, is put in the frame *before* the random data. As a result, the payload is random only after the Table UDF.

For example, if a frame has a Table UDF that is 1 byte wide starting at offset 100, random data cannot appear in the payload until byte 101. Thus, the first 100 of these frames would have the same ‘random’ data appear within the first 99 bytes of the payload—for all 100 frames. The data would truly appear random starting at byte 101, after the Table UDF insertion.

This is the same limitation currently for random data packets that have PGID or Data Integrity enabled.

The parameters that affect the counter's operation are shown in Table 2-18 on page 2-65.

Table 2-18. Table Mode UDF Parameters

IxExplorer Label	Tcl API Variables
Offset	offset
Counter Type	countertype
Init Value	initval
Add Column	addColumn
Add Row	addRow
Clear All Columns	clearColumns
Get First Column	getFirstColumn
Get Next Column	getNextColumn
Clear All Rows	clearRows
Get First Row	getFirstRow
Get Next Row	getNextRow
Export to File	export
Import from File	import

Transmit Operations

The transmit operations may be performed across any set of chassis, cards, and ports specified by you. These operations are described in Table 2-19 on page 2-65.

Table 2-19. Transmit Operations

Operation	Usage
Start Transmit	Starts the transmission operation on all ports included in the present set of ports. If no transmit operation has been performed yet, or if the last operation was *Stop Transmit*, then transmission begins with the first stream configured for each port. If a *Pause Transmit* operation was last performed, then transmission begins at the next packet in the queue for all ports.
Staggered Start Transmit	The same operation is performed as in *Start Transmit*, except that the start operation is artificially staggered across ports. The time interval between the start of transmission on consecutive ports is in the range of 25-30ms.
Stop Transmit	Stops the transmission operation on all ports included in the present set of ports. A subsequent *Start Transmission* or *Step Stream* operation commences from the first stream of each port.

Table 2-19. Transmit Operations

Operation	Usage
Pause Transmit	Stops the transmission operation on all ports in the present set of ports at the end of transmission of the current packet. A subsequent *Start Transmission* or *Step Stream* commences at the beginning of the next packet in the queue on each port.
Step Stream	Causes one packet to be transmitted from each of the ports in the present set of ports.

Repeat Last Random Pattern

The 10 GE LSM module transmit engine has the ability to provide repeatable random values in all its random number generators. This feature allows to run tests with random parameters such as frame size, frame data, and UDF values to rerun the tests with the same set of random data if a problem is found. A check box on the Port Properties transmit tab is used to enable/disable, repeating the last seed used on the port. In addition to the check box, there is a read-only window showing the last 32 bit master seed value used in generating seeds for all random number generators on the port.

Port Data Capture Capabilities

Most ports have an extensive buffer which may be used either to capture the packet data ‘raw’ as it is received, or to categorize it into groups known as Port Groups. Each port must be designated to have a *Receive mode* which is either *Capture* or *Packet Groups.* Packet groups are used in measuring latency.

The start of capture buffering may be triggered by a set of matching conditions applied to the incoming data, or all data may be captured. Packets can be filtered, as well. During capture mode operation, the amount of data saved in the capture buffer can be limited to a user-defined ‘capture slice’ portion of each incoming packet, rather than the entire packet.

Each port’s Capture trigger and filter conditions are based on:

- For Ethernet Modules:
  - Data link encapsulation type
  - Destination and source MAC addresses
  - Protocol layer type: such as IP, IPv6, and ARP
  - IPv4 and IPv6 source and destination addresses
  - TCP and UDP port numbers
  - VLAN IDs
- For POS Modules:
  - Use of PPP
  - Protocol layer type: such as IP, IPv6, and ARP

- IPv4 and IPv6 source and destination addresses
- TCP and UDP port numbers

- For ATM Modules:
  - VPI and VCI combinations
  - Protocol layer type: such as IP, IPv6, and ARP
  - IPv4 and IPv6 source and destination addresses
  - TCP and UDP port numbers
  - ATM OAM cells
- Data pattern match for the packet, and matching errors such as: Bad CRC, Bad Packet, Alignment Error, and Dribble Error
- Packet sizes within a user-specified range

Continuous Versus Trigger Capture

For some load modules, there are more advanced options provided for setting up data capture operations on a port. These options are set in the receive mode dialog for the port. The available options are described in the following list:

- Continuous Capture. Options are as follows:
  - All packets are captured.
  - All packets which match a user-defined Capture Filter condition are captured.
- Trigger Capture:
  - Capture operation starts **before** a packet matching the user-defined Trigger condition is received. Options are:
    - All packets are captured.
    - No packets are captured.
    - All packets which match a user-defined Capture Filter condition are captured.
  - Capture operation starts **after** a packet matching the user-defined Trigger condition is met. Options are:
    - All packets are captured.
    - All packets that match a user-defined Capture Filter condition are captured.
    - All packets that match the user-defined Trigger Capture condition are captured.
  - Trigger Position: The slider bar is used to set the position (% transmitted) in the data stream where the Capture Trigger is first applied to incoming packets.

Port Capture Operations

The data capture operations may be performed across any set of chassis, cards, and ports defined by you. These operations are described in Table 2-20 on page 2-68.

Table 2-20. Capture Operations

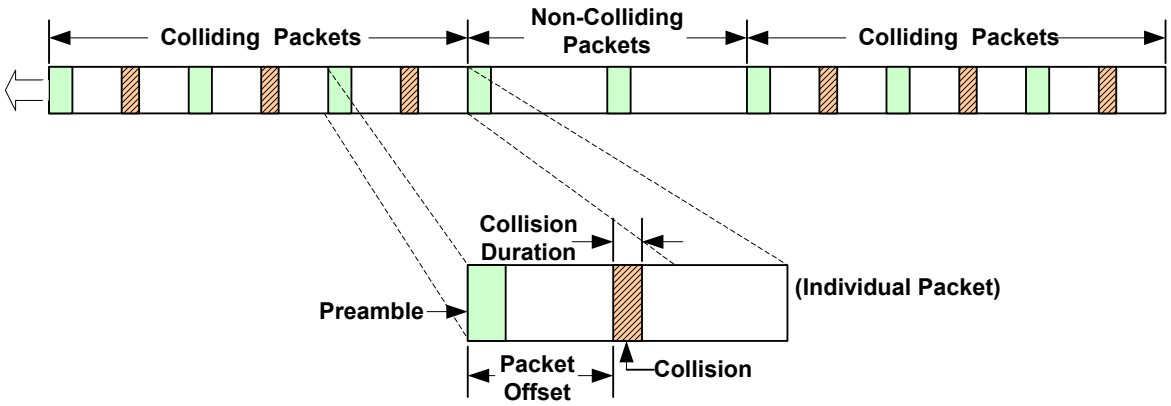
Operation	Usage
Start Capture	Enables data capture on all ports in the set of ports whose receive mode is set to *Capture*. Packets are not actually captured until the user-specified capture trigger condition is satisfied.
Stop Capture	Stops data capture on all ports in the set of ports.
Start Latency	Initiates latency measurements for all ports in the set of ports whose receive mode is set to *Packet Group* operation.
Stop Latency	Stops latency measurements on all ports in the set of ports.
Start Collision	Enables generation of forced collisions on received data, for all ports in the set of ports—if this option is selected for the port and enabled. Applies to half-duplex 10/100 Ethernet connections only.
Stop Collision	Stops generation of forced collisions for all ports in the set of ports.

Forced Collision Operation

In addition to normal capture operation, forced collisions can be generated on the receive side of some 10/100/1000 load module ports, but only when the port is in half-duplex mode.

Forced collisions operate by generating ‘collision’ data as information is being received on the incoming port. The ‘collision’ takes the form of a number of nibbles inserted at a user-specified offset within a packet as it is received. A period with a number of consecutive ‘collisions’ is followed by a period with no collisions. This combination of collisions and non-colliding periods can be repeated indefinitely, or repeated for a user-specified number of times. These parameters are shown in Figure 2-50 on page 2-69.

Figure 2-50. Forced Collisions



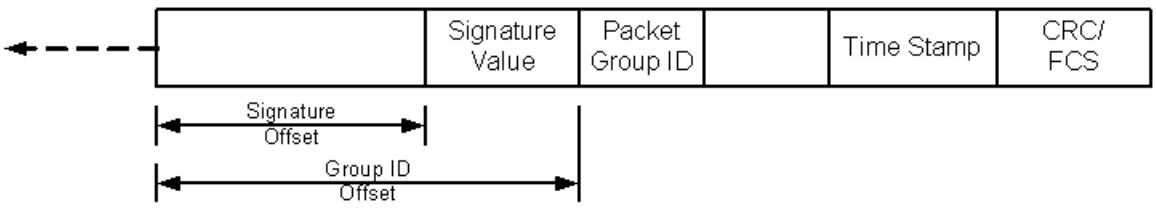
Packet Group Operation

Packet groups are sets of packets which have matching tags, called *Packet Group IDs*. Real-time latency measurements within packet groups depend on coordination between port transmission and port reception. Each transmitted packet must include an inserted 4-byte packet 'group signature' field, which triggers the receiving port to look for the packet group ID. This allows the received data to be recognized and categorized into packet groups for latency analysis.

Packet group IDs should be used to group similar packets. For example, packet groups can be used to tag packets connected to individual router ports. Alternatively, packet groups may be used to tag frame sizes. Such groupings allow to measure the latency with respect to different characteristics (for example, router port number or frame size as in the above scenario).

After packet group operation is triggered on the receiving port, the packet group ID—a 2-byte field which immediately follows the signature—is used as an index by the port's receive buffer to store information related to the latency of the packet. When packet group signatures and packet group IDs are included in transmitted data, an additional time stamp is automatically inserted into the packet. Figure 2-51 on page 2-69 shows the fields within packets which are important for packet grouping and latency analysis.

Figure 2-51. Packet Format for Packet Groups/Latency



A special version of packet groups, known as wide packet groups, uses a 4-byte packet group ID, of which only the low order 17 bits are active. A mask may be applied to the matching of the packet group ID. Latency, sequence checking, and

first/last timestamps are supported at the same time. Latency over time and data integrity checking are not supported in this mode. Frames must be greater than or equal to 64 bytes.

Split Packet Group Operation

Split PGID allows the 32-bit PGID field used to identify and group packets to be generated from a concatenation of three separate PGID fields. Note that the method for detecting and determining if a packet has a valid signature is no different from standard PGID operation. A valid signature is still required before the concatenated PGID is considered to be valid.

Instead of having one PGID offset value with one mask, you are allowed to enter up to three separate PGID offsets and masks. The split PGID method works with both the standard instrumentation method or the floating instrumentation method, and does not interfere with other features such as time bins and bin by latency.

In addition to having three 16 bit offset values and three 32 bit mask values, the following possibilities are available for the PGID offset:

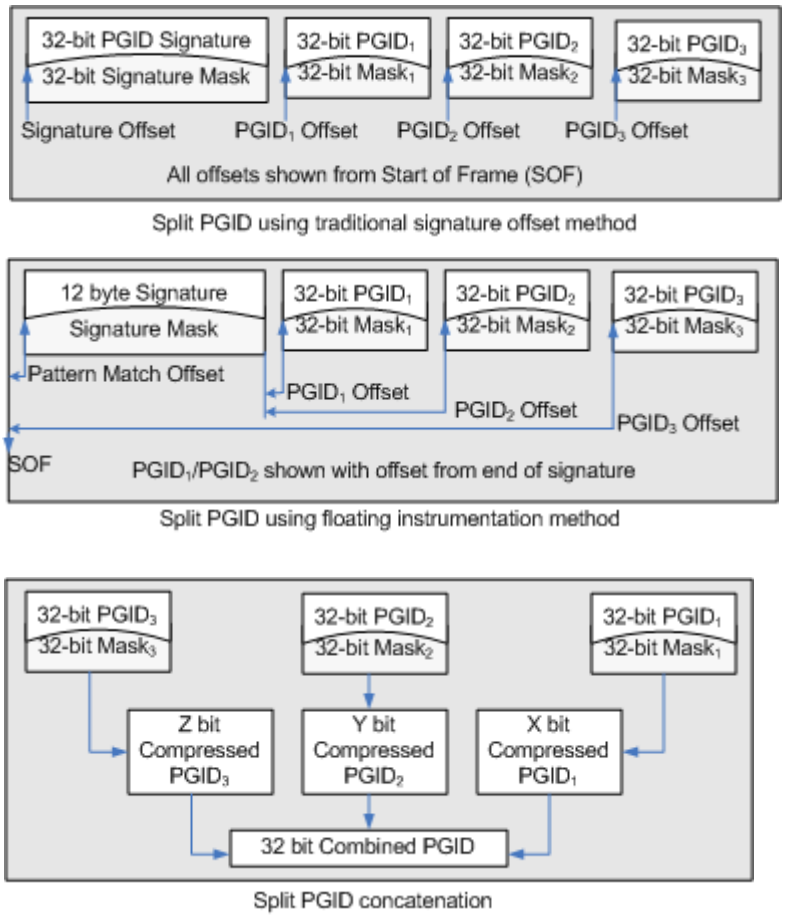
- Offset from Start of Frame (Original starting point for PGIDs)
- Offset from End of Floating Instrumentation Pattern Match
- Offset from Start of IP
- Offset from Start of Protocol

The definition of the mask is also different when in split PGID mode. In the standard PGID mode, the mask is only used to zero out PGID values and not to change the width of the final PGID. In split PGID mode, the mask is used to reduce the overall width of the PGID value for that region. A value of 1 in mask field indicates the bit is discarded (masked out).

The final 32 bit PGID value used is a concatenation of the values extracted based on the offset/mask combinations provided for the three PGID regions. The final 32 bit PGID is generated by concatenating the three regions as follows: PGID3, PGID2, and PGID1. If the concatenation of the three regions is not sufficient to fill the 32 bit value, a padding of 0 is used on the remaining leftmost bits.

Figure 2-52 on page 2-71 demonstrates the three options when employing split PGIDs.

Figure 2-52. Split PGID Scenarios



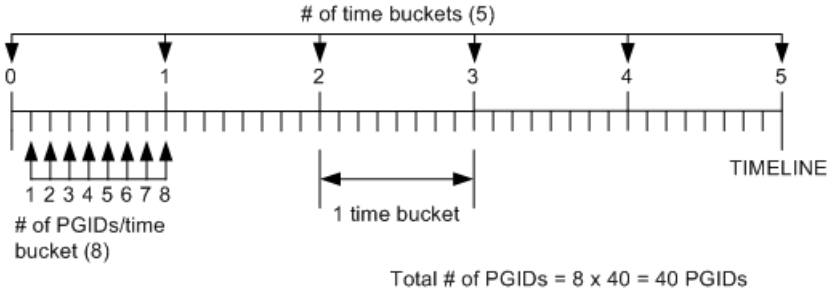
Latency/Jitter Measurements

Latency and Jitter can be measured when packet groups are enabled on a transmitting port and received on a port enabled to receive packet groups. The difference between the received time and the transmitted time held in the packet's time stamp is the measured latency or jitter. The latency is included in a memory cell indexed by the packet group ID. The count of packets received, minimum, maximum, average, and mean latencies are maintained. There are two modes for latency measurement:

- Instantaneous: Latency measured for all received data (continuous). The number of PGID groups available depends on the features being employed on the receive side. The PGID is used as an index into an area of cells and the count/min/max/avg/mean is maintained for each PGID.
- Latency over time: Latency measured for a number of time intervals of equal length, called 'time buckets.' The range of cells is divided up over a period of time—for example, for one second intervals over a 30 second period. Each time period (one second in this example) is called a *time bucket*. Within each time bucket, the data for all PGIDs must be stored into a limited number of cells. This is accomplished by grouping a number of

PGIDs together. The grouping is called the '# of PGIDs/Time Bucket'. Figure 2-53 on page 2-72 demonstrates the relationship between the time buckets and PGIDs in an example. The minimum size time bucket varies by port type, but the size set should be reasonable for the transmission speed of the port—certainly no shorter than 1 microsecond.

Figure 2-53. Multiple Latency Time Measurements—Example



The timeline is equally divided into a *# of Time Buckets,* each of which is **one** *Time Bucket Duration* in length. A time bucket duration can range anywhere from nanoseconds to hours, depending on the user configuration.

The maximum number of time buckets that can be handled is determined by the number of PGIDs in each bucket.

Four types of timing measurements are available, corresponding to the type of device under test:

- Cut-Through: For use with switches and other devices that operate using packet header information. The time interval between the first data bit out of the Ixia transmit port and the first data bit received by the Ixia receive port is measured. The first data bit received on Ethernet links (10/100 and Gigabit modules) is the start of the MAC DA field. For Packet over SONET links, the first bit received is the start of the IP header.
- Store and Forward: For use with routers and other devices that operate on the contents of the entire packet. The time interval between the last data bit out of the Ixia transmit port and the first data bit received by the Ixia receive port is measured. The last data bit out is usually the end of the FCS or CRC, and the first data bit received is as described above for Cut Through.
  NOTE: Store and Forward latency mode is intended to test Store and Forward switching devices, which receive the entire packet before transmitting it to its destination. If Store and Forward latency is used in loopback, back-to-back or without a Store and Forward switch, then either a zero latency or very high latency is reported.
- Store and Forward Preamble (only available on some load modules): As with store and forward, but measured with respect to the preamble to the Ethernet frame. In this case, the time interval between the last data bit out of the Ixia transmit port and the first preamble data bit received by the Ixia receive port is measured. For this measurement, the size of the preamble (in bytes) is considered.
- Inter-Arrival Time (IAT): Compares the time between PGID packet arrivals. In this case, when a packet with a PGID is received, the PGID is examined. If

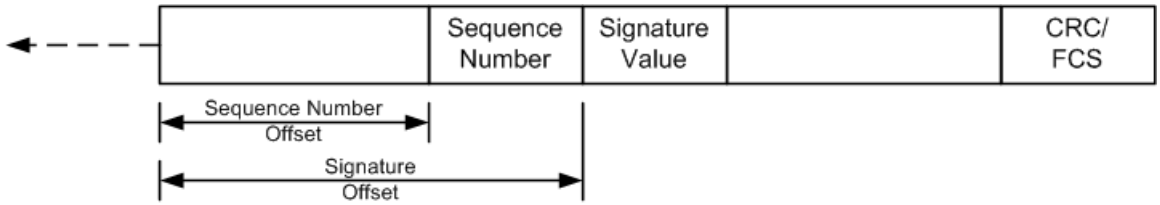
a packet has already been received with the same PGID, then the timestamp of the previous packet is subtracted from the current timestamp. The interval between the timestamps is the jitter, and it is recorded for statistical purposes.

Sequence Checking Operation

A number of ports have the additional ability to insert a sequence number at a user-specified position in each transmitted packet. This sequence number is different and distinct from any IP sequence number within an IP header. On the receiving port, this special sequence number is retrieved and checked, and any out-of-sequence ordering is counted as a sequence error.

As in packet groups (see *Packet Group Operation* on page 2-69), for sequence checking a signature value is inserted into the packet on the transmit side to signal the receive side to check the packet. In fact, this particular signature value is shared by both the packet group and the sequence checking operations. Both the signature value and sequence number are 4-byte quantities and must start on 4-byte boundaries. These fields are shown in Figure 2-54 on page 2-73.

Figure 2-54. Packet Format for Sequence Checking



Sequence numbers are integers which start at ‘0’ for each port when transmission is started, and increment by ‘1’ continuously until a Reset Sequence Index operation is performed. Note that multiple sequence errors results when a packet is received out of sequence. For example, if five packets are transmitted in the order 1-2-3-4-5 and received in the order 1-3-2-4-5, three sequence errors are counted:

1. At 1-3, when packet 2 is missed
2. At 1-3-2, when 2 is received after 3
3. At 1-3-2-4, when 4 is received after 2

Switched-Path Duplicate/Gap Checking Mode

This is a mode in sequence checking that allows for detecting duplicate packets, or sequence gaps. IxExplorer stores the largest sequence number received. Any packet that arrives with a lower or equal sequence number is regarded as a duplicated packet. For a flow with no packet reordering, the ‘reversal errors’ matches the number of duplicates received. For a flow with packet reordering, the ‘reversal errors’ gives a count that may be higher than the number of duplicates received.

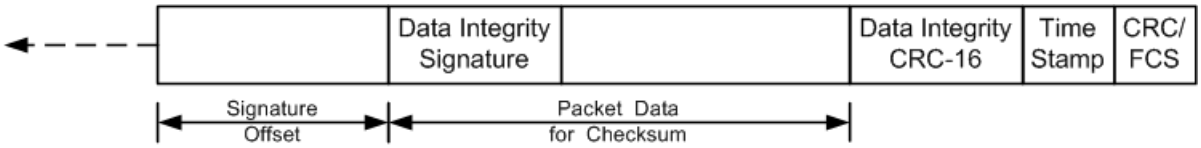
Data Integrity Checking Operation

A number of ports also possess the ability to check the integrity of data contained in a received packet, by computing an additional 16-bit CRC checksum.

As with packet groups (see *Packet Group Operation* on page 2-69) and sequence checking (see *Sequence Checking Operation* on page 2-73), a signature value is inserted into the packet on the transmitting interface, to serve as a trigger for the receiving port to notice and process the additional checksum. The data integrity operation uses a different signature value from the one shared by packet groups and sequence checking.

The data integrity signature value marks the beginning of the range of packet data over which the 16-bit data integrity checksum is calculated, as shown in Figure 2-55 on page 2-74. This packet data ends just before the timestamp and normal CRC/FCS. The CRC-16 checksum value must end on a 4-byte boundary. There may be 1, 2, or 3 bytes of zeroes (padding) inserted after the CRC-16, but before the Time Stamp, to enforce all boundary conditions.

Figure 2-55. Packet Format for Data Integrity Checking



When the Receive Mode for a port is configured to check for data integrity, received packets are matched for the data integrity signature value, and the additional CRC-16 is checked for accuracy. Any mismatches are recorded as data integrity errors.

Automatic Instrumentation Signature

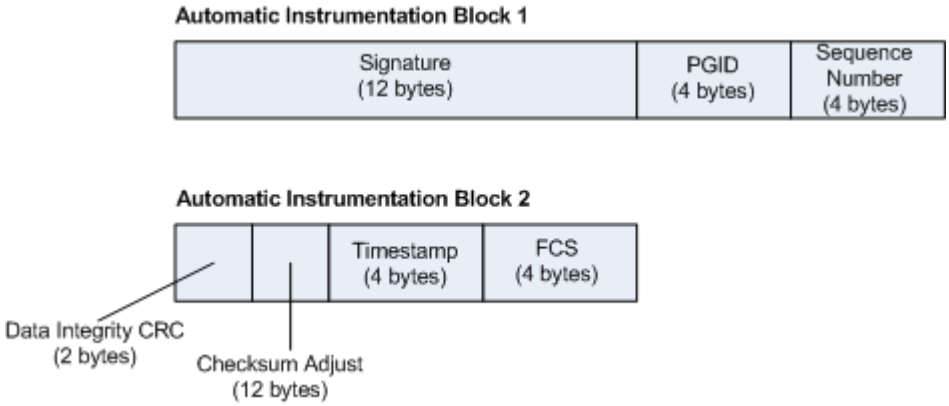
The Automatic Instrumentation Signature feature allows the receive port to look for a signature at a variable offset from the start of frames. The feature supports Sequence Checking, Latency, Data Integrity functionality, with signature and Packet Group ID (when Automatic Instrumentation is enabled, these receive port options are enabled as well).

In normal stream operation, signatures for Data Integrity, Latency, and Sequence Checking are forced to a single, uniform offset location in each frame of the stream. Many of the Ixia software application (that is, IxVPN, IxChariot, and so forth) can generate streams that place a signature at random places within the frames of a single stream. To accurately detect these signatures on the receive side of the chassis, Automatic Instrumentation Signature is used.

Automatic Instrumentation Signature allows the chassis to look for a floating pattern in the frame. Two data blocks are placed in the frame (by some stream generating application). The first is positioned at a variable offset from the start of the frame. The second is positioned at a fixed 12 byte offset from the end of the frame.

Figure 2-56 shows the composition of the blocks.

Figure 2-56. Automatic Instrumentation Signature Block



The receive port recognizes an instrumented frame by detecting the Signature in the first block. Once a signature match has occurred, the Packet Group ID (PGID) and Sequence Number are extracted from the frame. Data Integrity also starts immediately following the signature.

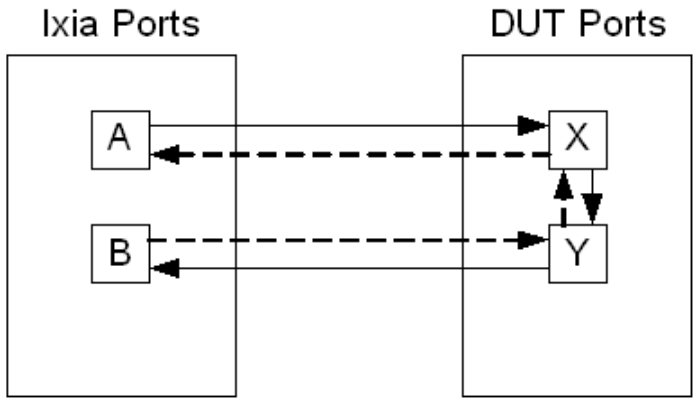
The Checksum Adjust field is reserved for load modules that cannot correctly do checksums on large frames.

Port Transmit/Receive Capabilities

Round Trip TCP Flows

For most 10/100 load modules, a special capability exists in the Ixia hardware to enable the measurement of round trip times for IP packets sent through a switch or other network device. The normal setup for this measurement is shown in Figure 2-57 on page 2-75.

Figure 2-57. RoundTrip TCP Flows Setup



In this scenario, Ports A and X are configured on one IP subnet, and Ports B and Y are configured on a different IP subnet. IP packets sent from A have a source

address of A and destination address of B. The DUT is configured to route or forward to Y any packets that it receives on X for an address on B-Y's subnet. After being received on Port B, the packet is reconstructed in a modified form as described in the following list, and sent back in the opposite direction along the path to Port A.

When enabled on the Ixia receiving port (in this case, Port B), the Round Trip TCP Flows feature performs several operations on the received IP packet:

- The Source and Destination IP addresses are reversed, and a packet destined for Port A is created using the reversed addresses.
- The frame size, source and destination MAC addresses, and background data pattern are set as specified by you.
- The timestamp is copied to the new packet unmodified.
- The new packet is transmitted to Port Y on the DUT, and should be routed back to Port A by the DUT.

This re-assembly/retransmit process makes it possible to measure the round-trip time for the packet's trip from Port A through the DUT to Port B, and back through the DUT to Port A again. Note that the Packet Groups feature may be used, in addition, for latency measurements on this round trip. For latency testing, the background data set by the Round Trip TCP Flows feature overwrites the Packet Group Signature Value contained in the packet. It is important that proper programming of the background data pattern be used to insert the appropriate signature value back into the packet.

Port Statistics Capabilities

Each port automatically collects statistics. A wide range of statistics are preprogrammed and available for many types of load modules. Other statistics may be selected or programmed and include:

- User-Defined Statistics: Four counters which can be programmed to increment based on the same conditions as those involved in defining capture triggers and capture filters.
- Quality of Service Types: Separate counts for each of eight Quality of Service values used in IP headers.
- IP/UDP/TCP Checksum Verification Statistics: For hardware checksum verification.
- Data Integrity Statistics: For errors relating to Data Integrity Operation. Refer to *Data Integrity Checking Operation* on page 2-74.
- Packet Group Statistics: For statistics relating to Latency operations. Refer to *Latency/Jitter Measurements* on page 2-71.
- Protocol Server Statistics: Protocol-based statistics for a wide range of routing protocols.
- SONET Extended Statistics: Statistics associated with SONET Line, Section and Path characteristics.
- VSR Statistics: Statistics associated with OC192 VSR modules.
- ATM Statistics: Statistics associated with ATM modules.

- BERT Statistics: Statistics associated with BERT error generation and detection.
- Temperature Sensors Statistics: For verifying that temperatures on high-performance 10 Gigabit and OC-192c POS cards are within operational limits.

IxExplorer Software

The IxExplorer software utilizes concepts that match the Ixia hardware hierarchy. The software hierarchy is:

- *Chassis Chain (Software)*: A set of Ixia chassis joined through sync-in/sync-out cables.
  - *Chassis*: A single Ixia chassis capable of holding different Ixia module cards.
    - *Card*: An Ixia module card, all of whose ports have the same features.
    - *Port*: An individual transmit/capture port on a card.
    - Capture View: A view of the capture buffer for the port.
    - Filters, Statistics and Receive Mode: A means of programming capture triggers, filters, and statistics.
    - Packet Streams: A means of programming sets of streams and flows.
    - Statistics: A view of the statistics gathered by the port.
- *Global Views:*
  - *Port Groups*: Hold groups of related ports that may be operated on at the same time.
  - *Stream Groups*: Hold groups of related ports that may be operated on at the same time.
  - *Packet Group Statistic Views*: Allows the latency data (including Inter-Arrival Time) to be collected from one or more ports that are configured to receive packet groups.
  - *Statistic Views*: Holds groups of related ports, all of whose statistics can be viewed at one time.
  - *Stream Statistic Views*: Holds groups of related streams, all of whose statistics can be viewed at one time.
- *MII Templates*: A means of creating and editing MII templates.
- *Layouts*: A means of saving open GUI features.
- *IxRouter Window*: A means of designating interface addresses associated with ports and programming routing protocol simulations on each port. Note that IxRouter must be installed for full use of this window. Without IxRouter, only limited use of ARP and PING are allowed. See *IxRouter User Guide* for more information.

Chassis Chain (Software)

The IxExplorer chassis chain corresponds to the hardware chain. The chain starts with a master, whose sync-out line is connected to the sync-in line of the next chassis, and so on. Multiple chassis chains may be defined in the IxExplorer and operated independently or at the same time. Various forms of time

synchronization may be used to coordinate multiple chassis chains dispersed world-wide into a single ‘virtual chassis chain’; see *Chassis Synchronization* on page 2-5. The Ixia 100 chassis includes a built-in GPS receiver to provide very accurate timing.

Chassis

The IxExplorer chassis corresponds to an Ixia 1600T, 400T, 250, 100, Optixia XL10, Optixia XM12, Optixia XM2, Optixia X16 or other chassis capable of holding Ixia module cards. The name or IP address of each chassis must be input; the type of the chassis is automatically discovered by the software. A chassis may hold any mix of module cards.

Card

The IxExplorer card corresponds to an Ixia load module card. The types of cards loaded in a chassis are automatically discovered and the appropriate number of ports are inserted into the hierarchy. Each port on a card has the same capabilities.

Port

The IxExplorer port corresponds to an individual port on an Ixia module card. Each port is independently programmed in terms of its transmit, capture and statistics capabilities. The IxExplorer software shows four separate views for programming and viewing operations:

- Filters, Statistics and Receive Mode: Sets the trigger and capture conditions for the capture buffer, conditions for the four user-defined statistics, and the receive mode for the port.
- Packet Streams/Flows: Defines the streams within stream regions and the contents of packets.
- Capture View: Shows the data gathered during capture operations. Data is displayed in raw form and interpreted for some protocols.
- Statistics : Shows the live statistics gathered during transmit and capture operation.

Port Properties

A Port Properties dialog allows other port related properties to be programmed:

- Auto-Negotiation: Low level physical controls, such as 10 versus 100 Mbps operation and full duplex versus half duplex.
- Advanced MII controls: Additional low level MII register controls.
- Flow control: Related to pause control operation.
- Collision Backoff Algorithm: Handling of collision situations.
- Forced Collisions: The generation of collision packets on receive ports.
- Transmit mode: The choice of streams or flows for the port.
- SONET Header: For use with Packet Over SONET frames.
- SONET Overhead: For generation of APS (K1/K2), J0/J1 bytes, and Error Insertion.

- PPP: For use with SONET. Includes dialogs for Negotiation, Link Control Protocols, and Network Control Protocols.

Port Groups

Port groups are an IxExplorer convenience. They allow to perform operations, such as start/stop transmit, start/stop capture and clear timestamps, for a wide range of ports all at the same time.

Stream Groups

Stream groups are an IxExplorer convenience. They allow to perform operations, such as start/stop transmit, start/stop capture and clear timestamps, for a group of streams all at the same time.

Packet Group Statistic Views

The Packet Group Statistics View allows the latency data (including Inter-Arrival Time) to be collected from one or more ports that are configured to receive packet groups. Packets representing different types of traffic profiles can be associated with packet group identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time for each packet belonging to different groups. Measurable latencies include Instantaneous Latency, where each packet is associated with one group ID only, and Latency Over Time, where multiple PGIDs can be placed in ‘time buckets’ with fixed durations.

Statistic Views

Statistic Views are similar to port groups, in that they let you consider a set of ports all at once. When a Statistic View group is selected, all of the statistics for all of the ports are simultaneously viewed. The particular statistics viewed may be independently selected for each Statistic View. Statistic logging and alerts are also provided; see *Statistics Logging and Alerts* on page 2-82

Stream Statistic Views

Stream Statistic Views are like Statistic Views, but on a per stream basis rather than per port basis.

MII Templates

Allows for the creation and/or editing of MII template files. Register templates are applied to physical ports through Port Properties dialogs.

Layouts

Allows for the creation of templates for the layout of the IxExplorer GUI. A layout consists of the combined open features in the GUI.

IxRouter Window

The IxRouter window provides the means by which routing protocols are emulated by the Ixia hardware and software. This window includes the interface by which multiple IPv4 and IPv6 interfaces are associated with each port. A growing number of protocols are supported in this window, including ARP, BGP, OSPF, ISIS, RSVP-TE, LDP, RIP, RIPng, and IGMP.

Note that full use of this window requires that IxRouter be installed. For more information on protocols and protocol testing, see *IxRouter User Guide*.

IxExplorer Operation

IxExplorer saves all settings and programming in 'saved' named files, which may be retrieved on each invocation. Captured data is lost when the IxExplorer is exited.

All IxExplorer test operations perform on an arbitrary set of ports, as single port or multiple ports may be selected. Any level of the hierarchy may be selected to include all ports below that level. For example, selecting a card includes all ports on that card, or selecting a chassis chain includes all ports on all cards in all chassis in the chassis chain. In addition, port groups may contain ports from any card; the port group may then be used in any testing operations.

The operations that can be performed on any group of ports:

- Start/Stop Capture: When capture is enabled, data for each port that is configured for capture (versus latency) is collected when the trigger is satisfied and to the extent that the filter is satisfied as well.
- Start/Stop Transmit: When transmit is enabled, data is transmitted as programmed to the extent designated by the synchronous stream region.
- Start/Stop Collision: Forced collisions are enabled/disabled for receive ports.
- Start/stop Latency: When latency measurement is enabled, data for each port configured for latency (versus capture) is collected when the trigger is satisfied and to the extent that the filter is satisfied as well.
- Pause/Single-Step Transmit: Transmittal of information may be paused and then single-stepped on a stream-by-stream basis or continued through a start transmit command.
- Interactive streams: This is a special function that allows for interactive variation of frame size and inter-packet gaps. Interactive streams may not be operated across ports that are configured for flows.

Multi-User Operation

IxExplorer provides an optional means of coordinating the sharing of chassis ports among multiple users. If a single user is operating a chassis, multi-user commands are not required at all. As an user, you may perform any operation on any port. Two or more people may also share ports on a chassis without use of IxExplorer multi-user facilities, through some verbal agreement (for example, 'You take cards 1-8 and I'll take cards 9-16'). IxExplorer provides no assistance in this instance.

Where more accurate control over port sharing is required, multi-user facilities should be used. IxExplorer's multi-user model is a very simple, advisory model. Each user logs in with an arbitrary name. Each and every user may take ownership of any and all ports. A port owner has the ability to read data and program the port; all other users have read-only access to the port. A port owner may clear ownership of ports, making them available for other users. You may take ownership of a port owned by someone else, with an optional warning message. Any user may clear all ownerships.

IxExplorer provides a further distinction of roles between users. Administrators are privileged users who may take ownership of ports, configure their characteristics, and initiate tests using those ports. Operators are unprivileged users who may only look at chassis, card, and port characteristics and measured data.

Note: We NEVER support multiple clients simultaneously changing data on one port. The rule is: one port-one owner for each system test.

The ownership model should not be used to have one script take ownership of a port and another script take ownership of that same port with the same username because one client may be working with a copy of the port configuration that has been made invalid by another owner.

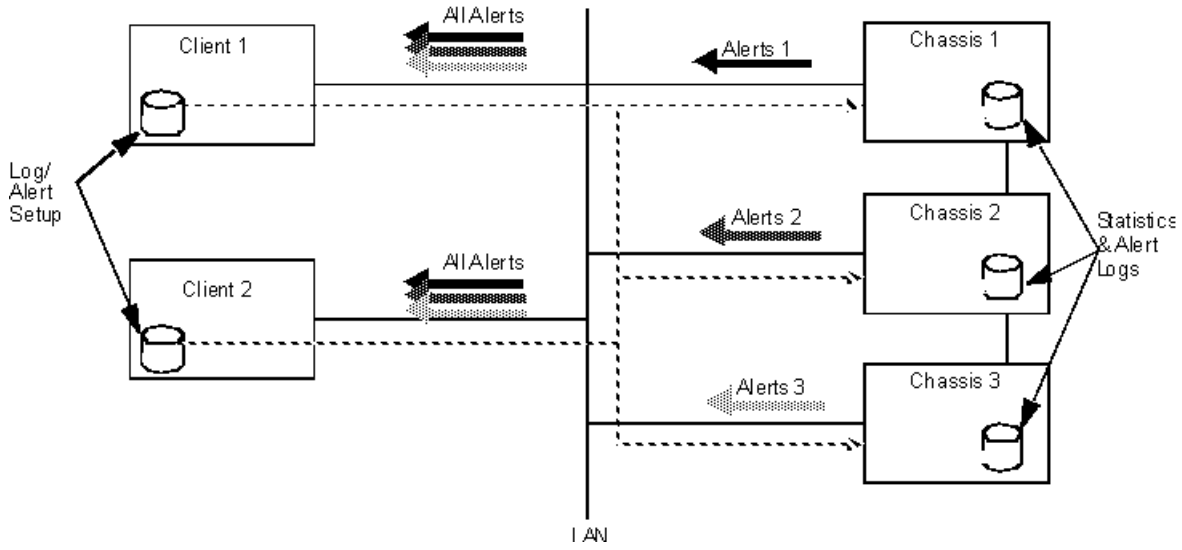
The two basic modes of multi-user operation are referred to as:

- Voluntary: All users are considered administrators and voluntarily login and take or clear ownership of ports. All chassis are initially configured in this mode.
- Secure: Users are characterized as Administrators or Operators. All users must login. Administrators operate in the same manner as all Voluntary mode users. Operators are restricted to viewing data.

Statistics Logging and Alerts

IxExplorer has the ability to centrally log statistics from any port and to signal alert conditions when a particular statistic goes out of a specified, valid range. Figure 2-58 on page 2-82 shows the basic operation of logging and alerts.

Figure 2-58. Statistics Logging and Alerts



The clients (Client 1 and Client 2) run IxExplorer and are connected to all of the chassis (Chassis 1, Chassis 2 and Chassis 3) in the chassis chain. The clients set up conditions under which statistics data is logged and alerts generated. These

conditions are transmitted to all of the chassis. Each chassis interprets these conditions and logs statistics data and alert conditions to their local disks.

When a chassis detects an alert condition, it sends signals to **all** of the clients connected to the chassis at the moment. Each client receives alerts from **all** of the chassis, regardless of whether they set up the particular alert condition themselves.

It can take considerable effort to set up one port's statistics logging and alert conditions. It is not necessary to repeat this process for multiple ports that have identical logging and alert behavior. IxExplorer's Port Copy feature may be used to copy these specifications.

It should be noted that logging and alerts continue even after a client has exited IxExplorer.

Statistics Logging

Each client selects particular statistics on particular ports to be logged. The data is logged at the chassis hosting the port. All clients connected to a chassis contribute their desired port-statistics to be logged. All statistics from all clients are logged to the same single file on a chassis.

The log file is ASCII in format and contains a line of text for each port on which statistics have been gathered. Each line contains all of the selected statistics for the port, separated by commas. The contents of the file are easiest to understand and interpret if the same statistics are gathered for all ports.

The statistic values that are logged are the 'rolling average' for the value logged. That is, a value at time slot *n* depends on the previous average and the current measured value, as per the following equation:

$$Average_n = (Average_{n-1} * (n-1)/n) + (Measurement_n * 1/n)$$

The client specifies several parameters that affect the logging of statistics:

- Enable/Disable: Enable or disable all statistics logging specified from this client.
- Log at interval: Specify an interval between logged entries.
- Log during alerts: Log statistics while alert conditions exist.
- File naming: The format and location of logging files on the chassis.

Multiple clients should agree on the log interval and file naming conventions; the chassis uses the settings received from any client that applies changes.

Alerts

Each client sets up anticipated valid ranges for particular statistics on specific ports. All clients connected to a chassis distribute their specific valid ranges to all chassis. Each chassis watches for out of range values on the specified port-statistics and generates alerts for the conditions. **All** alert conditions are sent to

all connected clients. Alert condition changes may be optionally logged on files at the chassis.

The client indicates how it wants to receive alerts for a particular statistic and port. There are three options:

- Visual: each statistic subject to alerting is displayed as green (in range), red (out of range) or yellow (was previously out of range) in any Statistic View containing the port-statistic.
- Audible: while any out of range condition exists, the client's computer issues a repeating beep-beep. A client may mute all audible alarms at once.
- Both visual and audible.

In addition, the existence of an alert condition for a particular port-statistic may be used to initiate statistics logging for that port, as described in *Statistics Logging* on page 2-83.

The client specifies several parameters that affect the setup of alert conditions:

- Enable/Disable alerts: Enable or disable all visual and/or audible alerts specified from this client.
- Enable/Disable Alert Logging: Enable or disable the logging of alert change conditions on the chassis.
- File Naming: The format and location of alert files on the chassis.

Multiple clients should agree on the valid range of port-statistics values and file naming conventions; the chassis uses the settings received from any client that applies changes.

Tcl Software Structure

The Tcl software is structured as a number of client-server pieces so that it may operate simultaneously in three different environments:

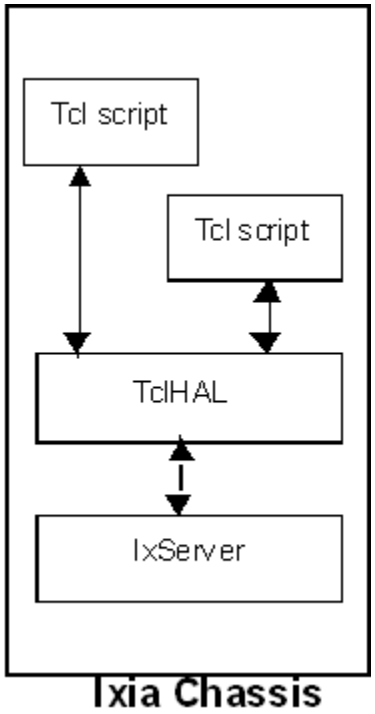
- On the Ixia chassis: The Tcl scripts are executed on the same computer that runs the Ixia hardware.
- On a Windows client: The Tcl scripts are executed on a Windows 2000/XP client.
- On a Unix client: The Tcl scripts are executed on a Unix client.

The following sections describe the components used in each of these scenarios.

Operation on the Ixia Chassis

When the Tcl client software is installed on the Ixia chassis itself three distinct software components are used, as shown in Figure 2-59 on page 2-85.

Figure 2-59. Software Modules Used on an Ixia Chassis



In this scenario, three components are used as described in Table 2-21.

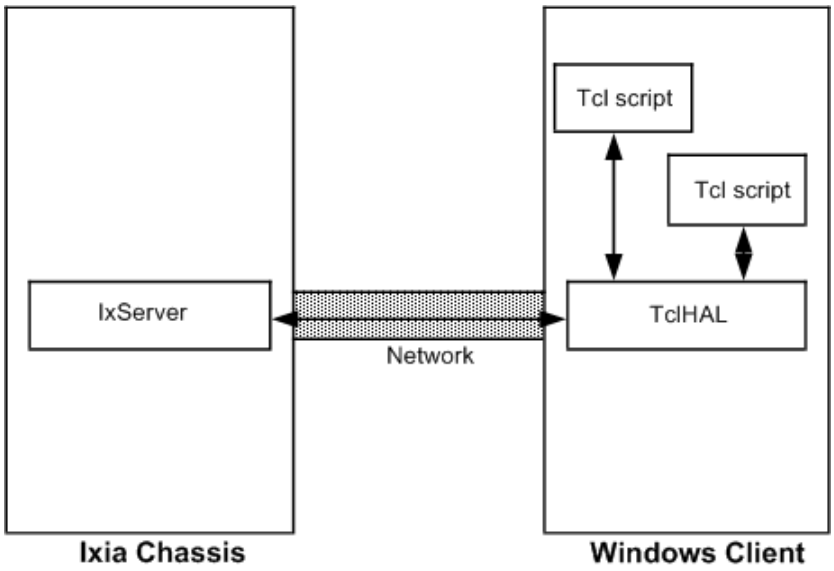
Table 2-21. Software Modules Used on an Ixia Chassis

Module	Usage
Tcl scripts	Ixia supplied and user developed Tcl. The Tcl extensions that program the Ixia hardware use the TclHAL layer.
TclHAL	A layer of software, supplied as a DLL (Dynamic Linked Library), that is responsible for interpreting the Tcl commands into C++ functions to be sent to the IxServer software.
IxServer	An independent Windows executable that is responsible for directly controlling the Ixia hardware.

Operation on a Windows Client

When the Tcl client software runs on a Windows client, the same three components are used but in a different configuration, as shown in Figure 2-60 on page 2-86.

Figure 2-60. Software Modules Used on a Windows Client



In this scenario, three components are used as described in Table 2-22.

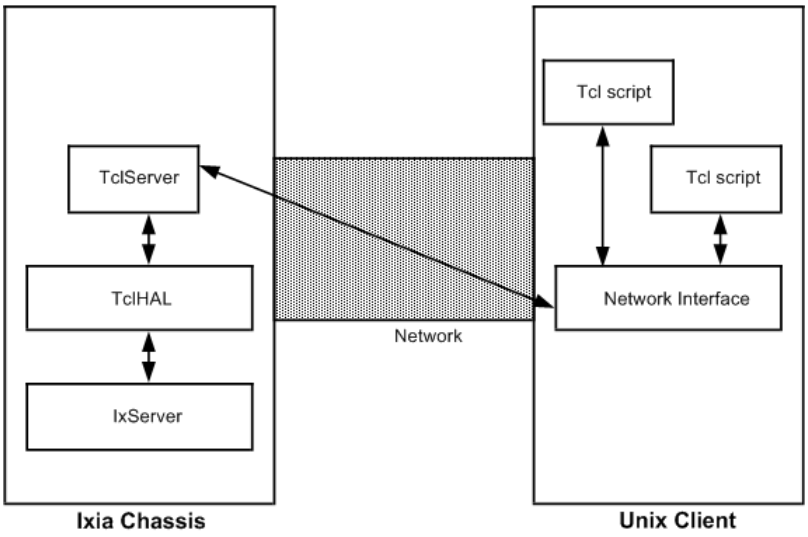
Table 2-22. Software Modules Used on a Windows Client

Module	Usage
Tcl scripts	Ixia supplied and user developed tests run on the Windows client using the Tcl software. The Tcl extensions that program the Ixia hardware use the TclHAL layer.
TclHAL	A layer of software, supplied as a DLL (Dynamic Linked Library), that is responsible for interpreting the Tcl commands into C++ functions to be sent to the IxServer over the local network.
IxServer	An independent Windows executable running on the Ixia Chassis that is responsible for directly controlling the Ixia hardware. Its commands are received from clients over the LAN.

Operation on a Unix Client

When the Tcl client software runs on a Unix client, five components are used as shown in Figure 2-61 on page 2-87.

Figure 2-61. Software Modules Used on a Unix Client



In this scenario, five components are used as described in Figure 2-23 on page 2-87.

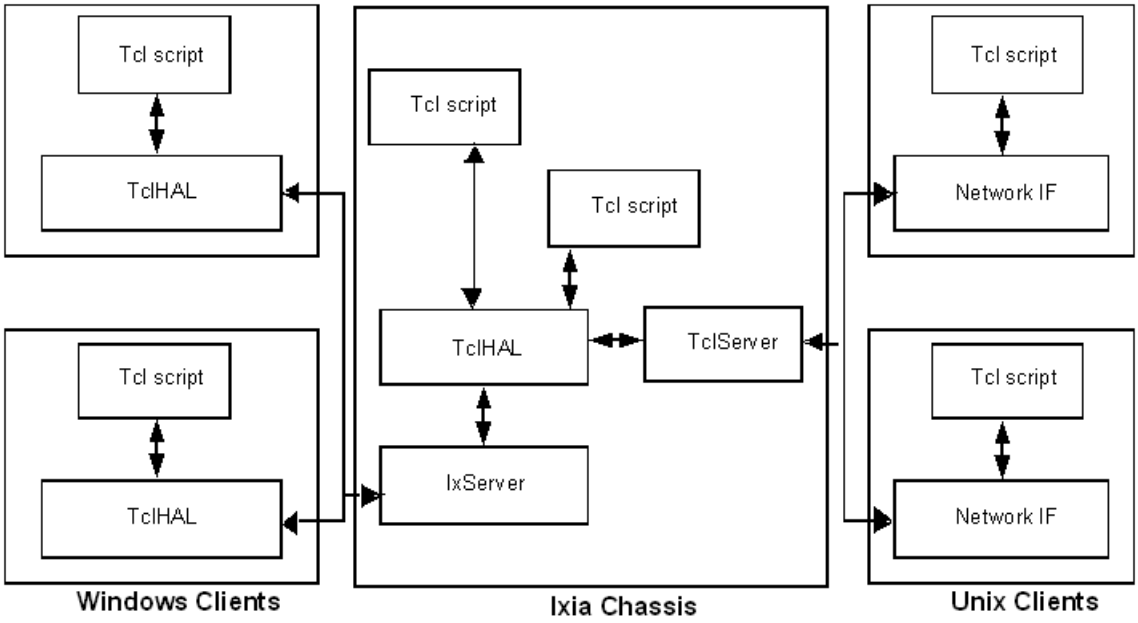
Table 2-23. Software Modules Used on a Unix Client

Module	Usage
Tcl scripts	Ixia supplied and user developed tests run on the Windows client using the Tcl software. The Tcl extensions that program the Ixia hardware use the Tcl-DP client software.
Network Interface	This is a layer of software within the TCL system that translates hardware commands into ascii commands, which are sent to the TCL Server on the connected Ixia chassis.
TclServer	This layer receives commands from the Tcl-DP client on Unix client platforms. Commands are translated into calls to the TclHAL layer.
TclHAL	A layer of software, supplied as a DLL (Dynamic Linked Library), that is responsible for interpreting the Tcl commands into C++ functions to be sent to IxServer on the chassis over the network.
IxServer	An independent Windows executable running on the Ixia Chassis that is responsible for directly controlling the Ixia hardware. Its commands are received from clients over the LAN.

Multiple Client Environment

A single Ixia chassis may be used by multiple clients simultaneously. Clients may run from the Ixia chassis, Windows clients, and Unix clients simultaneously, as shown in Figure 2-62 on page 2-88.

Figure 2-62. Multi-Client Environment



TCL Version Limitations

Note the following limitation with respect to Tcl versions and the use of Wish and Tclsh shells:

1. Tcl 8.0 is no longer supported.
2. Tclsh does not run on any version of Windows, with Ixia software. Under Linux or Solaris, Tclsh runs on any version of Tcl greater than or equal to 8.2.

The use of the Wish shell with Ixia software has been tested for Tcl 8.3 under Windows, Linux, and Solaris. It has not been tested, but should run with any Tcl version greater than or equal to 8.2.

Beginning with the Ixia TCL libraries supplied with IxOS version 3.80, these libraries are compatible with TCL version 8.3 and above. That is, it is not necessary to obtain a new version of the Ixia libraries when TCL 8.4 (or above) is installed on a computer.

3 Theory of Operation: Protocols

Protocol Server

Most ports in an Ixia chassis operate a Protocol Server. The Protocol Server includes a complete TCP/IP stack, allowing different forms of high-level DUT testing. The Protocol Server can be configured to test a set of provided Level 2 and Level 3 protocols, which include MAC and IP addressing and IP routing. The Protocol Server for Packet over SONET cards omits all MAC configuration items, since POS does not use a MAC layer. The information gathered by the Protocol Server is used within generated frame data, as well.

The Protocol Server can be accessed through the IxRouter Window. Each protocol must be individually enabled for a selected port in the IxRouter Window.

The protocols supported by the Ixia Protocol Server are described in the following sections in this chapter:

Table 3-1. Protocols Supported by Ixia Protocol Server

Address Resolution Protocol (non-POS only) **(includes IP to MAC addressing)**	See *ARP* on page 3-2
Internet Gateway Management Protocol	See *IGMP* on page 3-3
Open Shortest Path First Protocol	See *OSPF* on page 3-4
Open Shortest Path First Protocol Version 3 (for IPv6)	See *OSPFv3* on page 3-7
Border Gateway Protocol	See *BGP4/BGP+* on page 3-8
Routing Information Protocol	See *RIP* on page 3-14
Routing Information Protocol: Next Generation (for IPV6)	See *RIPng* on page 3-16
Intermediate System to Intermediate System (Dual Mode)	See *ISISv4/v6* on page 3-17

Table 3-1. Protocols Supported by Ixia Protocol Server

Resource ReSerVation Protocol: with Traffic Engineering Extensions	See *RSVP-TE* on page 3-20
Label Distribution Protocol	See *LDP* on page 3-27
Multicast Listener Discovery	See *MLD* on page 3-28
Protocol Independent Multicast: Sparse Mode	See *PIM-SM/SSM-v4/v6* on page 3-29
Multi-Protocol Label Switching	See *MPLS* on page 3-34
Bi-Directional Forwarding	See *BFD* on page 3-36
Connectivity Fault Management	See *CFM* on page 3-37
Fibre Channel over Ethernet (FCoE), FCoE Initialization Protocol (FIP) and NPIV	See *FCoE and NPIV* on page 3-39
Precision Time Protocol (PTP)	See *Precision Time Protocol (PTP) IEEE 1588v2* on page 3-41

There are additional sections on the following topics:

- *ATM Interfaces* on page 3-46
- *Generic Routing Encapsulation (GRE)* on page 3-53
- *DHCP Protocol* on page 3-57
- *Ethernet OAM* on page 3-59

ARP

The Address Resolution Protocol (ARP) facility controls the manner in which ARP requests are sent. This option is only available on Ethernet load modules. The resulting responses from ARP requests are held in the ARP Table, which is used to set MAC addresses for transmitted data. ARP'ing the Device Under Test (DUT) allows tests and generated frames to be configured with a specific IP address, which at run time is associated with the MAC address of that particular DUT.

IP

The IP table within the ARP window specifies a per-port correspondence between IP addresses, MAC addresses (for Ethernet ports only), and the Default

Gateway. IP addresses may be expressed as individual addresses or as a range of addresses.

All ARP requests (for Ethernet) are sent to the Default Gateway address. In most cases, the Default Gateway Address is the address of the DUT. When a gateway separates the Ixia port from the DUT, use the IP address of that gateway as the Default.

IGMP

The Internet Group Management Protocol (IGMP) is used with IPv4 to control the handling of group membership in the Internet. Version 3, specified in RFC 3376, is supported and is interoperable with Versions 1 and 2. Version 1 of the protocol is specified in RFC 1112, and Version 2 is specified in RFC 2236.

IGMP normally works in an environment in which there are a number of IGMP-capable hosts connected to one or more IGMP routers. The routers forward membership information and packets to other IGMP routers and receive group membership information and packets from other IGMP routers.

The Ixia hardware simulates one or more hosts, while the DUTs are assumed to be IGMP routers. The simulation calls for groups of simulated hosts to respond to IGMP router-generated queries and to automatically generate reports at regular intervals. A number of IGMP groups are randomly shared across a group of hosts.

Version 3 adds the concept of filtering, based on the IP source address, to cut down on the reception of unwanted multicast traffic. This filtering consists of limiting the receipt of packets to only those from specific sources (INCLUDE) or to those from all but specific sources (EXCLUDE). Refer to *MLD* on page 3-28 for information about similar functions for multicast traffic in IPv6 environments.

Compatibility with earlier versions of IGMP is an important part of IGMPv3. The Group Compatibility Modes for an IGMPv3 router are summarized as follows:

- IGMPv3 Compatibility Mode (default): An IGMPv2 and/or IGMPv1 Host is present, but NOT running.
- IGMPv2 Compatibility Mode: An IGMPv2 Host may be present and running. An IGMPv1 Host is present, but NOT running.
- IGMPv1 Compatibility Mode: An IGMPv1 Host is present and running.

OSPF

Note: See also *OSPFv3* on page 3-7.

Open Shortest Path First (OSPF) is a set of messaging protocols that are used by routers located within a single Autonomous System (AS). The Ixia hardware simulates one or more OSPF routers for the purpose of testing one or more DUT routers configured for OSPF. The OSPF version 2 specification (RFC 2328) details the message exchanges by OSPF routers, as well as the meanings and usage.

OSPF has the following three principal stages:

- The HELLO Protocol
- Database transfer
- HELLO Keepalive

When an OSPF router initializes, it sends out HELLO packets and learns of its neighboring routers by receiving their HELLO packets. If the router is on a Point-to-Point link, or on an Ethernet (transit network) link, these packets are addressed to the *AllSPFRouters* multicast address (224.0.0.5). In these types of networks, there is no need to manually configure any neighbor information for the routers.

Each router that is traversed on the path between neighbors is added to a list contained in the HELLO packet. In this way, each router discovers the shared set of neighbors and creates individual state machines corresponding to each of its neighbors.

If the network type is broadcast, then the process for selecting a Designated Router (DR) and Backup Designated Router (BDR) begins. A Designated Router is used to reduce the number of adjacencies required in a broadcast network. That is, if no Designated Router is used, then each router must pair (form an adjacency) with each of the other routers. In this case, the number of required adjacencies is equal to the square of the number of routers (N^2). If a DR and BDR are used, the number of required adjacencies drops to 2 times the number of routers (2N). Currently, the Ixia ports are unable to simulate a DR or BDR.

Once the routers have initialized their adjacency databases, they synchronize their databases. This process involves one router becoming the master and the other becoming the subordinate. On Ethernet networks, the DR is always the master; on point-to-point networks, the router with the highest Router ID is the master.

Link State Advertisements (LSAs) are OSPF messages that describe an OSPF router's local environment. The simplest LSA Type is the router-LSA (RouterLinks LSA). Each router is required to generate exactly one of these LSAs to describe its own attached interfaces. If a network that consists of a single OSPF area is being simulated with only point-to-point links and there are no

Autonomous System Border Routers (ASBR), then this is the only type of LSA that is sent.

The subordinate asks the master for its LSA (Link State Advertisement) headers, which enables the subordinate to determine the following information:

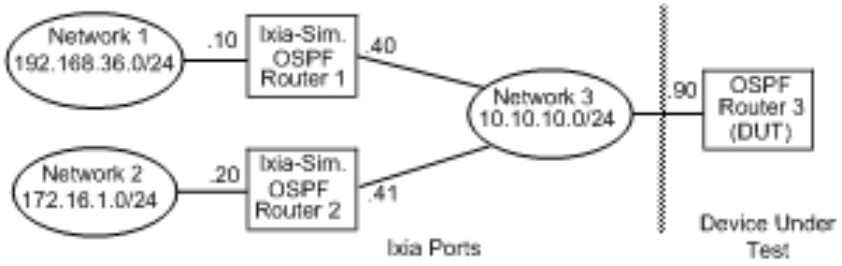
1. The subset of LSAs that the master holds, but that the subordinate does not have, **and**
2. The subset of LSAs that the master and subordinate both have, but which are more recent on the master.

The subordinate router then proceeds to explicitly query the master to send it each LSA from Steps (1) and (2). The subordinate sends an ACK to the master upon receipt of each LSA. The global Link State Database (LSDB) is constructed by each router, based on LSAs from all the other routers in the network.

Once this exchange process is complete, the routers are considered to have reached Full Adjacency, and each runs the link state algorithm to update its IP forwarding tables. The routers continue to exchange periodic HELLO packets, as keepalive messages, until a change occurs (for example, a link goes down or an LSA expires). OSPF routers continue to periodically exchange their LSAs every 30 minutes to ensure that they all hold identical LSDBs.

This section describes the programming of the Ixia hardware related to OSPF testing, as well as the theory of operation and protocol message formats. The Ixia hardware simulates multiple OSPF routers on multiple networks. For example, in Figure 3-1 on page 3-5 there are three networks and three routers.

Figure 3-1. Sample OSPF Network



The Protocol Server calls for the specification of router-network connections to be specified in a network-centric fashion. One specifies the network in terms of an Area ID and network mask. One specifies the routers in terms of the interface IP address on that network and Router ID, usually the lowest IP address for the router. For the sample OSPF network, in which Router 3 is the DUT, the three

networks are specified by their significant characteristics as shown in Table 3-2 on page 3-6.

Table 3-2. Sample OSPF Network Assignments

Network	Area ID	Network Mask	Router ID	Router Interface IP Address
1	192.168.36.0	255.255.255.0	192.168.36.10	10.0.0.40
2	172.16.0.0	255.255.255.0	172.16.0.20	10.0.0.41
3	10.0.0.0	255.255.0.0	10.0.0.40	10.0.0.40
			10.0.0.41	10.0.0.41
			10.0.0.90	10.0.0.90

Within this framework, Link State Advertisements (LSAs) may be issued from the perspective of any interface on any router. Any OSPF messages from the DUT Routers may be captured and analyzed in the normal manner.

OSPFv3

Open Shortest Path First Protocol Version 3 supports Internet Protocol version 6 (IPv6), as defined in RFC 2740. The 128-bit IPv6 addressing scheme has been accommodated in OSPF through the use of new LSA types.

Some of the differences between OSPFv2 (for IPv4) and OSPFv3 (for IPv6) are listed as follows:

- Changes to adapt to the IPv6 128-bit address size. No addresses are carried in OSPF packets or basic LSAs, but addresses are carried in certain LSAs.
- OSPFv3 operation is per Link, with the IPv6 concept of 'link' replacing the 'IP subnet' and 'network' terminology of OSPFv2.
- OSPVv3 supports multiple instances of the protocol per link, through 'Instance IDs.'
- LSA flooding scope is explicitly defined in the LS Type field of each LSA.
- Authentication is handled by the IPv6 protocol itself, rather than by the OSPF protocol. For this reason, Authentication information has been removed from the packet headers in OSPFv3.

Note: In OSPFv2, IPv4 addresses were used in many contexts besides IP source and destination addresses. For example, they were assigned as name identifiers for routers (RIDs). This naming convention for RIDs has been retained in OSPFv3.

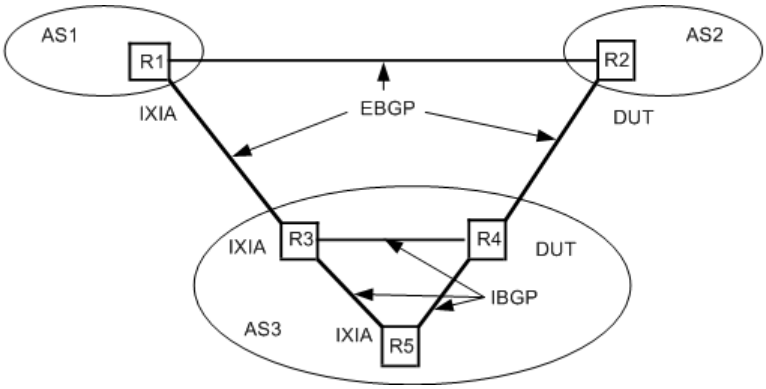
BGP4/BGP+

Border Gateway Protocol Version 4 (BGP-4) is the principal protocol used in the Internet backbone and in networks for large organizations. The BGP4 specification (RFC 1771) details the messages exchanged by BGP routers, as well as their meaning and usage. *BGP4 - Inter-Domain Routing in the Internet*, by John W. Stewart III is a descriptive reference on this protocol.

Internal Versus External BGP

The BGP4 protocol is used according to two sets of rules, depending on whether or not the two communicating BGP routers are within the same Autonomous System (AS). An AS is a collection of routers that implement the same routing policy and are typically administered by a single group of administrators. ASs connected to the Internet are assigned Autonomous System Numbers (ASNs) that are key to inter-domain routing. When BGP is used **between** two ASs, the protocol is referred to as EBGP (External BGP); when BGP is used **within** an AS it is referred to as IBGP (Internal BGP). Figure 3-2 on page 3-8 depicts the differences in topology between EBGP versus IBGP.

Figure 3-2. External BGP Versus Internal BGP



In the figure above, AS1, AS2, and AS3 are distinct Autonomous Systems. The Rns are routers in the various ASs. Routers on the links between ASs ‘speak’ EBGP, while the routers within AS3 ‘speak’ IBGP.

IBGP Extensions

In the original BGP4 specification (RFC 1771), all IBGP routers within an AS are required to establish a full mesh with each other. This leads to a lack of scalability which is solved by the introduction of two additional concepts: *route Reflection* and *Confederations*.

In route reflection, some routers in an AS are assigned the task of re-distributing internal routes to other internal AS routers. To prevent looping within an AS that uses route reflection, two concepts are important: the *originator-id* and *cluster-list* attributes.The originator-id is the identification of the router that originated a particular route. Routers within an AS propagate this information and refuse to send a route back to its originator. Even the use of route reflectors and originator-

ids can lead to scalability problems in an AS. The cluster-list concept helps this problem. A cluster consists of a reflecting router and its clients. A Cluster ID is the IP address of the reflecting router if there is one, or a configured number otherwise. A cluster-list is a constructed list, consisting of the cluster IDs of all of the clusters that a route has passed through. Each router refuses to send a route back to a cluster that has seen the route already.

In a confederation, an AS is divided into multiple sub-confederation subsets. Each sub-confederation is defined in terms of its own ASN and a list of routers. Routers within a sub-confederation are expected to fully mesh using IGP. Sub-confederations within a confederation speak a variant of EGP, called EIGP. Additional path attributes are used with a confederation to indicate paths that should not be propagated outside the confederation.

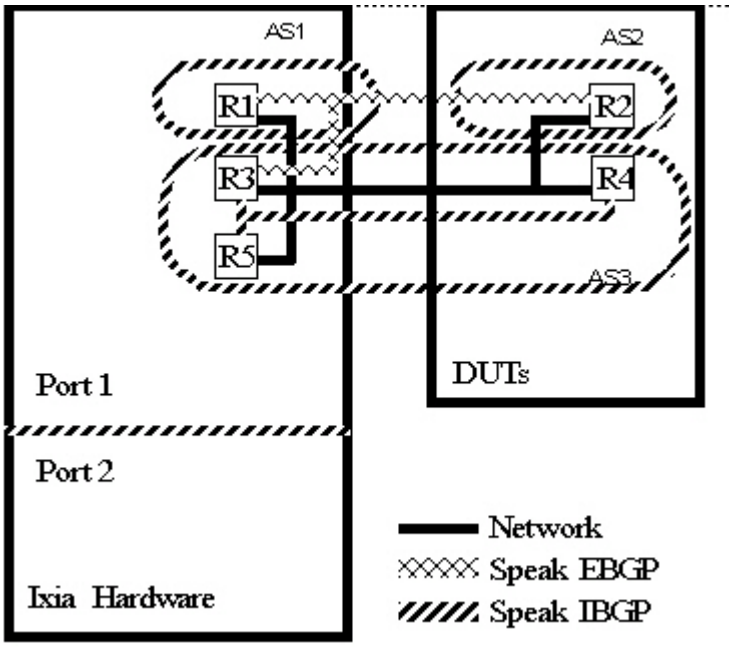
Communities

In deployment of BGP4 into a growing Internet environment, it became necessary to deal with certain routes in different manners not related to the strict routing of packets. The community attribute was invented to allow a route to be 'tagged' with multiple numbers, called communities. This is also referred to sometimes as *route coloring*.

BGP Router Test Configuration

The Ixia Protocol server implements an environment in which the Ixia hardware simulates multiple routers which speak IBGP and/or EBGP with one or more DUT routers. For example, in Figure 3-2 on page 3-8, the Ixia hardware emulates R1, R3, and R5 while the DUTs are R2 and R4. The following figure depicts the same setup based on the location of the simulated or actual router:

Figure 3-3. BGP Interconnection Environment

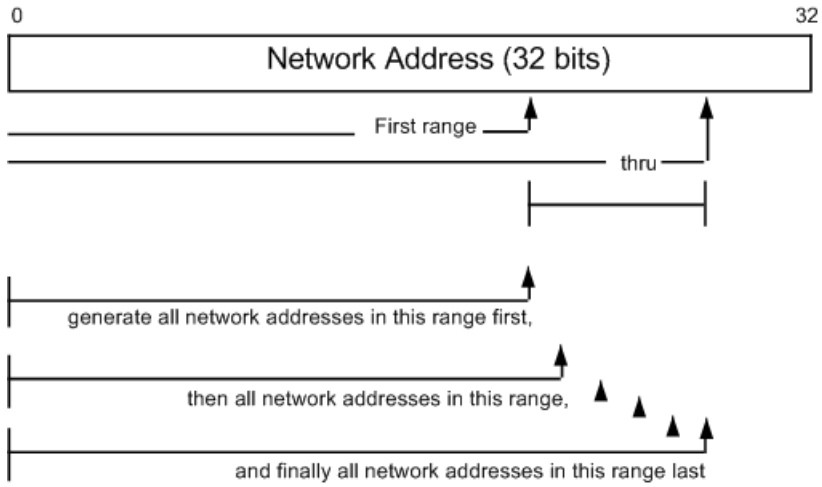


All of the routers are logically connected through appropriate networking hardware. The Ixia hardware is used to simulate three of the routers in two different ASs communicating with two routers being tested.

A single router emulated by the Ixia hardware is specified by a single IP address, and a number of emulated routers may be specified by a range of IP addresses. Each DUT router is identified by its IP address.

Messages may be sent between the emulated routers and the DUT routers when a connection is made and one of the two endpoints sends an OPEN message. Where the emulated routers and the DUT routers send their OPEN messages simultaneously, standard collision handling is applied. Thereafter, the emulated routers send a number of UPDATE messages to the DUT routers. The UPDATE messages contain a number of network address ranges (route ranges), also known as ranges of prefixes. The ranges of generated network addresses is illustrated in Figure 3-4 on page 3-10.

Figure 3-4. Generation of Network Addresses in BGP UPDATE Messages



A designated number of network addresses are generated with network Mask Width with the *From* through *To* values. Table 3-3 on page 3-11 shows some examples of generated addresses. Network Addresses are generated by starting with the First Route and *From* mask width up to, but not including 224.0.0.0. (127.*.*.* is also skipped). If the requested number of network addresses has not been generated before 224.0.0.0 is reached, then the next mask length is used with the First Route to generate network addresses.

Table 3-3. Examples of Generated BGP Routes (Network Addresses)

First Route	Mask Width From	Mask Width To	Iterator Step	Number of Routes	Generated BGP Routes (Network Addresses)
192.168.36.0	24	26	1	(14,378,756 Max.)	192.168.36.0/24 192.168.37.0/24 192.168.38.0/24 ... 223.255.255.0/24 (224.0.0.0+ skipped) 192.168.36.0/25 192.168.36.128/25 192.168.37.0/25 ... 223.255.255.128/25 (224.0.0.0+ skipped) 192.168.36.0/26 192.168.36.64/26 192.168.36.128/26 ... 223.255.255.192/26
204.197.56.0	24	24	10	4	204.197.56.0/24 204.197.66.0/24 204.197.76.0/24 204.197.86.0/24

All of the generated network addresses are associated with a set of attributes that describes routing to these generated network addresses and associated features.

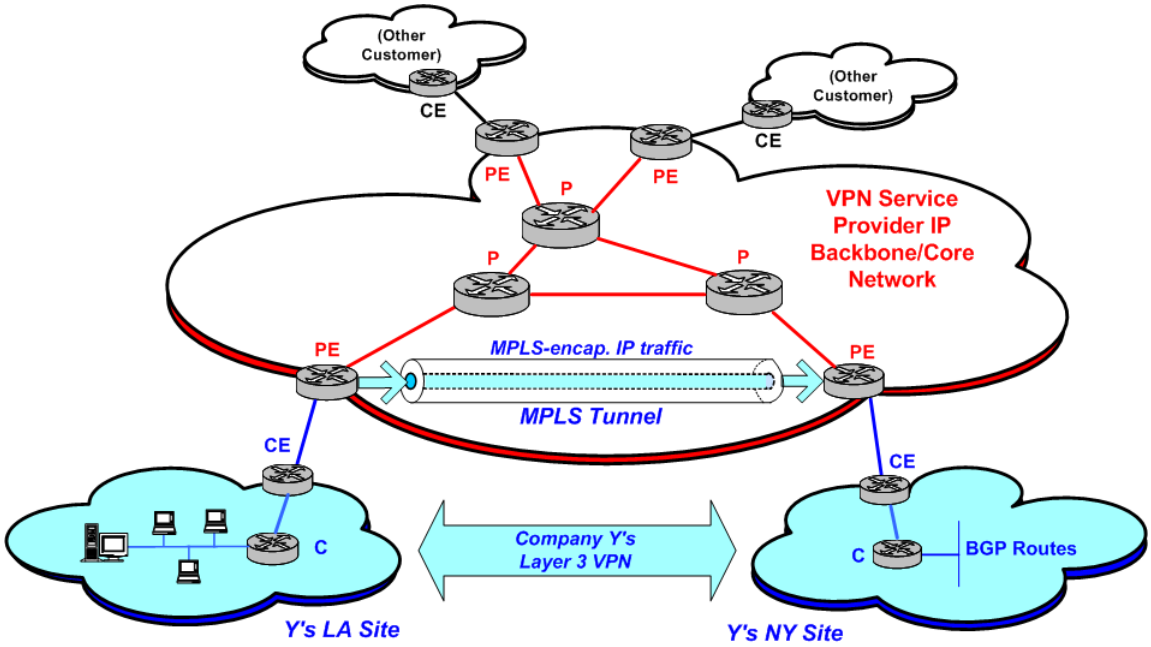
Only one route can be added per UPDATE message, but a variable number of *withdrawn* routes may be packed into each UPDATE message. The packing is randomly chosen across a range of a number of routes. The time interval between UPDATE messages is configurable, in units of milliseconds.

A BGP4 network condition called ‘flapping’ can be emulated by the protocol server on an Ixia port. In the Link flapping emulation, a peer BGP router appears to be going offline and online repeatedly, which is accomplished on the Ixia port by alternate disconnects and reconnects of the TCP/IP stack. In the Route flapping emulation, BGP routes are repeatedly withdrawn, and then re-advertised, in UPDATE messages.

BGP L3 VPNs

L3 Virtual Private Networks (VPNs) over an IP backbone (at Layer 3 of the OSI model), may be provided to the customers of a Service Provider (SP), providing connectivity between two or more sites owned by the customer. L3 VPNs are independent of the Layer 2 protocol. While MPLS handles the packet forwarding in the backbone/core, the BGP protocol provides a means of advertising external routes/network addresses across that backbone between sites. IETF Internet Draft 'draft-ietf-ppvpn-rfc2547bis-01.txt,' the proposed successor to RFC 2547, covers the VPN architecture designed for use by private service providers. A simplified example of a BGP L3 VPN topology is shown in Figure 3-5 on page 3-12.

Figure 3-5. Simplified BGP L3 VPN Diagram



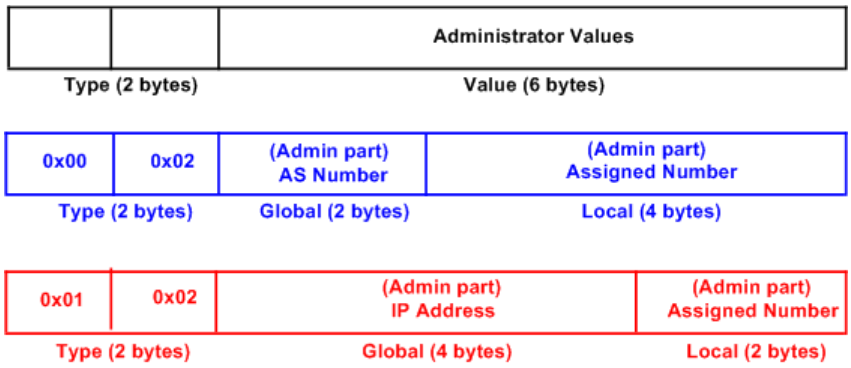
The term *site* refers to a customer/client site, which consists of a group of inter-connected IP devices, usually in one geographic location. A Customer Edge (CE) device, typically a router, connects the site, through a data link connection, to a Provider Edge (PE) router—an entry point to the service provider's backbone. The PE-to-CE routing protocols may be static routing, or a dynamic protocol such as eBGP or RIPv2.

Provider (P) network core routers, 'transparently' carry the IP traffic across the internal core between CE routers. CEs and Ps are not 'VPN-aware' devices. CE devices are considered as belonging to a only one site, but that site may belong to multiple VPNs. A VPN Routing and Forwarding table (VRF) on a PE consists of an IP routing table, a forwarding table, and other information on the set of interfaces in the VPN. The VRF generally describes a VPN site's routing information, and a PE may maintain multiple VRFs, one for each connected customer site. See *L3 VPN VRFs* on page 3-14 for additional information on VRFs.

Layer 3 VPN sites are identified by a Route Target (RT). A route target is based on the mechanism proposed in the IETF draft for the 'BGP Extended

Communities Attribute.' An 8-byte route target is common to all route ranges that belong to a single L3 site. Route targets are defined for individual VPN route ranges. The formats for Route Targets (RTs) are shown in Figure 3-6 on page 3-13.

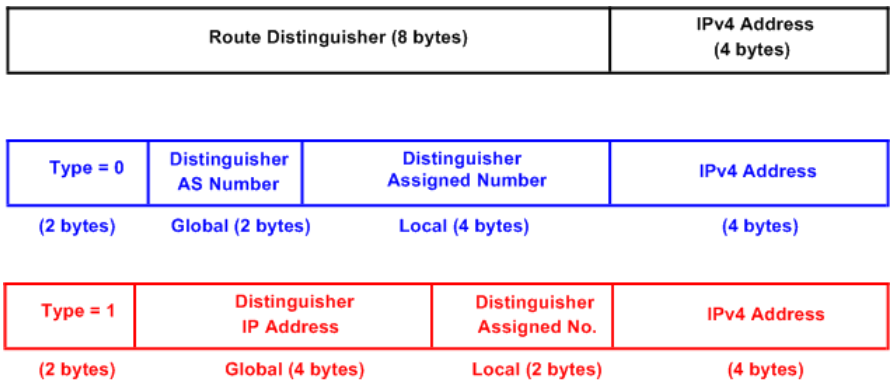
Figure 3-6. Route Target Formats (BGP Extended Community Types)



BGP VPN-IPv4 Address Formats

Globally unique 12-byte VPN-IPv4 prefixes are created by a PE router. This includes configuration of the 8-byte VPN Route Distinguishers (RDs). It should be noted that BGP IPv4 routes and VPN -IPv4 routes are considered noncomparable; VPN-IPV4 addresses can be used only within the VPN service provider network.The route distinguishers are used by PE routers to associate routes with the path to a particular CE site router in a VPN. Each route can only have one RD. The formats of the RDs are shown in Figure 3-7 on page 3-13.

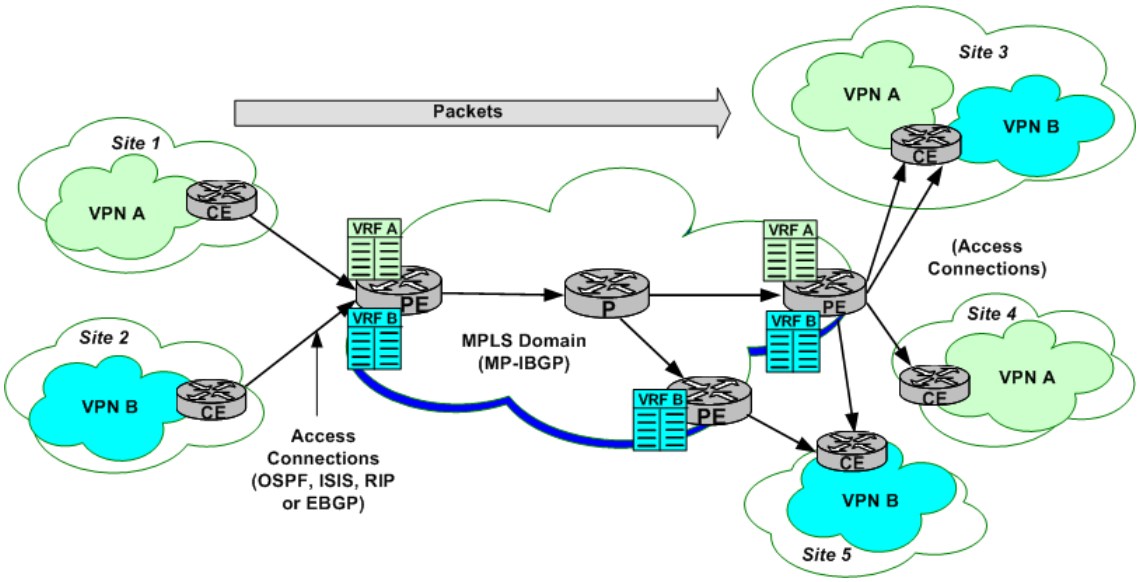
Figure 3-7. VPN-IPv4 Address Formats (with Route Distinguishers)



L3 VPN VRFs

For Layer 3 Virtual Private Network (L3 VPN) configurations, the Provider Edge (PE) routers maintain routing tables for each VPN that they participate in, termed VPN Routing and Forwarding tables (VRFs). The VRFs are populated with routes received from both the directly attached and remote Customer Edge (CE) routers. Each entry in the VRF is called a VPN Forwarding Instance (VPI). VRFs and CEs are not required to be configured on a one-to-one basis, although this is the typical situation. An example of the possible relationships between VRFs and CEs is shown in Figure 3-8 on page 3-14.

Figure 3-8. L3 VPN VRF Example



RIP

The Routing Information Protocol (RIP) is an interior routing protocol. It is the oldest and most frequently used of the LAN routing protocol. RIP routers broadcast or multicast to each other on a regular basis and in response to REQUEST packets. RIP routers incorporate routing information received from their neighbors into their own routing table and forward them on to other neighbors. Two distinct versions of RIP exist: version 1 and version 2. Both IPv4 and IPv6 are supported.

As implemented by the Protocol Server, each Ixia port is capable of simulating one or more routers at distinct addresses. Routing tables for the simulated routers are configured by you and sent out at regular intervals, with a configurable randomizing factor. Either version 1 or version 2 packet formats may be sent through multicast or broadcast (for compatibility with version 1 routers). Received packets may be filtered for version 1 and/or 2 compatibility.

The current implementation of the Protocol Server uses Split Horizon with Space Saver as its update mode, which receives, but not process RIP broadcasts heard from DUT routers. That is, it does **not** incorporate received information into its own table, but rather always broadcast the same routing table. Future versions will offer Split Horizon, Split Horizon with Poison Reverse, and Silent modes of update.

The Protocol Server, however, responds to REQUEST packets that it receives. Two types of requests are processed:

- Request for all routes: The Protocol Server sends the same routing table that it sends at regular intervals back to the requestor.
- Request for specific routes: The Protocol Server fills in the requested information in the received packet and send it back to the requestor.

RIP Overview

The Routing Information Protocol (RIP) is an interior gateway routing protocol (IGP) and uses a Distance Vector Algorithm. It is the oldest and most frequently used of the LAN routing protocols. RIP routers broadcast or multicast to each other on a regular basis and in response to REQUEST packets. RIP routers optionally incorporate routing information received from their neighbors into their own routing table and forward it on to other neighbors.

Note: For information on **RIPng** (RIP-Next Generation), based on IPv6, see *RIPng* on page 3-16.

As implemented by the Protocol Server, each Ixia port is capable of simulating one or more routers with separate addresses. Routing tables for the simulated routers are configured by you and sent out at regular intervals, with a configurable randomizing factor. Either Version 1 or Version 2 packet formats may be sent through multicast or broadcast (for compatibility with Version 1 routers). Received packets may be filtered for Version 1 or Version 2 compatibility.

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- Request for all routes: The Protocol Server sends the same routing table that it sends at regular intervals back to the requestor.
- Request for specific routes: The Protocol Server fills in the requested information in the received packet and send it back to the requestor.

RIPng

Routing Information Protocol - Next Generation (RIPng) is specified for use with IPv6 in RFC 2080. Like the IPv4 version of RIP, this routing protocol is based on a Distance Vector algorithm. RIPng routers compare information for various routes through an IPv6 network, especially the information related to the RIPng metric. Due to the limited number of allowed hops, this protocol is used in small- to moderate-sized networks. The valid metric range is from 1 to 15 (hops). The metric values of 16 and above are defined as ‘infinity’ and are considered unreachable.

An RIPng router is assumed to have interfaces to one or more directly-connected networks. Each router maintains a routing table, with one entry for every reachable destination in the RIPng network. Each routing table entry contains a minimum of:

- IPv6 destination prefix(es)
- total metric cost for the path to the destination(s)
- IPv6 address of the next hop router
- a ‘route change flag’
- timers

As a UDP-based protocol, the RIPng routing process functions on UDP well-known port number 521 (the ‘RIPng port’), on which datagrams are sent and received. The RIPng port supports the following:

- Receives all communications received from another router’s RIPng process.
- Sends all RIPng routing update messages.
- Unsolicited routing update messages specify this port as the source and destination.
- Responses to request messages are sent to the originating UDP port.
- Specific requests need not come from the RIPng port, but the destination on the targeted device must be the RIPng port.

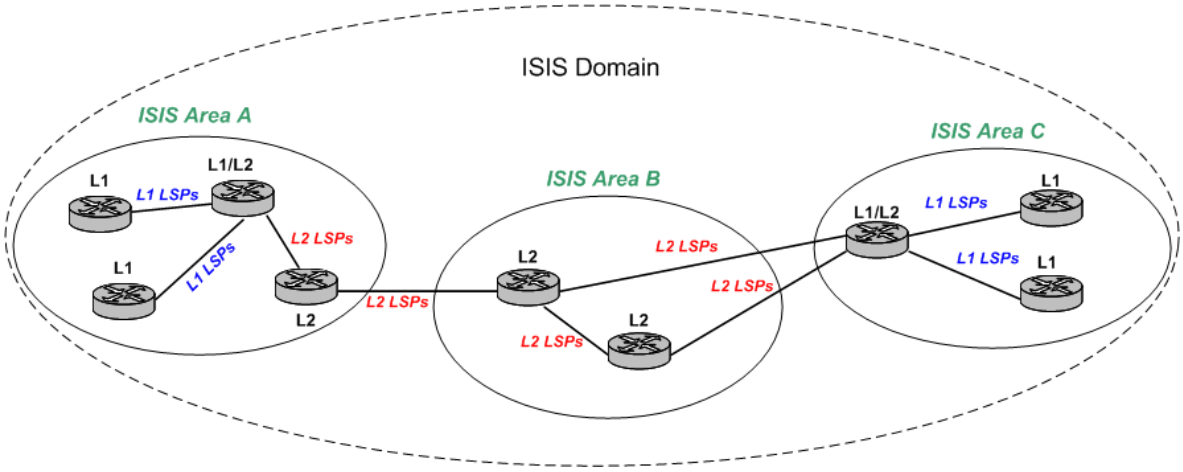
ISISv4/v6

The Intermediate System to Intermediate System (ISIS) routing protocol was originally designed for use with the OSI Connectionless Network Protocol (CLNP) and was defined in ISO DP 10589. It was later extended to include IP routing in IETF RFC 1195. When routing for OSI and IP packets (defined in ISO/IEC 10589:1992(E)) is combined in this way, the protocol is referred to as Integrated ISIS or Dual ISIS. In addition, RFC 2966 extends the distribution of routing prefixes among ISIS routers, and IETF DRAFT draft-ietf-isis-ipv6-05 adds IPv6 routing capability to the protocol.

ISIS Topology

ISIS areas are administrative domains which contain ISIS routers, have one or more private networks, and may share networks with other areas. The example shown in Figure 3-9 on page 3-17 consists of a theoretical ISIS topology. Note that, as shown in this diagram, all ISIS routers are considered to reside entirely **within** an area, unlike some other protocols such as OSPF, where routers can reside at the edges of areas and domains.

Figure 3-9. ISIS Topology



One or more Area IDs are associated with an area. Most areas only require one ID during steady state operation, but up to three IDs may be needed during the process of migrating a router from one area to another. In most cases, the maximum number of area IDs is set to three.

ISIS routers can be divided into three categories, as follows:

- **Level 1 (L1)**: These routers can connect only to L1 or L1/L2 routers within their own area (intra-area). They have no direct connection to any other ISIS area.
- **Level 2 (L2)**: These routers can connect only to other L2 routers outside their area, or to L1/L2 routers within their own area. They are used as backbone routers in the routing domain, to connect ISIS areas.

- **Level 1/2 (L1/L2)**: These routers have separate interfaces which can connect to both L1 routers within their own area and L2 routers in other areas.

Entirely separate routing tables are maintained for Level 1 and Level 2 ISIS information, even within L1/L2 routers. All L1s within an area maintain identical databases. All L2s within a domain maintain identical databases.

ISIS Processing

Many OSI concepts are necessary for describing ISIS. The following terms are important to the following discussion:

- IS - Intermediate System. An ISIS router is an IS.
- ES - End System. A host is an ES. (Note: The Ixia hardware does not currently simulate End Systems.)
- PDU - Protocol Data Unit. PDUs contain messages used for the ISIS protocol. The following PDUs are used in IS-IS communications:
  - IIH - IS-to-IS Hello PDU. This message is multicast over broadcast networks, or unicast on point-to-point links, between ISs to discover neighbors and maintain ISIS state.
  - LSP - Link State PDU. This message holds the significant part of the routing table sent between ISIS routers.
  - SNP - Sequence Number PDU. This message is used to request LSPs and acknowledge receipt of LSPs. Two types are used depending on the network type:
    - CSNP - Complete SNP. In broadcast networks, these are sent by the Designated Router in an area. On point-to-point connections, CSNPs are used for initialization. A CSNP contains a complete description of the LSPs in the sender's database.
    - PSNP - Partial SNP. On broadcast networks, PSNPs are used to request LSPs. On point-to-point connections, PSNPs are used to acknowledge receipt of LSPs. On both types of networks, PSNPs are used to advertise newly learned LSPs or purge LSPs. A PSNP contains a subset of the received records.

ISIS routers maintain knowledge of each other by exchanging Hello PDUs at regular, configured *Hello intervals*. A router is considered down if it does not respond within a separately configured *Dead interval.*

ISIS routers update each other using Link State PDUs (LSPs) at a regular interval of 30 minutes. The LSP header contains the Remaining Lifetime for the LSP, a Sequence Number, and a checksum. Each LSP contains information about a router's connection to local networks, plus a metric related to each network. ISO DP 10589 defines four types of metrics: default, delay, expense, and error.

In a Broadcast/LAN network, the Designated Router sends a Complete Sequence Number PDU (CSNP). In a Point-to-Point network, the receiving router sends a Partial Sequence Number PDU (PSNP).

In the ISIS protocol, for each of the levels (L1 or L2), one of the routers is elected as the Designated IS, based on priority values assigned to each interface as part

of Hello PDU processing. The Ixia Protocol Server does not support the role of DR, so to ensure that it is not elected by its ISIS peers each Ixia-simulated ISIS router has a default priority of ‘0,’ indicating its unwillingness to be the Designated IS.

ISIS Addresses

Due to the OSI derivation of the ISIS protocol, each ISIS router has an OSI NET address of 8 to 20 octets in length. The NET address consists of two parts: an Area ID and a System ID. The Area ID has a number of different formats defined in OSI specifications. The System ID may be from 1 to 8 octets in length. The default System ID length defaults to 6 octets and must be the same length for every router in the domain. The System ID is unique within its ISIS **area** for Level 1, or unique within the ISIS routing **domain** for Level 2 or Level 1/2. Two types of network connections are supported: broadcast and point-to-point. In a broadcast network, each interface on an ISIS dual-mode router must have an IP address and mask.

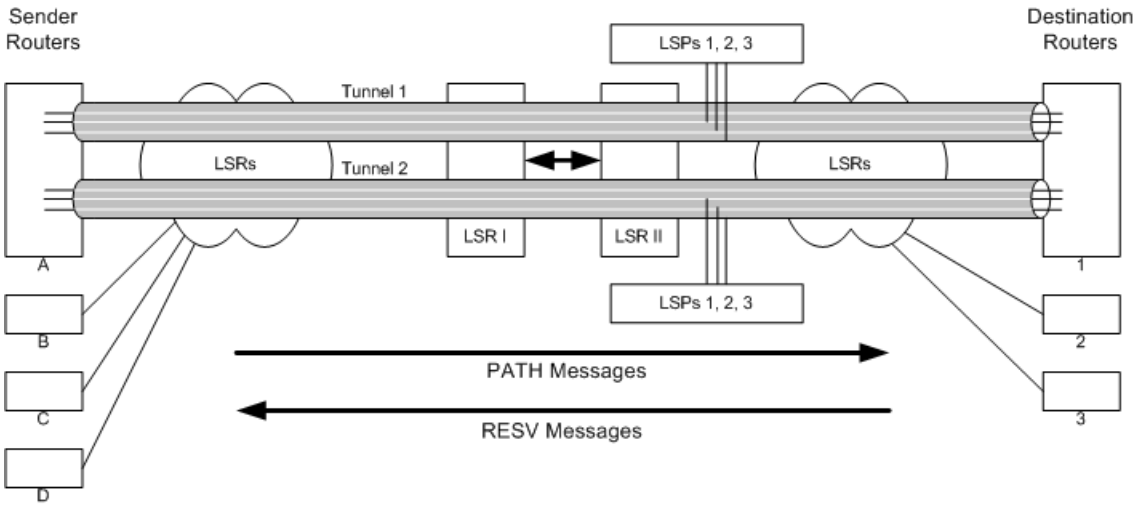
RSVP-TE

The Ixia protocol server implements a part of the Resource Reservation Protocol (RSVP) used for Traffic Engineering (TE). This subset of the RSVP protocol, referred to as RSVP-TE, is used in the process of constructing a path through a sequence of MPLS-enabled label switched routers (LSRs), while reserving necessary bandwidth resources. The use of an internal gateway routing protocol (IGP), such as OSPF, is also required to automatically determine the 'next hop' router.

Multi-Protocol Label Switching (MPLS) allows rapid forwarding of packets across a sequence of routers, without time-consuming examination of the packet contents at each hop. Label switching has been used extensively for ATM traffic, where overhead bytes for each 'cell,' or packet, of data constitute a large percentage of the overall data transmitted. The addition of a 'label' value to the header information in each cell or packet supplies the only forwarding information required to transit the MPLS domain. Based on information in its forwarding table, each LSR replaces (swaps) the incoming label with a new one which directs the packet to the next hop.

The most important output from an RSVP-TE setup session is the set of *MPLS labels*, which are used by the MPLS-enabled routers along the path to efficiently forward network traffic. The operation of RSVP-TE is shown in Figure 3-10 on page 3-20.

Figure 3-10. RSVP-TE Overview



Through the use of RSVP-TE message exchanges, the router at the entry to the MPLS domain, also known as an Ingress LSR, initiates the creation of a dynamic 'tunneled' pathway to the Egress LSR, the router at the exit side of the MPLS domain. Packets which pass through this 'tunnel' are essentially 'protected' from the extensive packet processing normally imposed by each router it traverses. Once this special pathway or Label Switched Path (LSP) is established, the router can **forward,** rather than route, packets across the domain, saving considerable

processing time at each intermediate LSR (Transit LSR). The resulting tunneled pathway is known as an LSP Tunnel. The traffic flows through an LSP Tunnel are unidirectional. To establish bidirectional traffic through the MPLS domain, a second LSP Tunnel must be created in the opposite direction.

An LSP Tunnel is defined by a Destination Address (the IP address of the Egress LSR), and a Tunnel ID. At a finer level of granularity are LSP IDs. Essentially, these LSP IDs can serve to provide a set of aliases for alternate hop-by-hop paths between a single pair of Ingress and Egress LSRs, and therefore exist within the same LSP Tunnel.

Note: Ingress LSRs and Egress LSRs are also known as Label Edge Routers (LERs).

Two principal RSVP-TE message types are used to establish LSP Tunnels:

- PATH message. A PATH message is generated by the ingress router and sent toward the egress router. This is termed the *downstream* direction. This PATH message is a request by the sending LSR for the establishment of an LSP to the egress router. Each LSR in the path to the destination router digests the PATH message and does one of three things:
  - If the LSR cannot accommodate the request, it rejects the request by sending a PATH_ERR message back to the source indicating the nature of the rejection.
  - If the LSR is not the egress router, it sends a PATH message to the next LSR toward the destination router.
  - If the LSR is the egress router, it should respond with a RESV message back to its most recent neighbor.
- RESV message. A RESV message is generated by the egress router and sent over the reverse path that the PATH messages took. This is termed the *upstream* direction.

An additional *HELLO* message is used between neighbor LSRs to ensure that LSRs are alive. This allows for quick tunnel replacement in the case of link or router failure.

A set of labels is passed in the RESV messages sent upstream from the egress to the ingress router. A label is sent from one LSR to its upstream neighbor telling the upstream router which label to use when later sending downstream traffic.

Three scenarios are currently supported to test MPLS/RSVP-TE on a DUT using Ixia equipment:

1. The DUT acts as the Ingress LSR, and the Egress LSR is simulated by an Ixia port.
2. The DUT acts as the Egress LSR, and the Ingress LSR is simulated by an Ixia port.
3. The DUT acts as a Transit/Intermediate LSR, and the Ingress and Egress LSRs are simulated by Ixia ports.

PATH Messages

PATH messages contain a number of objects which define the tunnel to be established. These are shown in Table 3-4 on page 3-22.

Table 3-4. RSVP-TE PATH Message Objects

Object	Contents	Usage
SESSION		Describes the destination router and associates a tunnel ID with the session.
	tunnel endpoint	The destination router's IP address.
	tunnel ID	A unique LSP tunnel ID.
SENDER_TEMPLATE		The description of the sender.
	tunnel sender address	The sender router's IP address.
	LSP ID	A unique LSP ID.
LABEL_REQUEST		Asks all the LSRs to send back label values through RESV messages.
SENDER_TSPEC and ADSPEC		Both of these objects deal with bandwidth and other QoS requirements for the path.
TIME_VALUES		Timing values related to the refresh of tunnel information.
	refresh interval	The interval between messages.
EXPLICIT_ROUTE		Allows the sender to request that the LSP tunnel follow a specific path from ingress to egress router. See *Explicit_Route* on page 3-22 for more details.
SESSION_ATTRIBUTE		Other attributes associated with the session: tunnel establishment priorities, session name, and optionally resource affinity.
RSVP_HOP		Describes the immediate upstream router's address to the downstream router.

Explicit_Route

An explicit route is a particular path in the network topology. Typically, the explicit route is determined by a node with the intent of directing traffic along that path. An explicit route is described as a list of groups of nodes along the explicit route. In addition to the ability to identify specific nodes along the path, an explicit route can identify a group of nodes that must be traversed along the path. Each group of nodes is called an *abstract node*. Thus, an explicit route is a specification of a set of abstract nodes to be traversed.

There are three types of objects in an explicit route:

- IPv4 prefix
- IPv6 prefix
- Autonomous system number

Each node has a *loose* bit associated with it. If the bit is not set, the node is considered *strict*. The path between a strict node and its preceding node may only include network nodes from the strict node and its preceding abstract node. The path between a loose node and its preceding node may include other network nodes that are not part of the strict node or its preceding abstract node.

RESV Message

The RESV message contains object that indicate the success of the PATH request and the details of the assigned tunnel. These are shown in Table 3-5 on page 3-23.

Table 3-5. RSVP-TE RESV Message Objects

Object	Usage
SESSION	Indicates which session is being responded to.
TIME_VALUES	As in the PATH message but from the downstream LSR to the upstream LSR.
STYLE	The type of reservation assigned by the egress router. This relates to whether individual tunnels are requested for each sender-destination connection or whether some connections may use the same tunnel.
FILTER_SPEC	The sender router's IP address and the LSP ID.
LABEL	The label value assigned by the downstream router for use by the upstream router.
RECORD_ROUTE	If requested, the complete route from the destination back to the source. The contents of this object include the IP addresses in either v4 or v6 format of all the LSRs encountered in the formation of the LSP, and optionally the labels used at each step. Each LSR on the upstream path perpends its own address information.
RESV_CONF	If present, it indicates that the ingress router should send a RESV_CONF message in response to the destination to indicate that the tunnel has been completely established.

Other Messages

Several additional messages are used in RSVP-TE, as explained in Table 3-6 on page 3-24.

Table 3-6. Additional RSVP-TE Messages

Message	Usage
PATH_ERR	Any LSR may determine that it cannot accommodate the tunnel requested in a PATH message. In this case it sends a PATH_ERR message back to the sender.
PATH_TEAR	When a sender router determines that it wants to tear down a tunnel, it sends a PATH_TEAR message to the destination router.
RESV_ERR	If a router cannot handle a reservation, it sends a RESV_ERR back to the destination router.
RESV_TEAR	When a destination router determines that it wants to tear down a tunnel, it sends a RESV_TEAR message upstream to the source router.
RESV_CONF	When requested, a sender router responds to the destination router with a RESV_CONF message to indicate that a complete tunnel has been successfully established.

RSVP-TE Fast Reroute

RSVP-TE Fast Reroute allows to configure backup LSP tunnels to provide local repair/protection ONLY for **explicitly-routed** LSPs/LSP tunnels, termed *protected LSPs* as described in IETF DRAFT draft-ietf-mpls-rsvp-lsp-fastreroute-03.

An example diagram of a backup scenario for rerouting around a downed link, using an LSP Detour, is shown in Figure 3-11 on page 3-25. Figure 3-12 on page 3-25 shows an example diagram for a backup scenario to reroute around a downed node, using an LSP Detour.

Figure 3-11. RSVP-TE Fast Reroute Backup Link (Detour) Example

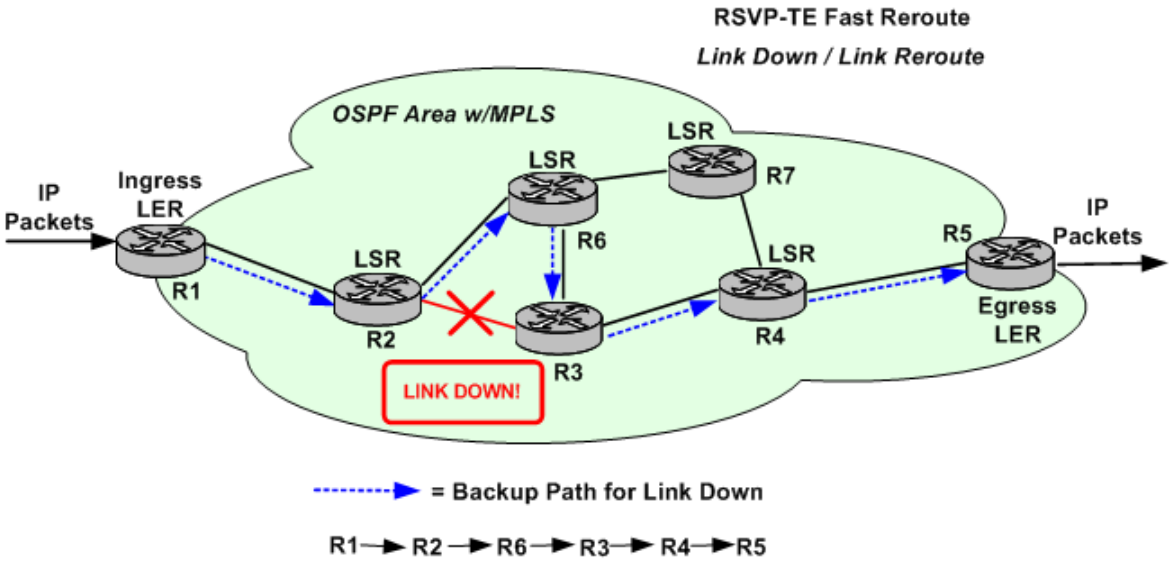
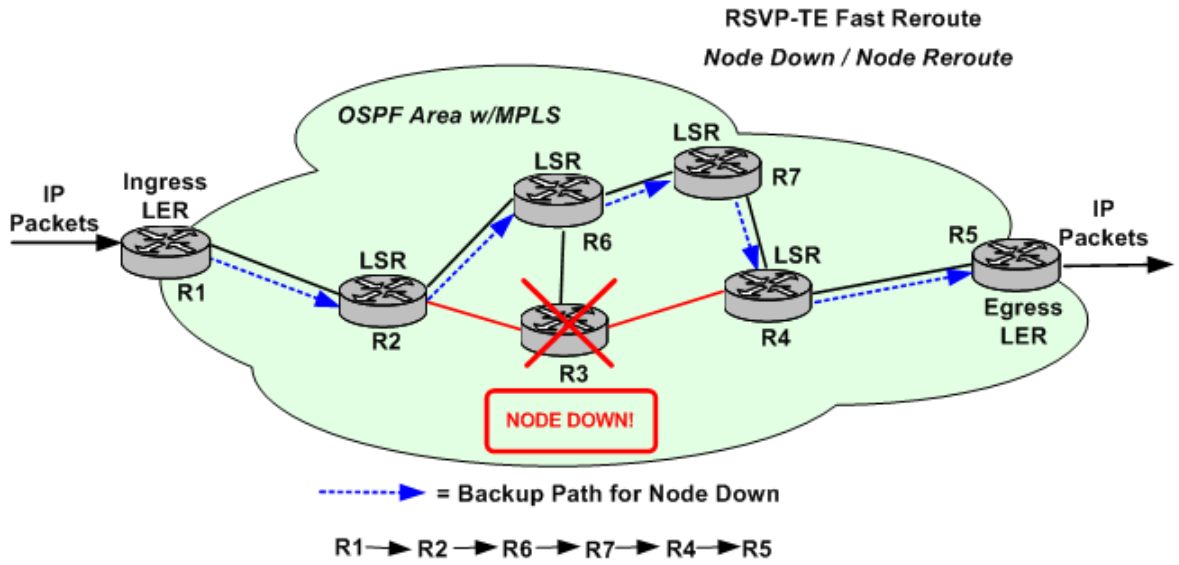


Figure 3-12. RSVP-TE Fast Reroute Backup Node (Detour) Example



The one-to-one backup method is based on including a DETOUR object in the Path message. The head-end router, the Point of Local Repair (PLR), sets up a separate detour LSP for each LSP it protects. For the Facility backup method, the PLR sets up a tunnel to protect multiple LSPs simultaneously, by using the MPLS label stack.

Ixia Test Model

The Ixia test process is designed so as to fully exercise RSVP functionality in MPLS routers. An Ixia port can simulate any number of LSR routers at the same time. Each router operates in an ingress or egress mode. In the following discussion, LSRs I and II refer to Figure 3-10 on page 3-20:

- Ingress mode: LSRs I and II are termed a neighbor pair, where LSR I is the upstream router being simulated and LSR II is its immediate downstream neighbor. The Ixia port generates the PATH and HELLO messages that LSR I would send. LSR II is the Device Under Test (DUT) and may be an egress router or be connected to other LSRs, as shown in the figure.
- Egress mode: the Ixia port simulates LSR II while LSR I is the DUT. The Ixia port interprets PATH messages that it receives to determine if they are directed for any of the defined destination routers. If that is the case, it responds with appropriate RESV messages.

If requested, HELLO messages are generated and responded to in either mode.

When the Ixia port operates in Ingress mode, it attempts to set up LSP tunnels for each combination of sender router and destination router, using any number of LSP tunnels and any number of LSP IDs for each LSP tunnel. Thus the number of PATH messages that the Ixia port attempts to generate for each refresh interval is:

# of sender routers
x # of destination routers
x # of LSPs
x # of LSP tunnels

The protocol server records all labels and other information that it receives on behalf of its simulated routers and displays those in a convenient format.

LDP

The Label Distribution Protocol (LDP) version 1, defined in RFC 3036, works in conjunction with Multi-Protocol Label Switching (MPLS), to efficiently 'tunnel' IP traffic across backbone topologies between Label Switching Routers (LSRs).

MPLS forwards packets based on added labels, so IP routing table lookups are not required along the length of the tunnel. RFC 3031 defines Forwarding Equivalence Classes (FECs) for use with MPLS, for purposes such as Quality of Service (QoS). LDP utilizes this option, assigning an FEC to every Label Switched Path (LSP) it sets up.

The LDP protocol creates peer sessions through a bidirectional exchange of messages, which include label requests and labels. While the initial Hello messages are based on UDP and sent to well-known port '646,' all other messages are based on TCP.

The following global timers can be configured: Hello Hold timer, Hello Interval timer, KeepAlive Hold timer, and KeepAlive Interval timer. The values for these timers can be entered by you, but the final values are negotiated during the Discovery and Session setup processes. When the LDP remote peer has a timeout value which is lower than the one configured for the local LDP router, the lower value is used by both peers.

Virtual Circuit (VC) Ranges of MAC Addresses can be created to simulate Virtual Private LAN Services (VPLS), where L2 PDUs can be carried over VC LSPs, which, in turn, are carried over MPLS. This creates a 'bridged,' Ethernet Layer Two Virtual Private Network (Ethernet L2VPN). Refer to IETF DRAFT draft-lasserre-vkompella-ppvpn-vpls-03, which defines the VC Type - Ethernet VPLS, and also discusses the use of MPLS transport tunnels by pseudowires (PWs).

A pseudowire is a logical link through the tunnel, made up of two parallel VC LSPs using the same VC Identifier (VCID), as shown in Figure 3-13 on page 3-27, and in more detail in Figure 3-14 on page 3-28.

Figure 3-13. LDP VPLS Example

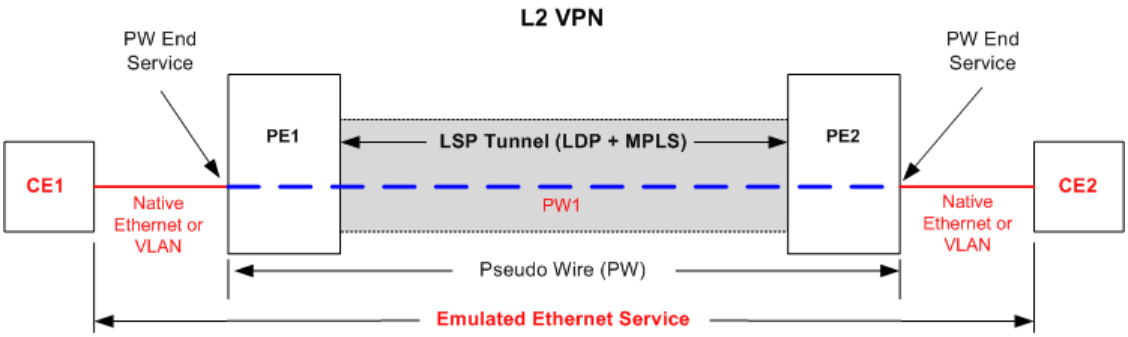
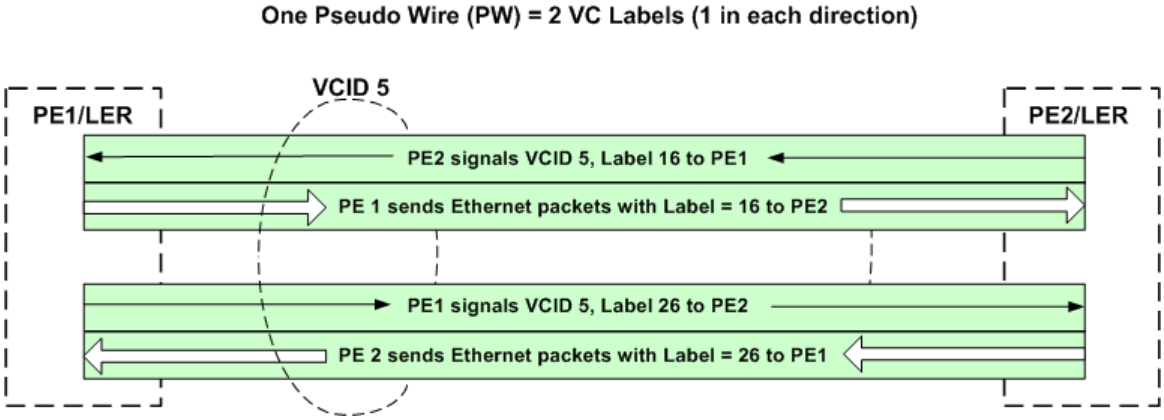


Figure 3-14. LDP VPLS Pseudowire Diagram



MLD

The Multicast Listener Discovery (MLD) protocol is integral to the operation of Internet Protocol Version 6 (IPv6). MLDv1 is defined by RFC 2710, while MLDv2 is defined by RFC 3810. The MLD operations are based on operations similar to the Internet Group Management Protocol (IGMP) that supports IPv4. MLDv2 corresponds to IGMPv3. Both versions are supported by the protocol server.

An IPv6 router uses MLD to: (1) discover multicast listeners (nodes) on the directly attached links, and (2) find out which multicast addresses those nodes have interest in. In MLDv2, nodes can indicate interest in listening to packets that are sent to a specific multicast address from a filtered group of source IP addresses. This filtering can be based on ‘all but’ (Excluding) or ‘only’ (Including) certain source addresses. Host nodes can only be multicast ‘listeners,’ while the multicast routers can act as routers or listeners.

PIM-SM/SSM-v4/v6

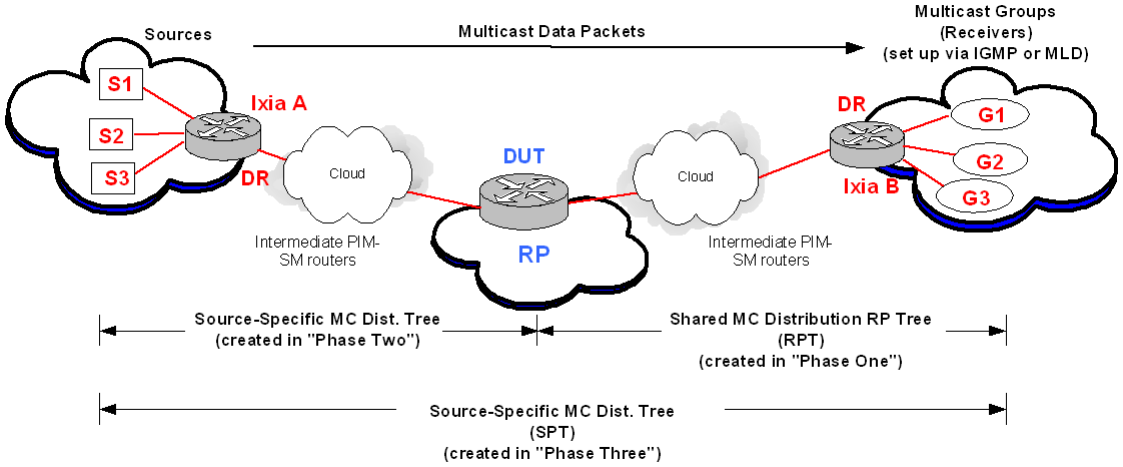
Protocol Independent Multicast - Sparse Mode (PIM-SM) Version 2 protocol is designed for multicast routing, and is defined in RFC 2362. IETF DRAFT draft-ietf-pim-sm-v2-new-06.txt is being designed to obsolete RFC 2362.

There is one Rendezvous Point (RP) per multicast group, and this router serves as the root of a unidirectional *shared* distribution tree whose 'leaves' consist of multicast receivers. In addition, PIM-SM can create an optional shortest-path tree for an *individual* source (where the source is the root). The term *upstream* is used to indicate the direction toward the root of the tree; *downstream* indicates the direction away from the root of the tree. The address of the RP can be configured statically by an administrator, or configured through a Bootstrap router (BSR) mechanism.

PIM-SM can use two sources of topology information to populate its routing table, the Multicast Routing Information Base (MRIB): unicast or multicast-capable. In a LAN where there are multiple PIM-SM routers and directly-connected hosts, one of the routers is elected as Designated Router (DR) to act on the behalf of the hosts.

The diagram in Figure 3-15 on page 3-29 shows a simplified PIM-SM test setup using Ixia ports.

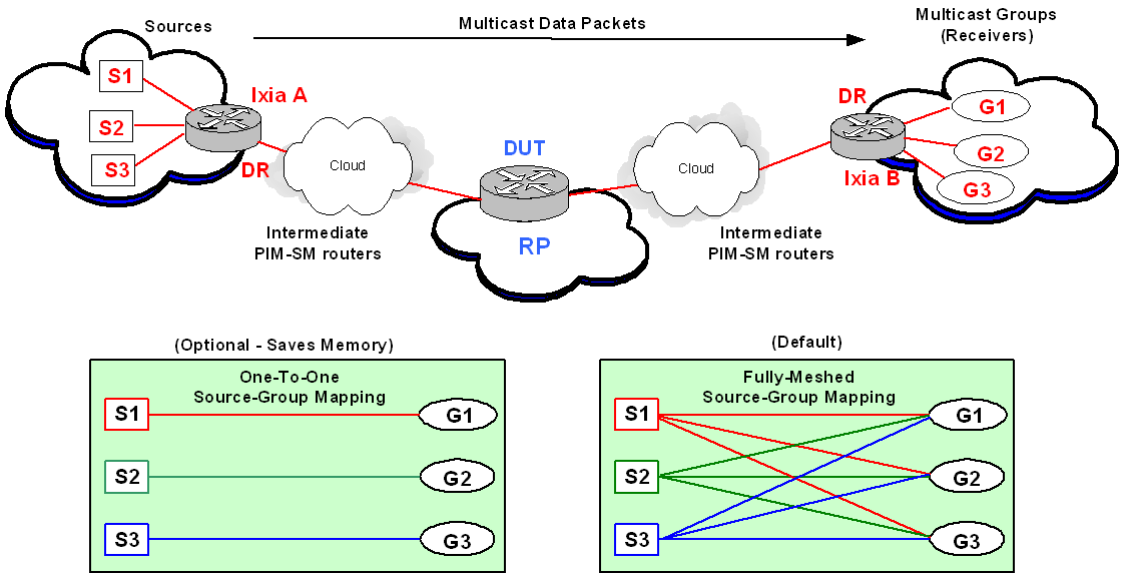
Figure 3-15. PIM-SM Diagram



PIM-SM Source-Group Mapping

PIM-SM Source-Group mapping involves the pairing of Sources and Groups. The default method is a fully-meshed mapping of sources to groups, where every source is paired with every group. For a situation where there are ‘X’ number of sources and ‘Y’ number of groups, there will be ‘X x Y’ number of mappings, resulting in a great deal of memory usage for processing. When full-mesh mapping is not desired, the optional ‘One-To-One’ Source-Group Mapping can be used to save memory. In comparison, if a one-to-one type mapping behavior was preferred and only a full-mesh setup was available, you would have to create ‘N’ fully-meshed source-group mapping ranges of size ‘1’ to emulate the one-to-one behavior. An example showing the differences between the two types of mapping is shown in Figure 3-16 on page 3-30.

Figure 3-16. PIM-SM Source-Group Mapping Example

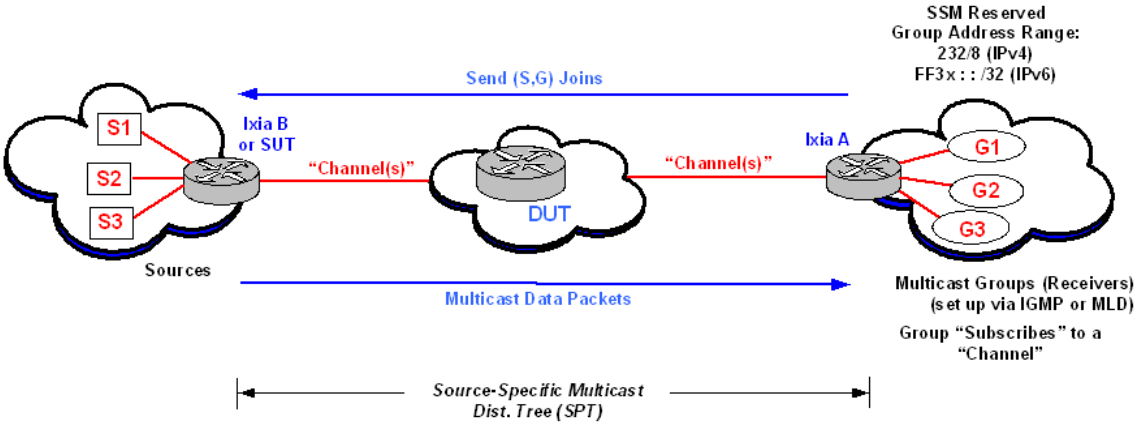


PIM-SSM

Protocol Independent Multicast - Source-Specific Multicast (PIM-SSM) uses a subset of the PIM-SM protocol, described in draft-ietf-ssm-arch-06, Source-Specific Multicast for IP, and in Section 4.8 of draft-ietf-pim-sm-v2-new-11, Protocol Independent Multicast - Sparse Mode (PIM-SM): Protocol Specification (Revised).

PIM-SSM is useful for broadcast-type applications, where one source sends packets to many host groups. There is no shared distribution tree topology, but there is a shortest-path tree (SPT) established, where the source is the root of the tree. In the case of SSM, the usual PIM-SM multicast terminology is modified, and the term *Channel* is used instead of *Group* and *Subscription* replaces *Join*. A multicast group (G) router that wants to receive packets from a specific Source (S) for its hosts/listeners, will 'Subscribe' to 'Channel (S,G).' An example of an PIM-SSM topology is shown in Figure 3-17 on page 3-31.

Figure 3-17. PIM-SSM Topology Example



An existing PIM-SM network can be modified to run SSM by enabling PIM-SSM on the source and destination/group routers. The typical PIM-SM signaling is not used for PIM-SSM, since the role of Rendezvous Point (RP) router is eliminated. The Subscribe (Join) message travels directly from the Destination router to the Source router, and data packets are transmitted in the opposite direction.

PIM-SSM Addressing

The PIM-SSM protocol uses a restricted addressing scheme, with reserved values for IPv4 SSM addresses defined by the IANA as 232.0.0.0 through 232.255.255.255 (232/8). IPv6 SSM addresses are defined in IETF DRAFT draft-ietf-ssm-arch- 06 and draft-ietf-pim-sm-v2-new-11 as FF3x: : /32. The range of FF3x: : /96 is proposed by RFC 3307, 'Allocation Guidelines for IPv6 Multicast Addresses.'

Differences Between PIM-SM and PIM-SSM

Some of the principal differences between PIM-SM and PIM-SSM routers, per draft-ietf-ssm-arch-06, are mentioned in the following list:

- PIM-SSM-only routers must not send (*,G) Join/Prune messages.
- PIM-SSM-only routers must not send (S,G,rpt) Join/Prune messages.
- PIM-SSM-only routers must not send Register messages for packets with SSM destination addresses.
- PIM-SSM-only routers must act in accordance with (*,G) or (S,G,rpt) state by forwarding packets with SSM destination addresses.
- PIM-SSM-only routers acting as RPs must not forward Register messages for packets with SSM destination addresses.

Protocol Elements for PIM-SSM

Protocol elements ***required*** for PIM-SSM-only routers are mentioned in the following list:

- (S,G) Downstream and Upstream state machines.
- Hello messages, neighbor discovery, and DR election.
- Packet forwarding rules.
- [(S,G) Assert state machine]

Some of the Protocol elements ***not required*** for PIM-SSM-only routers are mentioned in the following list:

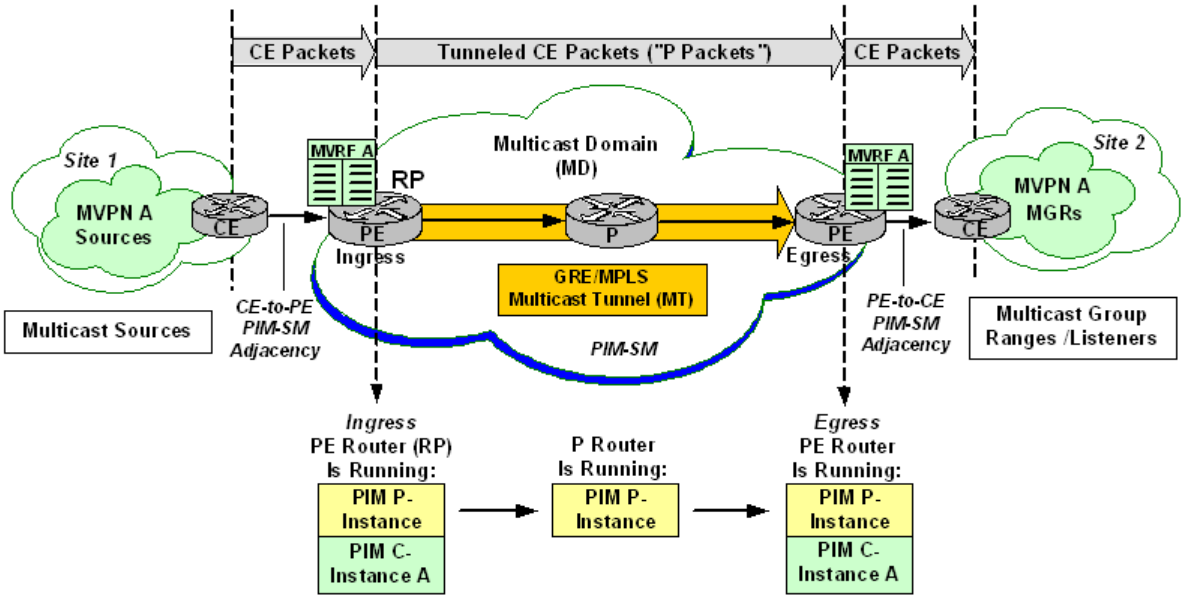
- Register state machine
- (*,G), (S,G,rpt), and (*,*,RP) Downstream and Upstream state machines.
- Keepalive Timer (treated as always running)
- SptBit (treated as always set for an SSM address)

Multicast VPNs

Multicast VPNs (MVPNs) can be created through the use of MP-BGP combined with PIM-SM. Multicast VPNs can be set up by a Service Provider to support scalable, IPv4 multicast traffic solutions, based on IETF draft-rosen-vpn-mcast-07, 'Multicast in MPLS/BGP IP VPNs.'

Multicast VRFs (MVRFs) on each PE router contain multicast routing tables. Within a Service Provider's domain, each MVRF is assigned to a Multicast Domain (MD), which is a set of MVRFs that can send multicast traffic to one another. Multicast packets from CE routers are sent over a (GRE) multicast tunnel to other PE routers in the multicast domain. A simplified example of a Multicast VPN topology, with one MVPN, is shown in Figure 3-18 on page 3-33.

Figure 3-18. Multicast VPN Topology Example



Each CE and its connected PE set up a PIM-SM adjacency. However, CEs do not set up PIM-SM adjacencies with each other. Separate CE-associated instances of PIM are run by each PE router, and these are called 'PIM C-instances.' Each C-instance is MVRF-specific. As each PE can be affiliated with many MVPNs/MVRFs, the router can run many PIM C-instances simultaneously, up to a maximum of one C-instance per MVRF.

PIM Provider-wide instances ('PIM P-instances') are run by each PE router, creating a global PIM adjacency with all of its IGP PIM-SM-enabled neighbors (P routers). P routers cannot set up PIM-SM C-instances.

At startup for the multicast domain's Provider Edge (PE) routers, the default Multicast Distribution Tree (MDT) is set up automatically. Each Multicast Domain is identified by a globally unique Service Provider (P) Group address and a Route Distinguisher. The MD group address is created by using BGP (L3 Site window). It is a valid 4-byte IPv4 multicast address prefix (for example, 239.1.1.1/32). The 12-byte Route Distinguisher is also created through BGP (L3 Site window). This Ixia implementation uses an RD value = 2. One C-Multicast Group Range (MGR) can be configured for each MVRF.

MPLS

Multi-Protocol Label Switching (MPLS) is based on the concept of label switching: and independent and unique ‘label’ is added to each data packet and this label is used to switch and route the packet through the network. The label is simple, essentially a shorthand version of the packet’s header information, so network equipment can be optimized around processing the label and forwarding traffic. This concept has been around the data communications industry for years. X.25, Frame Relay, and ATM are examples of label switching technologies.

It is important to understand the differences in the way MPLS and IP routing forward data across a network. Traditional IP packet forwarding uses the IP destination address in the packet’s header to make an independent forwarding decision at each router in the network. These hop-by-hop decisions are based on network layer routing protocols, such as Open Shortest Path First (OPSF) or Border Gateway Protocol (BGP). These routing protocols are designed to find the shortest path through the network, and do not consider other factors, such as latency or traffic congestion.

MPLS creates a connection-based model overlaid onto the traditionally connectionless framework of IP routed networks. This connection-oriented architecture opens the door to a wealth of new possibilities for managing traffic on an IP network. MPLS builds on IP, combining the intelligence of routing, which is fundamental to the operation of the Internet and today’s IP networks, with the high performance of switching. Beyond its applicability to IP networking, MPLS is being expanded for more general applications in the form of Generalized MPLS (GMPLS), with applications in optical and Time-Division Multiplexing (TDM) networks.

One of the primary original goals of MPLS, boosting the performance of software-based IP routers, has been superseded as advances in silicon technology have enabled line-rate routing performance implemented in router hardware. In the meantime, additional benefits of MPLS have been realized, notably Virtual Private Network (VPN) services and traffic engineering (TE).

Advantages of MPLS

Some of the advantages of using MPLS are:

- MPLS enables traffic engineering. Explicit traffic routing and engineering help squeeze more data into available bandwidth.
- MPLS supports the delivery of services with Quality of Service (QoS) guarantees. Packets can be marked for high quality, enabling providers to maintain a specified low end-to-end latency for voice and video.
- MPLS reduces router processing requirements, since routers simply forward packets based on fixed labels.

How Does MPLS Work?

MPLS is a technology used for optimizing forwarding through a network. Though MPLS can be applied in many different network environments, this discussion focuses primarily on MPLS in IP packet networks, by far the most common application of MPLS today.

MPLS assigns labels to packets for transport across a network. The labels are contained in an MPLS header inserted into the data packet.

These short, fixed-length labels carry the information that tells each switching node (router) how to process and forward the packets, from source to destination. They have significance only on a local node-to-node connection. As each node forwards the packet, it swaps the current label for the appropriate label to route the packet to the next node. This mechanism enables very-high-speed switching of the packets through the core MPLS network.

MPLS combines the best of both Layer 3 IP routing and Layer 2 switching. In fact, it is sometimes called a 'Layer 2-1/2' protocol. While routers require network-level intelligence to determine where to send traffic, switches only send data to the next hop, and so are inherently simpler, faster, and less costly. MPLS relies on traditional IP routing protocols to advertise and establish the network topology. MPLS is then overlaid on top of this topology. MPLS predetermines the path data takes across a network and encodes that information into a label that the network's routers can understand. This is the connection-oriented approach previously discussed. Since route planning occurs ahead of time and at the edge of the network (where the customer and service provider network meet), MPLS-labeled data requires less router horsepower to traverse the core of the service provider's network.

MPLS Routing

MPLS networks establish Label-Switched Paths (LSPs) for data crossing the network. An LSP is defined by a sequence of labels assigned to nodes on the packet's path from source to destination. LSPs direct packets in one of two ways: hop-by-hop routing or explicit routing.

Hop-by-Hop Routing

In hop-by-hop routing, each MPLS router independently selects the next hop for a given Forwarding Equivalency Class (FEC). A FEC describes a group of packets of the same type; all packets assigned to a FEC receive the same routing treatment. FECs can be based on an IP address route or the service requirements for a packet, such as low latency.

In the case of hop-by-hop routing, MPLS uses the network topology information distributed by traditional Interior Gateway Protocols (IGPs) routing protocols such as OPSF or IS-IS. This process is similar to traditional routing in IP networks, and the LSPs follow the routes the IGPs dictate.

Explicit Routing

In explicit routing, the entire list of nodes traversed by the LSP is specified in advance. The path specified could be optimal or not, but is based on the overall view of the network topology and, potentially, on additional constraints. This is called Constraint-Based Routing. Along the path, resources may be reserved to ensure QoS. This permits traffic engineering to be deployed in the network to optimize use of bandwidth.

Label Information Base

As the network is established and signaled, each MPLS router builds a Label Information Base (LIB), a table that specifies how to forward a packet. This table associates each label with its corresponding FEC and the outbound port to forward the packet to. This LIB is typically established in addition to the routing table and Forwarding Information Base (FIC) that traditional routers maintain.

Connections are signaled and labels are distributed among nodes in an MPLS network using one of several signaling protocols, including Label Distribution Protocol (LDP) and Resource reSerVation Protocol with Tunneling Extensions (RSVPTE). Alternatively, label assignment can be piggybacked onto existing IP routing protocols such as BGP.

The most commonly used MPLS signaling protocol is LDP. LDP defines a set of procedures used by MPLS routers to exchange label and stream mapping information. It is used to establish LSPs, mapping routing information directly to Layer 2 switched paths. It is also commonly used to signal at the edge of the MPLS network, the critical point where non-MPLS traffic enters. Such signaling is required when establishing MPLS VPNs.

RSVP-TE is also used for label distribution, most commonly in the core of networks that require traffic engineering and QoS. A set of extensions to the original RSVP protocol, RSVP-TE provides additional functionality beyond label distribution, such as explicit LSP routing, dynamic rerouting around network failures, preemption of LSPs, and loop detection. RSVP-TE can distribute traffic engineering parameters such as bandwidth reservations and QoS requirements.

Multi-protocol extensions have been defined for BGP, enabling the protocol to also be used to distribute MPLS labels. MPLS labels are piggybacked onto the same BGP messages used to distribute the associated routes. MPLS allows multiple labels (called a label stack) to be carried on a packet. Label stacking enables MPLS nodes to differentiate between types of data flows, and to set up and distribute LSPs accordingly. A common use of label stacking is for establishing tunnels through MPLS networks for VPN applications.

BFD

Bidirectional Forwarding Detection (BFD) is a network protocol used to detect faults between two forwarding engines. It provides low-overhead detection of

faults even on physical media that don't support failure detection of any kind, such as ethernet, virtual circuits, tunnels and MPLS LSPs.

BFD establishes a session between two endpoints over a particular link. If more than one link exists between two systems, multiple BFD sessions may be established to monitor each one of them. The session is established with a three-way handshake, and is torn down the same way. Authentication may be enabled on the session. A choice of simple password, MD5 or SHA1 authentication is available.

BFD does not have a discovery mechanism; sessions must be explicitly configured between endpoints. BFD may be used on many different underlying transport mechanisms and layers, and operates independently of all of these. Therefore, it needs to be encapsulated by whatever transport it uses. For example, monitoring MPLS LSPs involves piggybacking session establishment on LSP-Ping packets. Protocols that support some form of adjacency setup, such as OSPF or IS-IS, may also be used to bootstrap a BFD session. These protocols may then use BFD to receive faster notification of failing links than would normally be possible using the protocol's own keepalive mechanism.

A session may operate in one of two modes: asynchronous mode and demand mode. In asynchronous mode, both endpoints periodically send Hello packets to each other. If a number of those packets are not received, the session is considered down.

In demand mode, no Hello packets are exchanged after the session is established; it is assumed that the endpoints have another way to verify connectivity to each other, perhaps on the underlying physical layer. However, either host may still send Hello packets if needed.

Regardless of which mode is in use, either endpoint may also initiate an Echo function. When this function is active, a stream of Echo packets is sent, and the other endpoint then sends these back to the sender through its forwarding plane. This is used to test the forwarding path on the remote system.

CFM

Ethernet CFM is an end-to-end per-service-instance Ethernet layer OAM protocol that includes proactive connectivity monitoring, fault verification, and fault isolation. End to end can be PE to PE or customer edge (CE) to CE. Per service instance means per VLAN.

Being an end-to-end technology is the distinction between CFM and other metro-Ethernet OAM protocols. For example, MPLS, ATM, and SONET OAM help in debugging Ethernet wires but are not always end-to-end. 802.3ah OAM is a single-hop and per-physical-wire protocol. It is not end to end or service aware. Ethernet Local Management Interface (E-LMI) is confined between the uPE and CE and relies on CFM for reporting status of the metro-Ethernet network to the CE.

Troubleshooting carrier networks offering Ethernet Layer 2 services can be difficult. Customers contract with service providers for end-to-end Ethernet service and service providers may subcontract with operators to provide equipment and networks. Compared to enterprise networks, where Ethernet traditionally has been implemented, these constituent networks belong to distinct organizations or departments, are substantially larger and more complex, and have a wider user base. Ethernet CFM provides a competitive advantage to service providers for which the operational management of link uptime and timeliness in isolating and responding to failures is crucial to daily operations.

FCoE and NPIV

IxExplorer provides GUI access to all Ixia platform functionality with full support for stateless FCoE functional and scalability testing. The FCoE and Priority Flow Control (PFC) and FCoE Initialization Protocol (FIP) features allow testing of FCoE switches running both FCoE traffic and traditional Ethernet traffic.

Supported Load Modules

The following Ixia load modules have the Fibre Channel over Ethernet (FCoE) capability:

- LSM10GXM8-01, GXMR8-01, and GXM8XP-01, including 10GBASE-T versions LSM10GXM(R)8GBT-01
- LSM10GXM4-01, GXMR4-01, and GXM4XP-01, including 10GBASE-T versions LSM10GXM(R)4GBT-01
- LSM10GXM2XP-01 and GXMR2-01, including 10GBASE-T versions LSM10GXM(R)2GBT-01
- LSM1000XMVDCx-01 load modules. 4-port, 8-port, 12-port, and 16-port
- LSM1000XMVDC4-NG load modules. 4-port

Data Center Mode

FCoE support requires a new port mode, Data Center Mode. You need to switch port mode between Normal Mode and Data Center Mode to use the desired features in each mode.

- Mode switching (to or from Data Center Mode) triggers an FPGA re-download.
- There is no Packet Stream Mode support in Data Center Mode; only Advanced Scheduler Mode is supported.
- Supports 4-Priority traffic mapping for frame size up to 9216-byte. The different frame size support is determined by a sub mode in Data Center Mode. This limitation applies to all frames in Data Center Mode, whether FCoE frame or not.
- Data Center Mode only supports auto instrumentation mode for both TX and RX.
- When the port is in Data Center Mode, both existing Ethernet frames and FCoE frames are generated.

Priority Traffic Generation

The scheduling function is based on the existing Advanced Scheduler. A new parameter called ‘Priority Group’ has been added to each stream. You can map Priority Group to the priority field in the frame. The priority field in the same stream should not change (for example, if the priority is a VLAN priority field, then you cannot configure a UDF to control this field within a stream).

Priority-based Flow Control (PFC)

The Ixia port responds to either IEEE 802.3x pause frame or to IEEE 802.1Qbb Priority-based Flow Control (PFC) frame. The flow control type is determined by the selection made on the Flow Control tab of the Port Properties dialog, in IxExplorer.

IxExplorer Reference

See IxExplorer User Guide, Chapter 6 topic *Frame Data for FCoE Support*, subtopic *Priority-based Flow Control*.

Fibre Channel over Ethernet

When the port is in Data Center Mode, both existing Ethernet frames and FCoE frames are generated.

The Fibre Channel CRC is generated on the fly. This CRC is inserted at offset of Ethernet frame size minus 12 bytes. For example:

Ethernet Frame Size (bytes)	2000	2001	2002	2003
FC-CRC Offset in FCoE Frame (bytes)	1988	1989	1990	1991

The FC-CRC can be set to No Error or to Bad CRC.

Packet View Support

For Fibre Channel frame, there is no Extended Header and Optional Header support. It decodes only FC-2 Frame Header field.

FCoE Initialization Protocol (FIP)

FIP (FCoE Initialization Protocol) has been implemented (in addition to FCoE). It is used to discover and initialize FCoE capable entities connected to an Ethernet cloud.

IxExplorer Reference

See the IxExplorer User Guide, Chapter 6 topic *Frame Data for FCoE Support*.

NPIV Protocol Interface

NPIV stands for N_Port ID Virtualization. These can be used to virtually share a single physical N_Port. This allows multiple Fibre Channel initiators to occupy a single physical port, easing hardware requirements in SAN design. Up to 256 N_Port_IDs can be assigned to a single N_Port. NPIV interfaces can be configured using the Protocol Interface Wizard.

See the IxExplorer User Guide, Chapter 10, topic *NPIV Protocol Interface*.

Precision Time Protocol (PTP) IEEE 1588v2

Precision Time Protocol (IEEE 1588v2) allows precise synchronization of clocks in measurement and controls systems implemented with technologies such as network communications, local computing and distributed objects. The protocol supports system wide synchronization accuracy in sub-microseconds range with minimal network and local clock computing resources. The protocol operates in master/subordinate configuration. IEEE1588 deploys Multicast over an Ethernet network, and devices such as routers and switches can sync to the provided timing source.

Supported Load Modules

The following Ixia load modules have the PTP capability:

- LSM1000XMV(R)16, XMV(R)12, XMV(R)8, XMV(R)4
- ASM1000XMV12X
- Xcellon-Ultra XP, NP, and NG

Supported Messages

The following messages are supported between clocks participating in the PTP protocol.

- Event messages
  - Sync
  - Delay Request
- General Messages
  - Announce
  - Follow_up
  - Delay_Response

Supported Features

The following PTP features are supported.

- Only one two-step clock is supported on an Ixia port, at this time. One-step clock is not supported.
- Ixia ports can run other (non-PTP) traffic along with PTP traffic. Ixia ports have the ability to throttle transmit based on flow control packets being received.
- IEEE 1588 version 2.2 in IPV4 (multicast) is supported.
- Ports are manually configured in Master or Subordinate mode.
- A histogram reporting Subordinate clock OFFSET from master is provided in the form of plot along with PTP messages transmitted and received.
- Aggregate statistics are displayed in Statistics View in IxExplorer.
- Session/Per Interface stats is displayed in IxNw/Tcl/csv file.

- Per Interface configuration is done in protocol interfaces.
- Ability to compose or decode PTP messages from the IxExplorer user interface.
- Negative testing is supported.
    - Programmable follow-up messages as a percentage of sync messages. See how dropping 10-90% of follow-up messages (while sending 100% of sync messages) affects the DUT.
    - Send follow-up messages with a bad packet.
    - Purposely send data with timestamps that include jitter (to try forcing a sync to fail).
    - Negative testing is done with packet streams/linux.

Local Clock synchronization through PTP to another PTP clock

The local clock of the is synchronized to the ’s master clock by minimizing the Offset_from_master value of the current data set. The time and the rate characteristics of the local clock are modified upon receipt of either a sync message or follow-up message. Figure 3-19 illustrates the PTP communication path.

Figure 3-19. PTP Communication Path

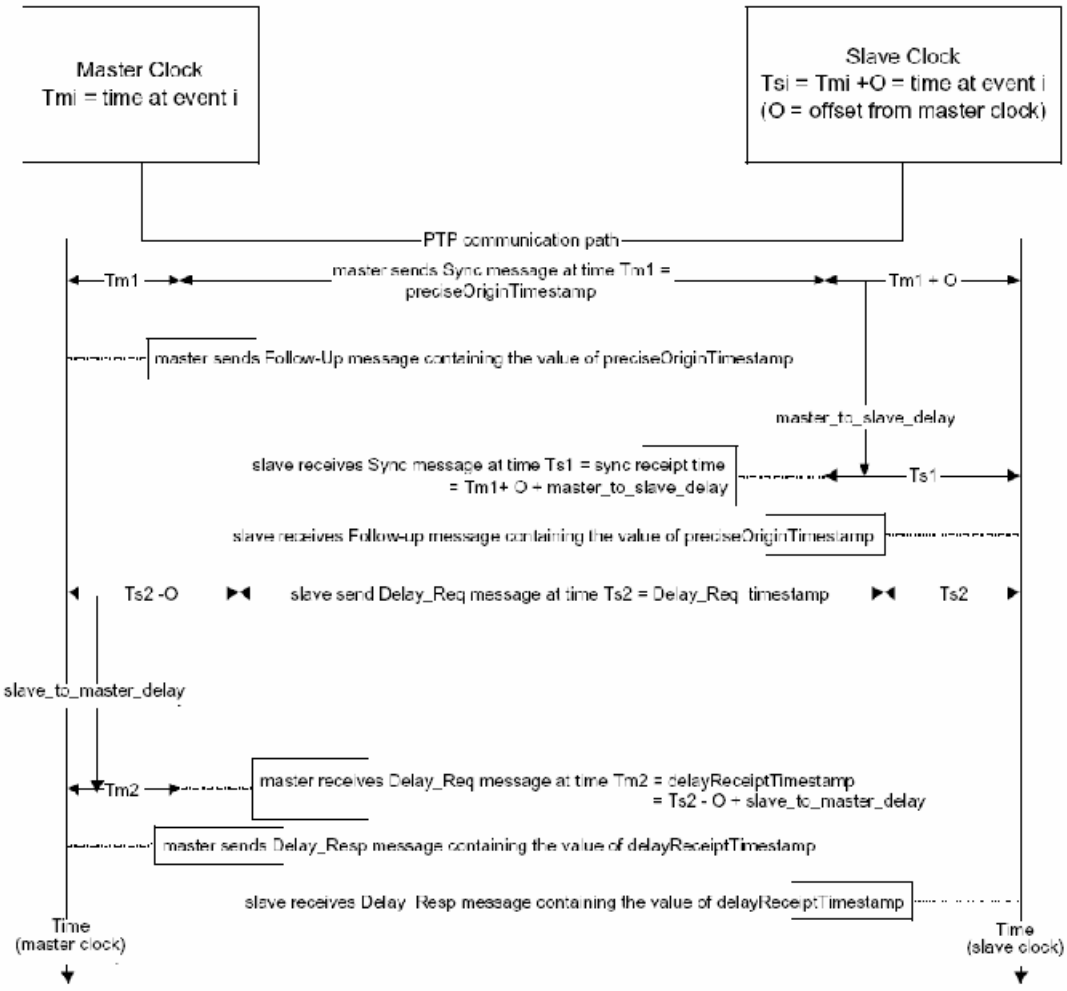


Table 3-7. PTP Communication Path

Term	Value
sync_receipt_time = Ts1	Ts1 =Tm1+O+master_to__delay
preciseOriginTimestamp = Tm1	Tm1
master_to__delay (computed)	Ts1–Tm1
delay_req_sending_time = Ts2	Ts2
delayReceiptTimestamp = Tm2	Tm2 = Ts2 – O + _to_master_delay
_to_master_delay (computed)	Tm2 – Ts2

Table 3-7. PTP Communication Path

Term	Value
one_way_delay	{(master_to__delay as computed) + (_to_master_delay as computed)}/2 {(Ts1-Tm1) + (Tm2-Ts2)}/2 {(O + master_to__delay) + –O +_to_master_delay)}/2 {(master_to__delay) + (_to_master_delay)}/2 master_to__delay if path is symmetrical

Notes:

1. Offset shall be computed as O= Ts1-Tm1 - one_way_Delay. Offset and One way delay shall be stored.
2. Offset correction shall be applied to the local clock.

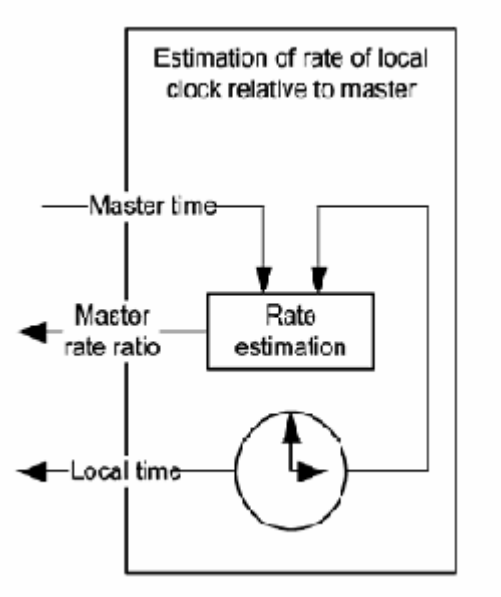
Local clock frequency transfer

In Slave mode of operation, the Ixia port implements a local clock in software (Linux). The frequency of the oscillator is not adjusted but allowed to free-run. The local clock shall be implemented based on time information synchronized from sync/follow_up messages and hardware timestamps associated with these messages. The local clock is associated with a constant and a slope. The rate of a local clock relative to a master clock is illustrated in Figure 3-20.

IxExplorer References

See the IxExplorer User Guide, Chapter 10, Protocol Interfaces, especially topics *Protocol Interfaces Tab*, *PTP Discovered Information*, and *PTP Clock Configuration*.

Figure 3-20. Rate of Local Clock Relative to Master



- Clock = K+ Slope*(TS-TS1),

- Slope = (T2-T1)/(TS2-TS1).
- K = T1

Where T1 is the time synchronized from the master and TS1 is the hardware timestamp associated with sync message 1. T2 and TS2 are corresponding parameters associated with sync message 2. T is the time at any point of time.

With a sync message, the parameters K and the slope are updated. The Clock Offset from master is calculated as discussed above and applied to K for correction.

Timestamps are cleared once when PTP is enabled.

In master mode of operation, server provides timestamp to the ports at the instant timestamps are cleared and slope is 1. OFFSET from master is 0.

If a GPS source is interfaced to the chassis, ports emulating the master are configured as Grand Master.

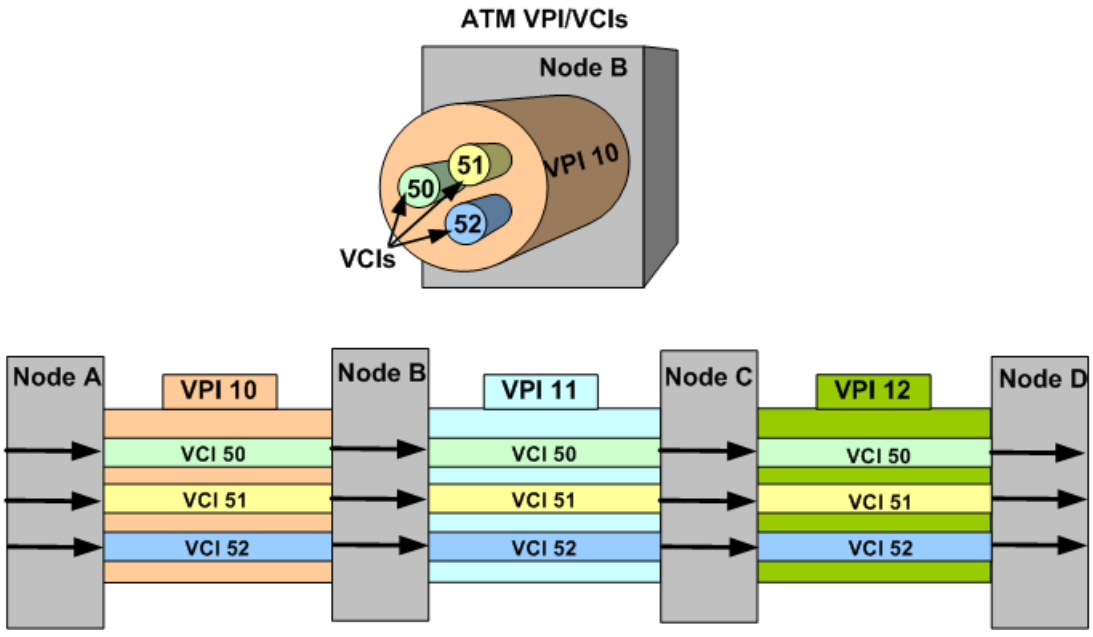
Local clock time format is seconds (32 bits) and nanoseconds (32 bits). The Ixia port supports a 2-step clock.

ATM Interfaces

On Asynchronous Transport Mode (ATM) is a Layer 2, connection-oriented, switching protocol, based on L2 Virtual Circuits (VCs). For operation in a connectionless IP routing or bridging environment, the IP PDUs must be encapsulated within the **payload field** of an ATM AAL5 CPCS-PDU (ATM Adaptation Layer 5—Common Part Convergence Sublayer—Protocol Data Unit). The ATM CPCS-PDUs are divided into 48-byte segments which receive 5-byte headers to form 53-byte ATM cells.

The ATM cells are then switched across the ATM network, based on the Virtual Port Identifiers (VPIs) and the Virtual Connection Identifiers (VCIs). The relationship between VPIs (identifying one hop between adjacent nodes) and VCIs (identifying the end-to-end virtual connection) is illustrated in Figure 3-21 on page 3-46.

Figure 3-21. ATM VPI/VCI Pairs (PVCs)



'Bridged ATM' Versus 'Routed ATM'

The ATM AAL5 frames allow for the overlay of the connectionless IP bridging or routing environment over the network of ATM nodes (that have frame handling capability). Each ATM node examines the payload of the AAL5 frame, and forwards the frame to the next node, based on the payload's MAC destination address (for IP bridging) or IP destination address (for IP routing). In effect, the ATM environment functions as a simulated Ethernet or IP network, respectively.

In the case of Label Distribution Protocol (LDP) routing over ATM, the process becomes more complex since MPLS tunnels are created over ATM core networks. For more information on the signaling, session setup, and label

distribution for LDP routing over ATM, see the *IxNetwork Users Guide: Network Protocols - LDP chapter*.

ATM Encapsulation Types

There are two main types of ATM Multiplexing encapsulations defined by RFC 2684, 'Multiprotocol Encapsulation over ATM Adaptation Layer 5.' The ATM AAL5 Frame is described in *ATM Frame Formats* on page 3-50. The various encapsulation types and references to diagrams of the encapsulated frame payloads are listed as follows:

- **VC Multiplexing (VC Mux)**: used when only one protocol is to be carried on a single ATM VC. Separate VCs are used if multiple protocols are being transported.
  - VC Mux IPv4 Routed: see Figure 3-27 on page 3-52
  - VC Mux IPv6 Routed: see Figure 3-28 on page 3-52
  - VC Mux Bridged Ethernet/802.3 (FCS): see Figure 3-23 on page 3-51
  - VC Mux Bridged Ethernet/802.3 (no FCS): see Figure 3-24 on page 3-51
- **Logical Link Control (LLC)**: used for multiplexing multiple protocols over a single ATM virtual connection (VC).
  - LLC Routed AAL 5 Snap: see Figure 3-29 on page 3-53
  - LLC Bridged Ethernet (FCS): see Figure 3-25 on page 3-51
  - LLC Bridged Ethernet (no FCS): see Figure 3-26 on page 3-52

Note: The Protocol Configuration Wizards for BGP, OSPFv2, and ISIS allow configuration on ATM ports, but ***ONLY*** for the VC Mux Bridged Ethernet/802.3 (FCS) encapsulation type.

Encapsulation Types by Protocol

The types of RFC 2684 ATM encapsulations available for each Ixia routing protocol emulation are listed in Table 3-8 on page 3-47.

Table 3-8. ATM Encapsulations for Protocols

Routing Protocol	ATM Encapsulation Type
BGP	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS) ***'Routed ATM':*** • VC Mux IPv4 Routed • VC Mux IPv6 Routed • LLC Routed AAL5 Snap

Table 3-8. ATM Encapsulations for Protocols

Routing Protocol	ATM Encapsulation Type
OSPF (v2 only) **Note**: Supported for both Point-to-Point and Point-to-MultiPoint links.	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS) ***'Routed ATM':*** • VC Mux IPv4 Routed • LLC Routed AAL5 Snap
LDP **Note**: Discovery Mode must be set to Basic, and Advertising Mode must be set to Downstream on Demand (DoD).	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS) ***'Routed ATM':*** • VC Mux IPv4 Routed • LLC Routed AAL5 Snap
RSVP-TE	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)
ISIS	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)
RIP	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)
RIPng	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)
IGMP	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS) - (the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)

Table 3-8. ATM Encapsulations for Protocols

Routing Protocol	ATM Encapsulation Type
MLD	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS)-(the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)
PIM-SM	***'Bridged ATM':*** • VC Mux Bridged Ethernet/802.3 (FCS)-(the default) • VC Mux Bridged Ethernet/802.3 (no FCS) • LLC Bridged Ethernet (FCS) • LLC Bridged Ethernet (no FCS)

ATM Frame Formats

The format of the ATM AAL5 CPCS-PDU (ATM AAL5 Frame) is shown in Figure 3-22 on page 3-50. The formats of the various types of AAL5 CPCS-PDU payloads for these frames are shown in the following diagrams:

- **BRIDGED:**
  - VC Mux Bridged Ethernet/802.3 (FCS): see Figure 3-23 on page 3-51
  - VC Mux Bridged Ethernet/802.3 (no FCS): see Figure 3-24 on page 3-51
  - LLC Mux Bridged Ethernet (FCS): see Figure 3-25 on page 3-51
  - LLC Mux Bridged Ethernet (no FCS): see Figure 3-26 on page 3-52
- **ROUTED:**
  - VC Mux IPv4 Routed: see Figure 3-27 on page 3-52
  - VC Mux IPv6 Routed: see Figure 3-28 on page 3-52
  - LLC Routed AAL5 Snap: see Figure 3-29 on page 3-53

Figure 3-22. ATM AAL5 CPCS-PDU (ATM AAL5 Frame)

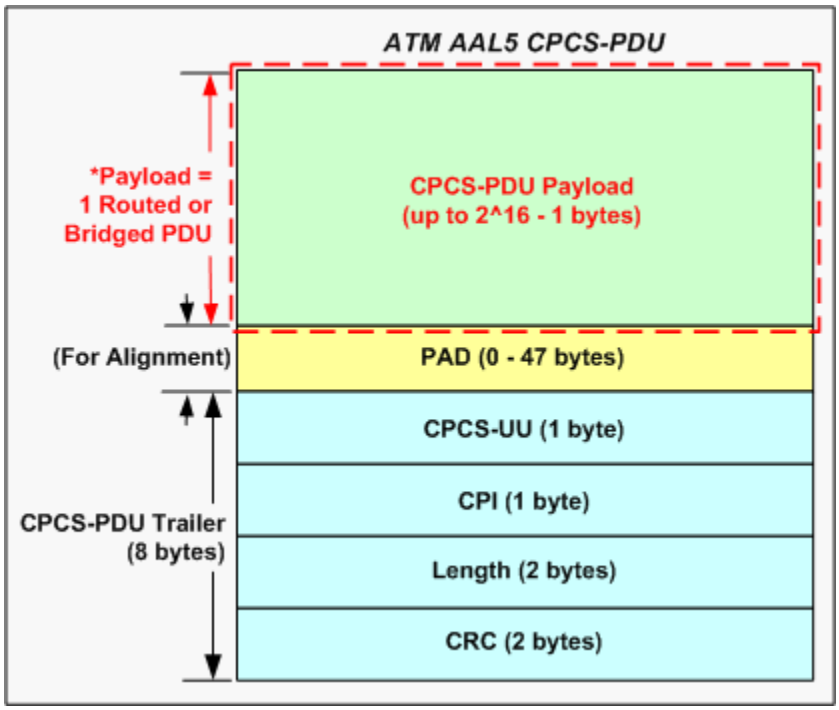


Figure 3-23. VC Mux Bridged Ethernet/802.3 (FCS)

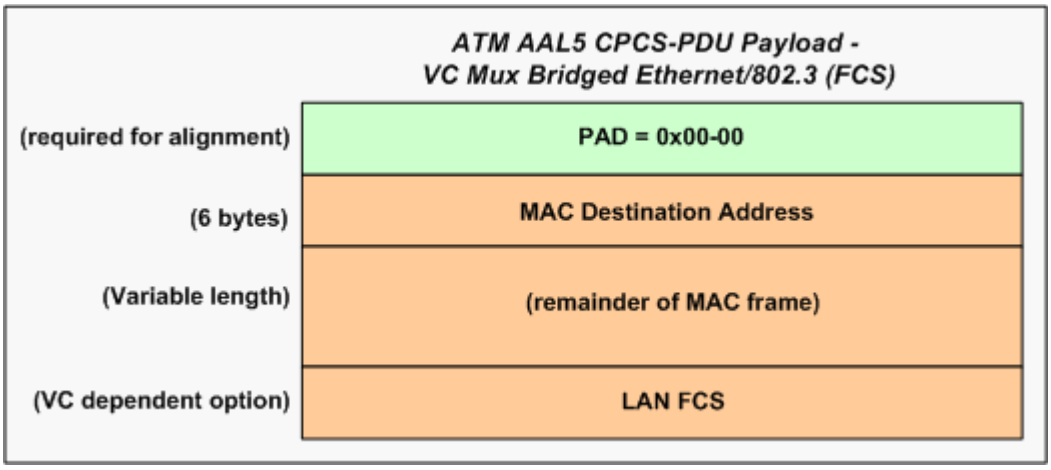


Figure 3-24. VC Mux Bridged Ethernet/802.3 (no FCS)

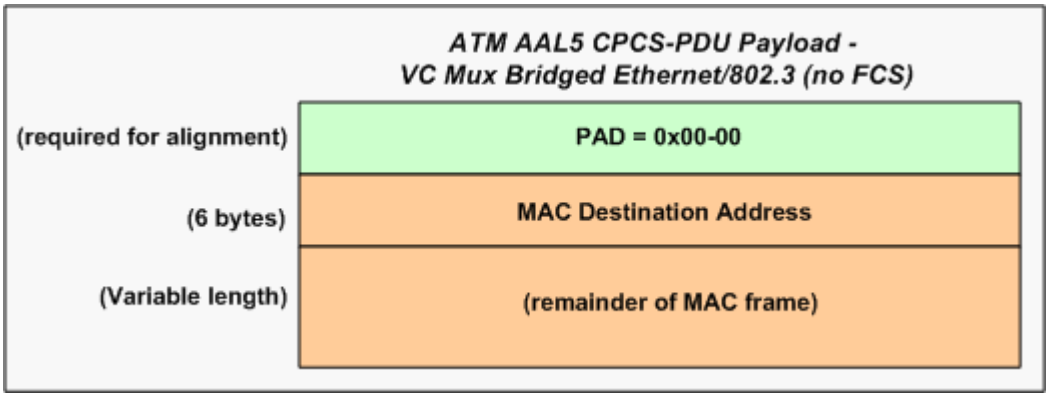


Figure 3-25. LLC Bridged Ethernet (FCS)

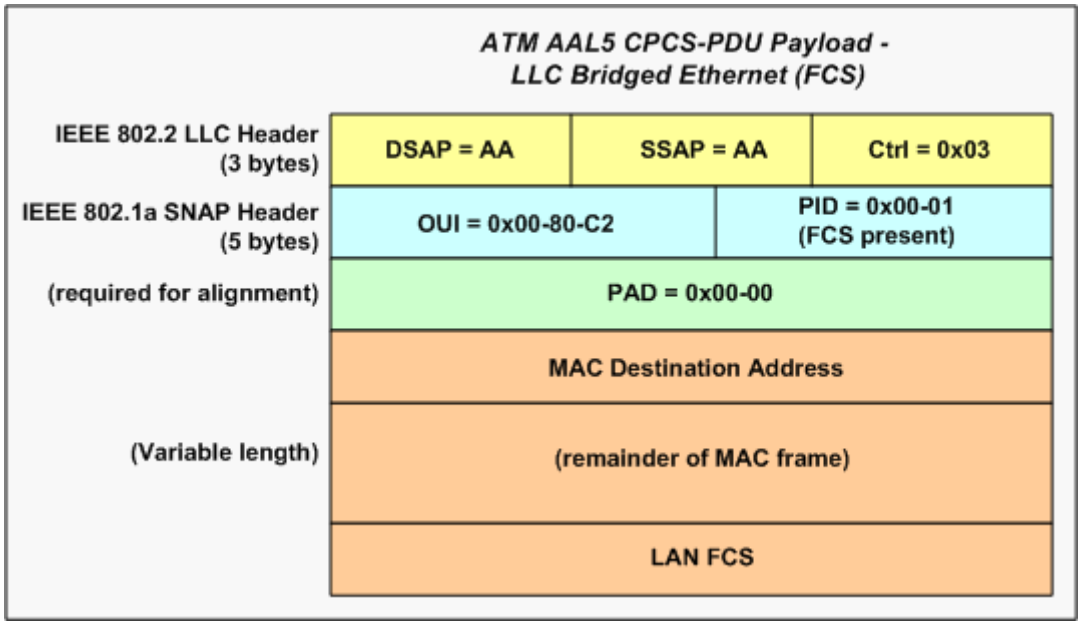


Figure 3-26. LLC Bridged Ethernet (no FCS)

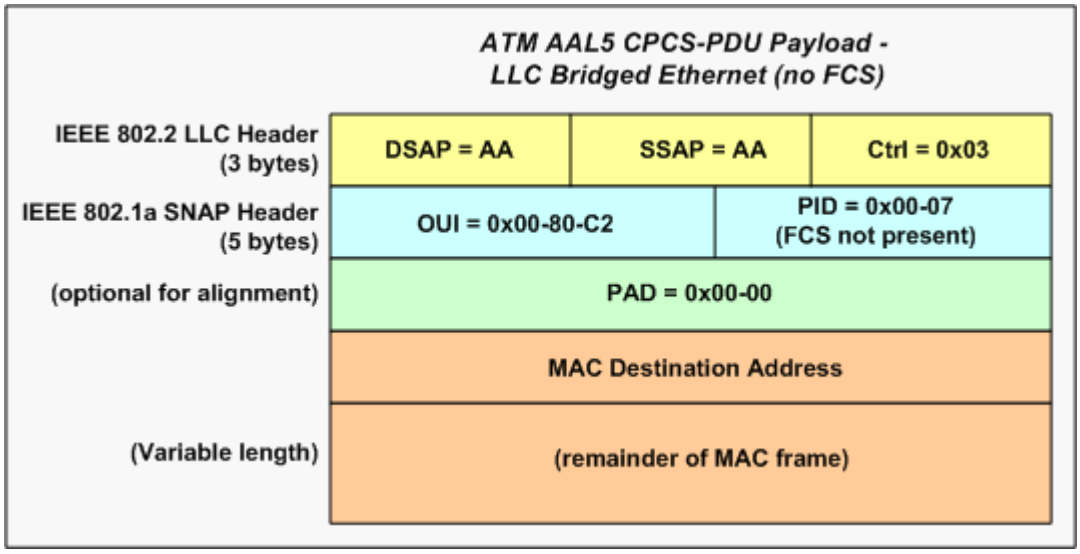


Figure 3-27. VC Mux IPv4 Routed

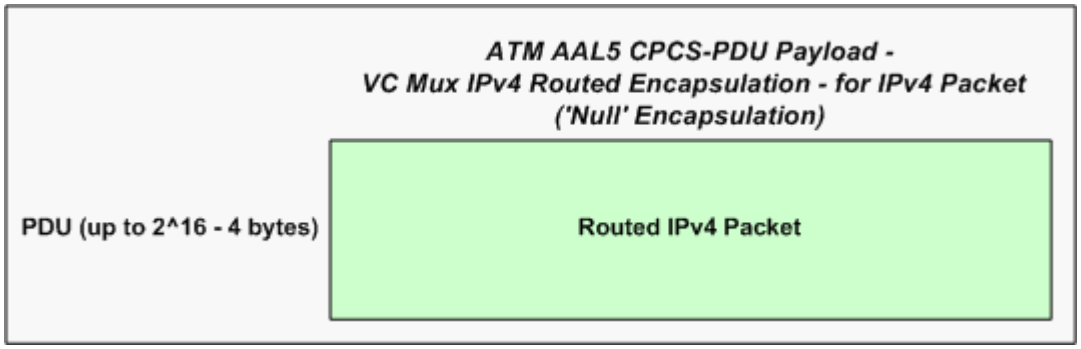


Figure 3-28. VC Mux IPv6 Routed

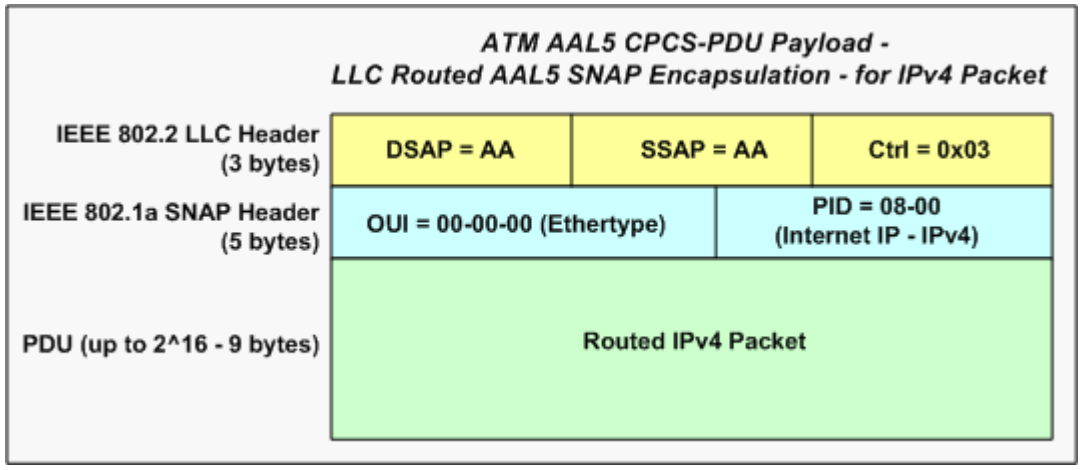
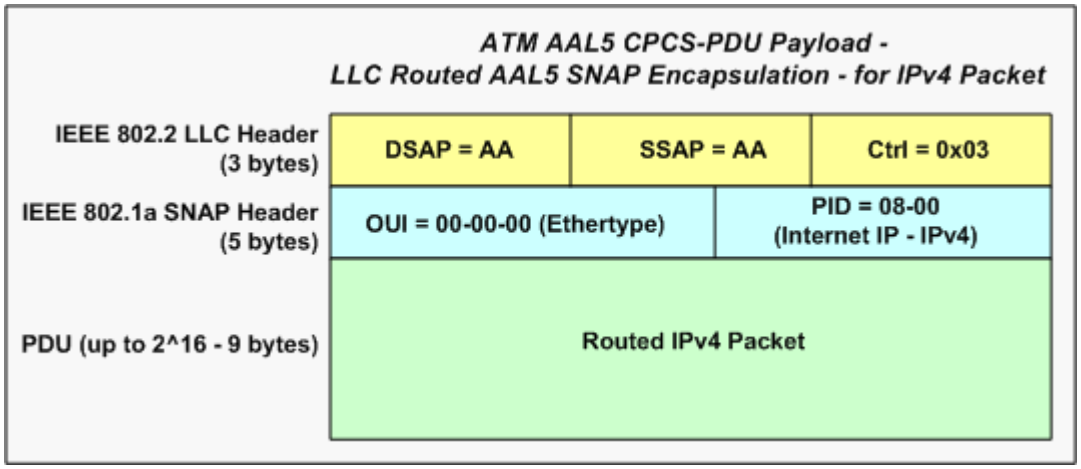


Figure 3-29. LLC Routed AAL5 Snap



Generic Routing Encapsulation (GRE)

RFC 2784, ‘Generic Routing Encapsulation’ (GRE), provides a mechanism for encapsulating a payload packet to send that packet over a network of a different type. First, a GRE header is prepended to the payload packet, and the Ethertype for the protocol used in that packet is included in the GRE header. Then, a Delivery header is prepended to the GRE header, which adds a Layer 2 Data Link Layer address plus a Layer 3 Network address (for a network protocol in this implementation, either IPv4 or IPv6). After a GRE-encapsulated payload packet has reached the last router of the GRE ‘tunnel,’ this router removes the GRE header and forwards the payload as a ‘normal’ packet for the native protocol in the network.

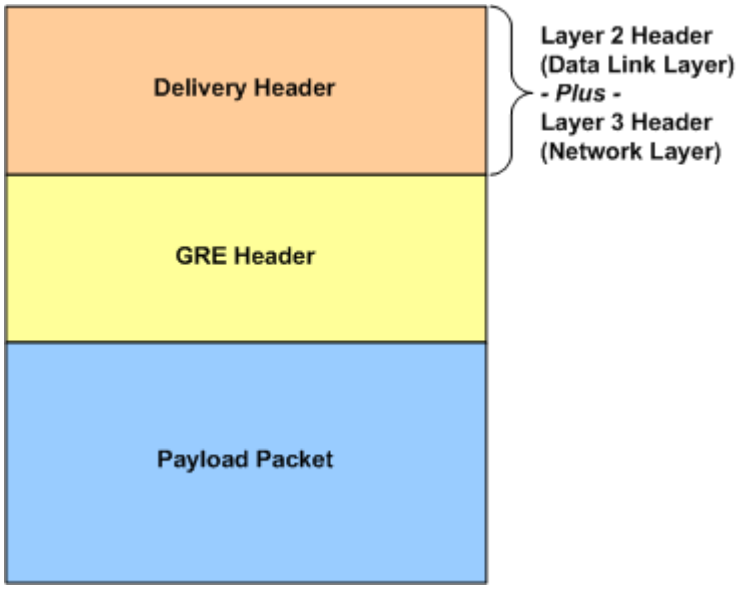
This is a relatively simple type of encapsulation and can be used to transparently carry packets for many different protocols, since it is based on Ethertypes. The original specifications for this encapsulation were RFC 1701, ‘Generic Routing Encapsulation (GRE),’ published in 1994, and RFC 1702, ‘Generic Routing Encapsulation over IPv4 Networks,’ also published in 1994.

RFC 2890, ‘Key and Sequence Number Extensions to GRE,’ provides optional fields for identifying individual traffic flows within a GRE tunnel through an authentication key value, and for monitoring the sequence of packets within each GRE tunnel.

GRE Packet Format

Both control and data packets can be GRE-encapsulated. The overall format of a GRE-encapsulated packet is shown in Figure 3-30 on page 3-54.

Figure 3-30. GRE-Encapsulated Packet



GRE Packet Headers

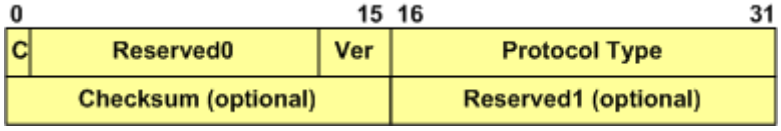
There are two formats for the GRE Packet Headers:

- *GRE Header per RFC 2784* on page 3-54
- *GRE Header per RFC 2890* on page 3-55

GRE Header per RFC 2784

The format of a GRE packet header per RFC 2784 is shown in Figure 3-31 on page 3-54.

Figure 3-31. GRE Packet Header (per RFC 2784)



The fields in the GRE header, per RFC 2784, are described in Table 3-9 on page 3-54.

Table 3-9. GRE Header Fields (per RFC 2784)

Field	Description
C	The Checksum Present flag bit. If set (= 1), the Checksum and Reserved1 fields are present, and the information in the Checksum field is valid.

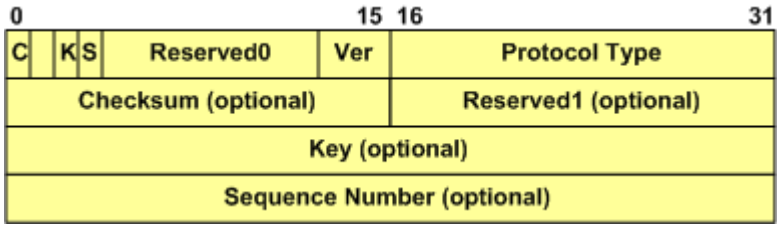
Table 3-9. GRE Header Fields (per RFC 2784)

Field	Description
Reserved0	(Bits 1 - 12) • Bits 1 - 5 unless the receiver is implementing RFC 1701, the receiver must discard the packet if any of these bits are non-zero. • Bits 6 - 12 reserved for future use.
Ver	The Version Number field. The value must be zero.
Protocol Type	Protocol Type field. The protocol type of the payload packet. These values are defined in RFC 1700, 'Assigned Numbers' and by the IANA 'ETHER TYPES' document. When the payload is an IPv4 packet, the protocol type must be set to 0x800 (Ethertype for IPv4).
Checksum	(Optional) The IP (one's complement) checksum of all of the 16-bit words in the GRE header and the payload packet. The value of the checksum field = zero for the purpose of computing the checksum. The checksum field is present only if Checksum Present bit is set (= 1).
Reserved1	(Optional) These bits are reserved for future use. This field is present only if the Checksum field is present (that is, the Checksum Present bit = 0). If present, this field must be transmitted as zero.

GRE Header per RFC 2890

The format of a GRE header, with added information per RFC 2890, is shown in Figure 3-32 on page 3-55.

Figure 3-32. GRE Header (per RFC 2890)



The fields in the GRE header, per RFC 2890, are described in Table 3-10 on page 3-56.

Table 3-10. GRE Header Fields (per RFC 2890)

Field	Description
C	The Checksum Present flag bit. If set (= 1), the Checksum field and the Reserved1 is present, and the information in the Checksum field is valid.
Reserved0	Bits 1 - 12. For bits 1 - 5, unless the receiver is implementing RFC 1701 the receiver must discard the packet if any of these bits are non-zero. For bits 6 - 12, these bits are reserved for future use.
K	The Key Present flag bit. If set (= 1), the Key field is present. If not set (= 0), this field is not present. (Compatible with RFC 1701)
S	The Sequence Number Present flag bit. If set (= 1), the Sequence Number Present field is present. If not set (= 0), this field is not present. (Compatible with RFC 1701)
Ver	The Version Number field. The value must be zero.
Protocol Type	Protocol Type field. The protocol type of the payload packet. These values are defined in RFC 1700, 'Assigned Numbers' and by the IANA 'ETHER TYPES' document (located at www.iana.org/assignments/ethernet-numbers). When the payload is an IPv4 packet, the protocol type must be set to 0x800 (Ethertype for IPv4).
Checksum	(Optional) The IP (one's complement) checksum of all of the 16-bit words in the GRE header and the payload packet. The value of the checksum field = zero for the purpose of computing the checksum. The checksum field is present only if Checksum Present bit is set (= 1).
Reserved1	(Optional) These bits are reserved for future use. This field is only present if the Checksum field is present (that is, the Checksum Present bit = 0). If present, this field must be transmitted as zero.

Table 3-10. GRE Header Fields (per RFC 2890)

Field	Description
Key Present	(Optional) This field is present only if the Key Present bit is set (= 1). A 4-octet number that can be used to identify an individual, logical traffic flow within the GRE tunnel. The encapsulator/sender uses the same key value for all packets within a single flow, for identification by the decapsulator/receiver.
Sequence Number Present	(Optional) This field is present only if the Sequence Number Present bit is set (= 1). A 4-octet number that can be used to identify the order of transmission of the packets, with the goal of providing unreliable, but in-order delivery of packets. The decapsulator/receiver uses the sequence number to monitor the order of the packets as they are received. Out-of-sequence packets should be silently discarded. The sequence number of the first packet = 0. The value range is from 0 to (2 ** 32) -1.

DHCP Protocol

Dynamic Host Configuration Protocol (DHCP) is defined in RFC 2131, and it is based on earlier work with the protocol for BOOTP relay agents, which was specified in RFC 951. A DHCP Server provides permanent storage and dynamic allocation of IPv4 network addresses and other network configuration information. A DHCP Server is a host, and a DHCP Client is also a host. This protocol is designed for allocating IPv4 addresses to hosts, but not to routers.

A Client Identifier (Client ID) is required so that the DHCP Server can match a DHCP client with its ‘lease.’ If the Client does not supply a Client Identifier option, the Client Hardware MAC Address (chaddr) is used by the Server to identify the Client. A lease is the period of time that a DHCP Client may use an IPv4 address that has been allocated by the DHCP Server. This lease period may be extended, and may even be set to ‘infinity’ (0xffffffff hex), to indicate a ‘permanent’ IPv4 address allocation.

DHCP messages are exchanged between client and server using UDP as the transport protocol. The DHCP Server port is UDP Port 67, and the DHCP Client port is UDP Port 68.

DHCPDISCOVER messages are broadcast by the Client on the local subnet, to reach the DHCP Server. Suggested values for a network address and lease period may be included in the Discover message. The Server(s) may respond with a DHCPOFFER message. The Offer message includes available IPv4 network

address, plus configuration parameters contained in the DHCP options (TLVs/objects).

Note: You will not be able to select DHCP-enabled protocol interfaces for use with Ixia protocol emulations, with the exception of IGMP.

DHCPv6 Protocol

The Dynamic Host Control Protocol for Version 6 (DHCPv6) is defined in RFC 3315. DHCPv6 uses UDP packets to exchange messages between servers and clients. The servers provide IPv6 addresses and additional configuration information to clients. A DHCPv6 server listens on a reserved, link-scope multicast address. A client identifies itself to the server by a link-local source address.

The groups of IPv6 addresses managed by the servers and clients are called Identity Associations (IAs), where each IA has a unique identifier. IA_NAs are identity associations of non-temporary (permanent) IPv6 addresses. IA_TAs are identity associations of temporary addresses.

RFC 3633, 'IPv6 Prefix Options for Dynamic Host Configuration Protocol (DHCP) Version 6,' adds capability for *automated* allocation of IPv6 prefixes from a delegating router to a requesting router. IA_PDs are identity associations used for delegated IPv6 address prefixes.

The setup for DHCPv6 involves a four-message exchange 'handshake.' Maintaining the DHCPv6 client-server relationship, and managing the return or deletion of IPv6 addresses involves three additional messages. These messages are described in the following list:

Message exchange (handshake):

- SOLICIT: Client sends a DHCPv6 SOLICIT message to the all DHCPv6 Agents multicast address to locate suitable servers.
- ADVERTISE: Multiple servers respond to the client's SOLICIT message by sending an ADVERTISE message to the client. The Client receives and stores ADVERTISE messages until the first retransmit timeout for SOLICIT messages, then accepts the message with the highest preference value. Or, the client immediately accepts an ADVERTISE message that has the preference value set to 255.
- REQUEST: Client sends a REQUEST message to the DHCPv6 server that has the highest preference value.
- REPLY: Server responds to the client's REQUEST message with a REPLY message containing the IPv6 address and configuration parameters required by the client.

Additional messages for Maintenance/Return/Deletion of Addresses:

- RENEW: Client sends a RENEW message to the assigned server after the Renew time specified for the IA. The server may respond with a REPLY message.
- REBIND: If the client does not receive a response (REPLY) from the primary (assigned) server, it multicasts a REBIND packet according to the Rebind time specified for the IA. The server(s) may each respond with a REPLY message.
- RELEASE: Client sends a RELEASE message to return one or more IPv6 addresses to the server when it has completed using the IPv6 address(es).
- **Note**: If the client does not receive any REPLY messages from the server in response to its RENEW or REBIND messages, the client deletes the assigned addresses according to the valid lifetimes of the addresses.

Ethernet OAM

The IEEE Std 802.3ah Operations, Administration, and Maintenance (OAM) sublayer provides mechanisms useful for monitoring link operation such as remote fault indication and remote loopback control. In general, OAM provides network operators the ability to monitor the health of the network and quickly determine the location of failing links or fault conditions.

OAM information is conveyed in Slow Protocol frames called OAM Protocol Data Units (OAM PDUs). OAM PDUs contain the appropriate control and status information used to monitor, test and troubleshoot OAM-enabled links.

The addition of Ethernet OAM support in IxOS involves the following :

- support in stream configuration dialogs to send OAM packets.
- support for a PCPU based state machine that is configured to act as a *passive* mode endpoint and reply to OAM packets.

A list of load modules and the Ethernet OAM statistics they can generate are provided in Table B-31 on page B-159. Ethernet OAM statistics counters are defined in Table B-6 on page B-9.

4 Optixia XM12 Chassis

This chapter provides details about the Optixia XM12 chassis—its specifications and features.

The Optixia XM12 is a next generation chassis that is a combination of the Optixia backplane architecture and a XM form factor. The 12-slot platform allows for higher port density load modules. The XM12 High Performance version has two 2.0 kW powersupplies, while the Standard version has two 1.6 kW power supplies. An upgrade kit is available to convert the Standard XM12 to the High Performance version. See *High Performance Upgrade Kit* on page 16.

Caution: This equipment is intended to be installed and maintained by Service Personnel.

The Optixia XM12 Chassis has 12 slots for support of up to 12 single wide load modules. The Optixia XM12 supports all load modules with improved system power and cooling. The Optixia XM12, shown in *Figure 4-1,* was specifically designed to allow the hot-swapping of modules, without requiring the chassis to be powered down.

Warning: To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Figure 4-1. Optixia XM12 Chassis

The Optixia family of chassis has improved data throughput between Load Modules and the chassis, with improved backplane performance.

The Optixia chassis provides improved modularity of major components to reduce downtime of a failed chassis and reduce the probability of needing to remove a failed chassis from the test environment. Among the modular features provided are:

- Power supplies
- Motherboard and support components (RAM, Hard Drive)
- Fans

The motherboard and power supplies are accessible from the front of the chassis. Each of the modular components is capable of being removed in the field and replaced with minimum downtime for the customer.

Note: In the event of indications of inadequate power, remove load modules starting from the low-number slots (slot 1, 2, 3), then working upward toward slot 12 until the problem is solved.

Warning Multiple Sources of Supply. Disconnect All Sources before Servicing	**Avertissement** Présence de plusieurs sources d'alimentation électrique. Débrancher toutes les sources d'alimentation avant intervention	**Achtung** Mehrfachstromquellen! Alle Versorgungskabel vor Wartung entfernen.	警告 複数のパワーサプライがありますので、保守する際には必ず全ての電源ケーブルを抜いてください

Warning High Touch Current. Earth Connection Essential Before Connecting Supply	**Avertissement** Fort courant de contact Raccordement à la Terre impératif Avant branchement de l'alimentation	**Achtung** Stellen Sie eine sichere Erdverbindung her, bevor Sie die Stromquelle anschließen.	警告 高漏洩電流に気を付け、適切に設置してから電源を接続してください

Specifications

XM12 Chassis

The Optixia XM12 computer and chassis specifications are contained in *Table 4-1*.

Table 4-1. Optixia XM12 Specifications

CPU	Intel Pentium D, 3.0 GHz
	**Caution–Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	4 GB
Disk	250GB SATA Disk DVD Drive
Operating System	Windows XP Professional
Physical	
Load Module Slots	12
Size	19.25 in. W x 17.5 in. H x 21 in. D (48.9cm W x 44.45cm H x 53.34cm D)
Weight (empty)	83 lb (37.65 kg)
Avg. Shipping Wt.	88 lb (39.92 kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for these load modules.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing

Table 4-1. Optixia XM12 Specifications

Storage	0% to 85%, non-condensing
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted.
Power	Upper line cord 1: 200-240V 60/50Hz Standard: 10A, High Performance: 15A Lower line cord 2: 200-240V 60/50Hz Standard: 8A, High Performance: 11A **Note**: Both power cords must be connected to the AC power source to provide sufficient power to the chassis. The upper line cord power supply provides power to the motherboard, fans, and some load modules. and the lower line cord power supply provides power to the remainder of the load modules. The chassis does not power up unless the upper power cord is installed. For North American customers, the power cords have NEMA L6-20P plugs for attachment to the power source and IEC-60320-C19 connectors that attach to the XM12 chassis.
	**Caution**: The chassis' safety approvals (UL and CE) are only valid when the unit is operating from 200-240VAC mains.
	**Caution:** The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.
	**Caution**: Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.
Power Supplies	Standard: two 1.6 kW; High Performance: two 2.0 kW
Front Panel Switches	On/Off momentary power push button
Front Panel Connectors	
Mouse	PS/2 6-pin DIN
Keyboard	PS/2 6-pin DIN
Monitor	HD-DB15 Super VGA
Printer	Female DB25 parallel port
Ethernet	RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port
Firewire	IEEE 1394
Serial	1 male DB9 port
USB	4 USB dual type A, 4-pin jack connectors

Table 4-1. Optixia XM12 Specifications

Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Line In/Line Out/Mic	3.5mm mini-TRS stereo jacks (qty 3)
Front Panel Indicators	See *LEDs/LCD Display* on page 6
	2 Paired LEDs above each slot position indicating Power and Active status
	LCD on front panel indicating chassis information
Back Panel Switches/ Connectors	Power On/Off rocker switch/Circuit Breakers (qty 2)
Power	2 male receptacles (IEC 60320-C19)

Electrical Grounding requirements for Multi-Chassis system configuration

To ensure consistent grounding:

- All equipment must be mounted and screwed in to grounded 19" racks.
- Equipment should not be powered via distribution units with isolated grounding.

If equipment grounding is not consistent, the software will detect this and shutdown to protect equipment from damage.

LEDs/LCD Display

The Optixia XM12 has the following set of front panel LEDs, for each load module slot:

Table 4-2. Optixia XM12 LEDs

Label	Color	Description
Power	Green	For each load module slot, the Power LED is illuminated when the board is being powered. When the Power LED is flashing, the board is being detected or initialized.
In Use	Green	For each load module slot, the Active LED is illuminated when a Load Module in a particular slot is owned by you.

LCD Display

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/ subordinate, and chassis status.

Supported Modules

The modules that are supported on the Optixia XM12 are listed in Table 4-3..

Table 4-3. Optixia XM12 Supported Modules

Module	SFF - Requires Adapter	Function
HSE40GETSP1-01 HSE100GETSP1-01 HSE40/100GETSP1-01		40 and 100 Gigabit Ethernet 1-port, 2-slot CFP interface (Full feature) dual-speed, 1-port, 2-slot CFP interface (Full feature)
HSE40GEQSFP1-01		1-port, 1-slot, QFSP interface (Full feature)
Xcellon-Ultra NP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
Xcellon-Ultra XP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
Xcellon-Ultra NG-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
ASM1000XMV12X-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
LSM1000XMSP12-01		12-Port Gigabit Ethernet Load Module, Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber
LSM1000XMVDC4-01 LSM1000XMVDC-NG LSM1000XMVDC8-01 LSM1000XMVDC12-01 LSM1000XMVDC16-01 LSM1000XMVDC16NG		4/8/12/16-Port Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber. FCoE enabled
LSM1000XMS12-01		10/100/1000 Ethernet 12 port module
LSM1000XMSR12-01		10/100/1000 Ethernet 12 port module, reduced feature set
LSM10GXM2XP-01 LSM10GXM2GBT-01 LSM10GXM2S-01		10 Gigabit Ethernet 2 port module, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version and SFP+ version.

Table 4-3. Optixia XM12 Supported Modules

Module	SFF - Requires Adapter	Function
LSM10GXMR2-01 LSM10GXMR2GBT-01 LSM10GXMR2S-01		10 Gigabit Ethernet 2 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version and SFP+ version.
LSM10GXM3-01		10 Gigabit Ethernet 3 port module
LSM10GXMR3-01		10 Gigabit Ethernet 3 port module, reduced feature set
LSM10GXM4-01		10 Gigabit Ethernet 4 port single slot, full-featured load module, 800MHz, 512MB. Full L2/7 support. Linux SDK, and L4-7 applications.
LSM10GXM4XP-01 LSM10GXM4GBT-01 LSM10GXM4S-01		10 Gigabit Ethernet 4 port module, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version and SFP+ version.
LSM10GXMR4-01 LSM10GXMR4GBT-01 LSM10GXMR4S-01		10 Gigabit Ethernet 4 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version and SFP+ version.
LSM10GXM8-01		10 Gigabit Ethernet 8 port single slot, full-featured module, 800MHz, 512MB. Full L2/7 support. Linux SDK, and L4-7 applications.
LSM10GXM8XP-01 LSM10GXM8GBT-01 LSM10GXM8S-01		10 Gigabit Ethernet 8 port module, 800MHz, 1GB, Extra Performance Includes 10GBASE-T version and SFP+ version.
LSM10GXMR8-01 LSM10GXMR8GBT-01 LSM10GXMR8S-01		10 Gigabit Ethernet 8 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version and SFP+ version.
NGY-NP8-01 NGY-NP4-01 NGY-NP2-01		10 Gigabit Application Network Processor Load Module, 2/4/8-Port LAN/WAN, SFP+ interface
AFM1000SP-01	X	10/100/1000 3 port Stream extraction module

Table 4-3. Optixia XM12 Supported Modules

Module	SFF - Requires Adapter	Function
LSM1000XMV4-01		4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR4-01		4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
LSM1000XMV8-01		8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR8-01		8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
LSM1000XMV12-01		12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR12-01		12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
LSM1000XMV16-01		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR16-01		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
CPM1000T8	X	Special 10/100/1000 Ethernet load module
MSM10G1-02	X	LAN/WAN/POS Multimode load module
LM100TXS2	X	10/100 Ethernet load module
LM100TXS8	X	8-port multilayer 10/100Mbps Ethernet load module
LM100TX8	X	8-port 10/100Mbps Ethernet, reduced features
LM1000STXR4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced feature set
LM1000STXS2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module.
LM1000STXS4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LM1000STXS4-256	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module; -256 version has 256MB of processor memory per port

Table 4-3. Optixia XM12 Supported Modules

Module	SFF - Requires Adapter	Function
LM1000STX2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LM1000STX4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LM1000TXS4	X	4-port 10/100/1000 Mbps Base-T Ethernet copper
LM1000TXS4-256	X	4-port 10/100/1000 Mbps Base-T Ethernet copper; -256 version has 256MB of processor memory per port
LM1000TX4	X	4-port 10/100/1000 Mbps Base-T Ethernet copper, reduced features
LM1000SFPS4	X	4-port Gigabit Ethernet fiber
ALM1000T8	X	Special 10/100/1000 Ethernet load module
ELM1000ST2	X	Special 10/100/1000 Ethernet load module
LSM10G1-01	X	10 Gigabit Ethernet load module
LSM10G1-01M	X	10 Gigabit Ethernet load module
LSM10GL1-01	X	10 Gigabit Ethernet load module
LSM1000POE4-02	X	4-port PoE load module
PLM1000T4-PD	X	Power over Ethernet load module
LM622MR	X	ATM/POS load module
LM622MR-512	X	ATM/POS load module
MSM2.5G1-01	X	OC-48c load module

Table 4-3. Optixia XM12 Supported Modules

Module	SFF - Requires Adapter	Function
VQM01XM		Voice Quality Resource Module performs real-time processing of speech quality analysis using PESQ algorithm, on streams received on ports of the following load modules: • Xcellon-Ultra NP-01 • Xcellon-Ultra XP-01 • Xcellon-Ultra NG-01 • ASM1000XMV12X-01 • LSM1000XMV4-01 • LSM1000XMV16-01 • ALM1000TS • CPM1000TS See *Voice Quality Resource Module* on page 17.
EIM10G4S	SFP adapter	10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces
EIM1G4S	SFP adapter	1Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces
LavaAP40/100GE 2P	CFP to QSFP	This is the dual speed 40GE/100GE Ethernet Lava load module with Accelerated Performance. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces. This load module supports full feature for layer 1 to layer 7 testing
LavaAP40/100GE 2RP	CFP to QSFP	This is the dual speed 40GE/100GE Ethernet Lava load module with data plane support only. It is an economic alternative to the Accelerated Performance load module, perfectly suitable for testing layer 1 to layer 3 applications that does not require routing protocol emulation. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces

Hot-Swap Procedure

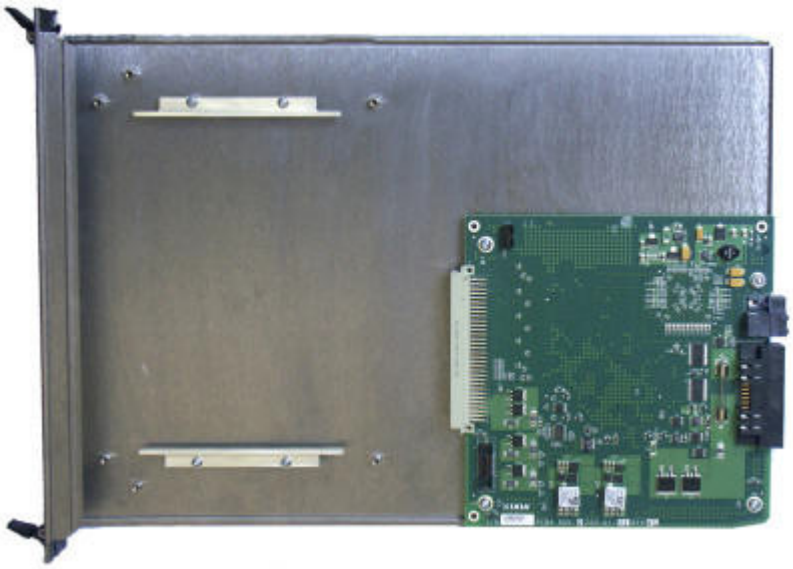
Each Optixia XM12 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D, *Hot-Swap Procedure*.

SFF Adapter Module

The Optixia XM12 adapter module allows legacy modules to be fit into the XM12 chassis. Figure 4-2 on page 4-12 shows an SFF adapter module.

Figure 4-2. SFF Adapter



A legacy module is inserted into the front of the adapter module and connects to the pins in the rear of the adapter. The entire assembly can then be inserted into any Optixia XM12 slot.

Once an adapter module is installed in a chassis, legacy load modules can be hot-swapped without removing the adapter module from the chassis.

Figure 4-3 on page 4-12 shows an SFF Adapter module with a legacy ATM card.

Figure 4-3. SFF Adapter with ATM Module

Table 4-3 on page 4-7 identifies the modules that can be used with the SFF Adapter.

Installing Filler Panels

The airflow in an Optixia XM12 chassis is inefficient if load modules are installed in a few slots and the rest of the chassis is left open. For best cooling results, filler panels are required. It is required that filler panels are used in situations where the slots in the chassis are not all in use.

An empty Optixia XM12 chassis includes:

- 5 ea. 1-slot wide XM12 Filler Panel/Air Baffle units (p/n 652-0648-04)
- 1 ea. 6-slot wide XM12 Filler Panel/Air Baffle unit (p/n 652-0353)

Prerequisites for Filler Panel Installation:

- The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.

Filler Panel Installation Procedure:

ESD Caution: Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

Example: Slide the one-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with two of the supplied screws.

Caution: Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

Not using filler panels could cause random failures in port operations or damage installed modules.

Cooling Fan Speed Control

The XM12 chassis automatically senses the temperature of specified modules and adjusts the cooling fan speed. If the system and board heat load is low enough, the cooling fan operates at a lower (quieter) speed.

The following modules have thermal sensors that report temperature readings:

- LSM1000XMS(R)12
- LSM1000XMV(R)16/12/8/4
- LSM10GXM(R)3
- NGY LSM10GXM2/4/8(R), LSM10GXM2/4/8XP, LSM10GXM(R)2/4/8S, and 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01, NGY-NP2/4/8, and NGY SFP+ 2/4/8.
- LavaAP40/100GE 2P and LavaAP40/100GE 2RP

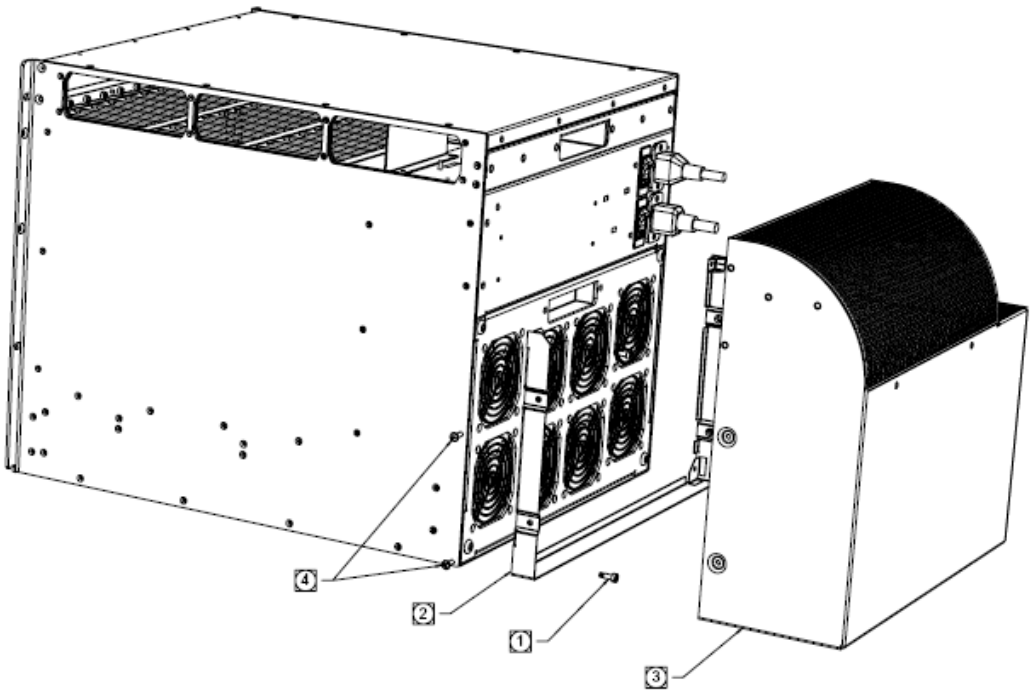
Other modules control the fan speed by means of a fixed speed setting. For a list of supported modules, see Table 4-3 on page 4-7.

XM12 Sound Reducer Installation

The XM12 Sound Reducer (PN 942-0021) is an optional accessory that installs on the rear of the XM12 chassis to reduce the sound of the cooling fans. It reduces the sound by approximately 10 dB.

Refer to the following figure when performing the installation.

Figure 4-4. XM12 Sound Reducer Installation



Note: The chassis should be placed in a horizontal position, in a well-lighted work area.

1. On the XM12 chassis rear, remove the four shoulder screws that hold the fan panel in place. Do not remove the fan panel.
2. Attach the sound reducer mounting bracket to the fan panel using the same four shoulder screws removed in Step 1.
3. Slide the sound reducer onto the mounting bracket.
4. Secure the sound reducer onto the mounting bracket using the four pan-head screws included in the XM12 Sound Reducer kit.

Rack Mount Cautions

Caution: If this unit is installed in a Rack Mount, observe the following precautions.

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced.
Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In Addition, Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

f: Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.

High Performance Upgrade Kit

A standard XM12 chassis (with two 1.6 kW power supplies) can be converted to a high performance XM12 (with two 2.0 kW power supplies) using an upgrade kit that is available from Ixia. Request 'Field Replaceable Unit, Power Supply Upgrade Kit' (FRU-OPTIXIAXM12-01) PN 943-0005.

Note: Standard XM12 chassis that are running more than ten NGY load modules must have a power supply upgrade kit installed.

We recommend the upgrade kit for existing XM12s with a fully loaded chassis combined with one or more NGY modules.

Caution: This equipment is intended to be installed and maintained by Service Personnel.

Voice Quality Resource Module

Voice Quality Resource Module (VQM01XM) performs real-time processing of speech quality analysis using PESQ algorithm, on streams received on ports of the following load modules:

- Xcellon-Ultra NP-01
- Xcellon-Ultra XP-01
- Xcellon-Ultra NG-01
- ASM1000XMV12X-01
- LSM1000XMV4-01
- LSM1000XMV16-01
- ALM1000TS
- CPM1000TS

The VQM01XM communicates with load modules through the chassis backplane. A single VQM01XM module can perform PESQ analyses, including necessary decoding, on up to 300 narrowband streams concurrently in real time. The PESQ stats are published in Stats View just after the last RTP packet of the analyzed sequence is received on port.

Statistics and Measurements

The following real time metrics (Min, Max, and Average values) are provided by the Voice Quality Resource Module, depending on the application being run:

- Active level
- Activity factor
- Noise level
- Peak level
- Listening effort (effort required to understand the meaning of spoken material)
- Listening quality (quality of speech)

These statistics are available in aggregated mode and individual per stream, as part of ‘VoIP RTP Per Channel’ statistics.

5 Optixia XM2 Chassis

This chapter provides details about the Optixia XM2 chassis—its specifications and features.

The Optixia XM2 is the next generation portable chassis that is a combination of the Optixia architecture with the XM form factor. The 2-slot platform allows for higher port density load modules in a portable chassis.

The Optixia XM2 Chassis has 2 slots for support of up to 2 single wide load modules. The Optixia XM2 supports all XM form factor load modules and many standard form factor load modules with improved system power and cooling. The Optixia XM2 was specifically designed to allow the hot-swapping of load modules, without requiring the chassis to be powered down. The Optixia XM2 is shown in *Figure 5-1*.

Note: The Optixia XM2 must only be operated in the horizontal position as shown in Figure 5-1.

Warning: To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Figure 5-1. Optixia XM2 Chassis

The Optixia family of chassis has improved data throughput between Load Modules and the chassis, with improved backplane performance.

The Optixia chassis provides improved modularity of major components to reduce downtime of a failed chassis and reduce the probability of needing to remove a failed chassis from the test environment. Among the modular features provided are:

- Power supplies
- Hard drive

The power supply is accessible from the back of the chassis. The hard drive is accessible from the bottom of the chassis.

Specifications

XM2 Chassis

The Optixia XM2 computer and chassis specifications are contained in *Table 5-1*.

Table 5-1. Optixia XM2 Specifications

CPU	Intel Pentium Mobile, 2.0 GHz
	Caution–Battery replacement There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	2 GB
Disk	250GB SATA Disk HD USB Drive
Operating System	Windows XP Professional

Table 5-1. Optixia XM2 Specifications

Physical	**Note**: The Optixia XM2 must only be operated in the horizontal position as shown in Figure 5-1 on page 5-2.
Load Module Slots	2 XM form factor
Size	4.8 in. H x 20.0 in. W x 14.2 in. D (12.2cm H x 50.8cm W x 36.1cm D)
Weight (empty)	25 lb (11.34 kg)
Avg. Shipping Wt.	30 lb (13.61 kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for each load module.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
Clearance	Sides: 4 in (10 cm); fan openings should be clear of all cables or other obstructions.
Power	100-240V 60/50Hz 12-6A
	**Caution:** The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.
Front Panel Switches	On/Off momentary power push button
Front Panel Connectors	
USB	1 USB dual type A, 4-pin jack connector
Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Front Panel Indicators	See *LEDs/LCD Display* on page 4.

Table 5-1. Optixia XM2 Specifications

	2 Paired LEDs above each slot position indicating Power and Active status 1 LED indicating chassis Power ON 1 LED indicating HDD operation LCD on front panel to display chassis information
Rear Panel Connectors	
Mouse	PS/2 6-pin DIN You **must** use the supplied Y-cable when using the PS/2 mouse.
Keyboard	PS/2 6-pin DIN (with or without the Y-cable)
Monitor	HD-DB15 Super VGA
Printer	Female DB25 parallel port
Ethernet	RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port
Serial	1 male DB9 ports
USB	2 USB dual type A, 4-pin jack connectors
Power	Male receptacle (IEC 60320-C13)

LEDs/LCD Display

The Optixia XM2 has the following set of front panel LEDs:

Table 5-2. Optixia XM2 LEDs

Label	Color	Description
Power	Green	For each load module slot, the Power LED is illuminated when the board is being powered. When the Power LED is flashing, the board is being detected or initialized.
Active	Green	For each load module slot, the Active LED is illuminated when a Load Module in a particular slot is owned by you.
Pwr	Green	For the chassis, indicated Power ON
HDD	Green	For the chassis, indicates hard disk is active

LCD Display

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.

- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

Supported Modules

The modules that are supported on the Optixia XM2 are listed in *Table 5-3*..

Table 5-3. Optixia XM2 Supported Modules

Module	SFF - Requires Adapter	Function
HSE40GETSP1-01 HSE100GETSP1-01 HSE40/100GETSP1-01		40 and 100 Gigabit Ethernet 1-port, 2-slot CFP interface (Full feature) dual-speed, 1-port, 2-slot CFP interface (Full feature)
HSE40GEQSFP1-01		1-port, 1-slot, QFSP interface (Full feature)
Xcellon-Ultra NP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
Xcellon-Ultra XP-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
Xcellon-Ultra NG-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
ASM1000XMV12X-01		12-port 10/100/1000 Mbps and 1-port 1GE aggregated and 1-port 10GE aggregated, Base T Ethernet copper, single-slot load module
LSM1000XMSP12-01		12-Port Gigabit Ethernet Load Module, Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber
LSM1000XMVDC4-01 LSM1000XMVDC4-NG LSM1000XMVDC8-01 LSM1000XMVDC12-01 LSM1000XMVDC16-01 LSM1000XMVDC16NG		4/8/12/16-Port Dual-PHY RJ45 10/100/1000 Mbps and SFP fiber. FCoE enabled
LSM1000XMS12-01		10/100/1000 Ethernet 12 port module
LSM1000XMSR12-01		10/100/1000 Ethernet 12 port module, reduced feature set

Table 5-3. Optixia XM2 Supported Modules

Module	SFF - Requires Adapter	Function
LSM10GXM2XP-01 LSM10GXM2GBT-01 LSM10GXM2S-01		10 Gigabit Ethernet 2 port module, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version and SFP+ version.
LSM10GXMR2-01 LSM10GXMR2GBT-01 LSM10GXMR2S-01		10 Gigabit Ethernet 2 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version and SFP+ version.
LSM10GXM3-01		10 Gigabit Ethernet 3 port module
LSM10GXMR3-01		10 Gigabit Ethernet 3 port module, reduced feature set
LSM10GXM4-01		10 Gigabit Ethernet 4 port single slot, full-featured load module, 800MHz, 512MB. Full L2/7 support. Linux SDK, and L4-7 applications.
LSM10GXM4XP-01 LSM10GXM4GBT-01 LSM10GXM4S-01		10 Gigabit Ethernet 4 port module, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version and SFP+ version.
LSM10GXMR4-01 LSM10GXMR4GBT-01 LSM10GXMR4S-01		10 Gigabit Ethernet 4 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version and SFP+ version.
LSM10GXM8-01		10 Gigabit Ethernet 8 port single slot, full-featured module, 800MHz, 512MB. Full L2/7 support. Linux SDK, and L4-7 applications.
LSM10GXM8XP-01 LSM10GXM8GBT-01 LSM10GXM8S-01		10 Gigabit Ethernet 8 port module, 800MHz, 1GB, Extra Performance. Includes 10GBASE-T version and SFP+ version.
LSM10GXMR8-01 LSM10GXMR8GBT-01 LSM10GXMR8S-01		10 Gigabit Ethernet 8 port module, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version and SFP+ version.
NGY-NP8-01 NGY-NP4-01 NGY-NP2-01		10 Gigabit Application Network Processor Load Module, 2/4/8-Port LAN/WAN, SFP+ interface

Table 5-3. Optixia XM2 Supported Modules

Module	SFF - Requires Adapter	Function
AFM1000SP-01	X	10/100/1000 3 port Stream extraction module
LSM1000XMV4-01		4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR4-01		4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
LSM1000XMV8-01		8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR8-01		8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
LSM1000XMV12-01		12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR12-01		12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
LSM1000XMV16-01		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LSM1000XMVR16-01		16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance
CPM1000T8	X	Special 10/100/1000 Ethernet load module
MSM10G1-02	X	LAN/WAN/POS Multimode load module
LM100TXS2	X	10/100 Ethernet load module
LM100TXS8	X	8-port multilayer 10/100Mbps Ethernet load module
LM100TX8	X	8-port 10/100Mbps Ethernet, reduced features
LM1000STXR4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced feature set
LM1000STXS2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module.
LM1000STXS4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module

Table 5-3. Optixia XM2 Supported Modules

Module	SFF - Requires Adapter	Function
LM1000STXS4-256	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module; -256 version has 256MB of processor memory per port
LM1000STX2	X	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LM1000STX4	X	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module
LM1000TXS4	X	4-port 10/100/1000 Mbps Base-T Ethernet copper
LM1000TXS4-256	X	4-port 10/100/1000 Mbps Base-T Ethernet copper; -256 version has 256MB of processor memory per port
LM1000TX4	X	4-port 10/100/1000 Mbps Base-T Ethernet copper, reduced features
LM1000SFPS4	X	4-port Gigabit Ethernet fiber
ALM1000T8	X	Special 10/100/1000 Ethernet load module
ELM1000ST2	X	Special 10/100/1000 Ethernet load module
LSM10G1-01	X	10 Gigabit Ethernet load module
LSM10G1-01M	X	10 Gigabit Ethernet load module
LSM10GL1-01	X	10 Gigabit Ethernet load module
LSM1000POE4-02	X	4-port PoE load module
PLM1000T4-PD	X	Power over Ethernet load module
LM622MR	X	ATM/POS load module
LM622MR-512	X	ATM/POS load module
MSM2.5G1-01	X	OC-48c load module

Table 5-3. Optixia XM2 Supported Modules

Module	SFF - Requires Adapter	Function
VQM01XM		Voice Quality Resource Module performs real-time processing of speech quality analysis using PESQ algorithm, on streams received on ports of the following load modules: • Xcellon-Ultra NP-01 • Xcellon-Ultra XP-01 • Xcellon-Ultra NG-01 • ASM1000XMV12X-01 • LSM1000XMV4-01 • LSM1000XMV16-01 • ALM1000TS • CPM1000TS See *Voice Quality Resource Module* on page 17.
EIM10G4S	SFP adapter	10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces
EIM1G4S	SFP adapter	1Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces
LavaAP40/100GE 2P	CFP to QSFP	This is the dual speed 40GE/100GE Ethernet Lava load module with Accelerated Performance. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces. This load module supports full feature for layer 1 to layer 7 testing
LavaAP40/100GE 2RP	CFP to QSFP	This is the dual speed 40GE/100GE Ethernet Lava load module with data plane support only. It is an economic alternative to the Accelerated Performance load module, perfectly suitable for testing layer 1 to layer 3 applications that does not require routing protocol emulation. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces

Rack Mount Instructions

Caution: If this unit is installed in a rack mount, observe the following precautions:

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

Installing Rack-Mount Ear Brackets

To mount the Optixia XM2 chassis into an equipment rack, first attach the rack-mount ears to the sides of the chassis.

1. If side feet are present (on left side of chassis) remove them. Discard the rubber feet, but keep the screws. See Figure 5-2 on page 5-11.
2. Reinstall the screws removed in step 1 (into the same holes).
3. Install left-side ear bracket (Ixia PN 652-0688-02) using supplied screws (PN 600-0105). See Figure 5-3 on page 5-11.
4. Install right-side ear bracket (Ixia PN 652-0688-01) using supplied screws (PN 600-0105). See Figure 5-4 on page 5-12.

Figure 5-2. Remove Side Feet (If Present)

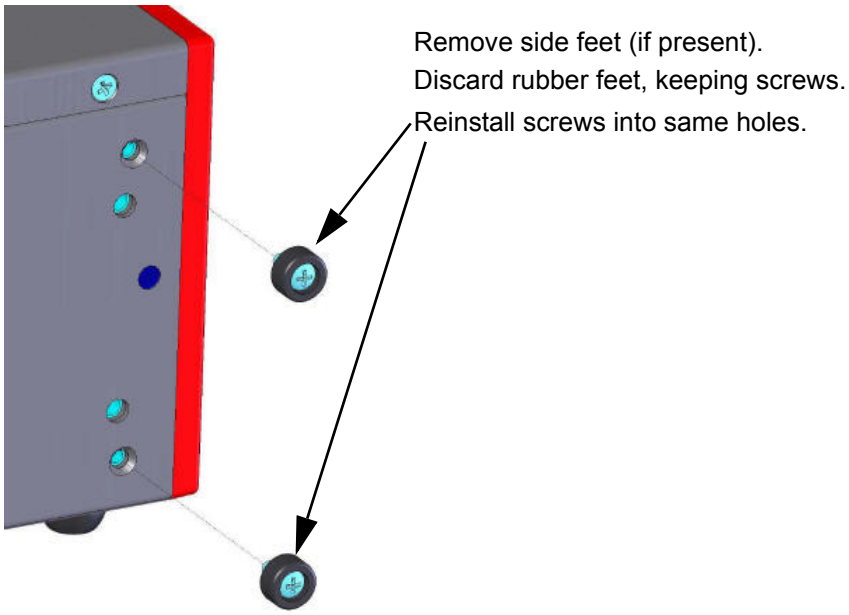


Figure 5-3. Install Left Ear Bracket

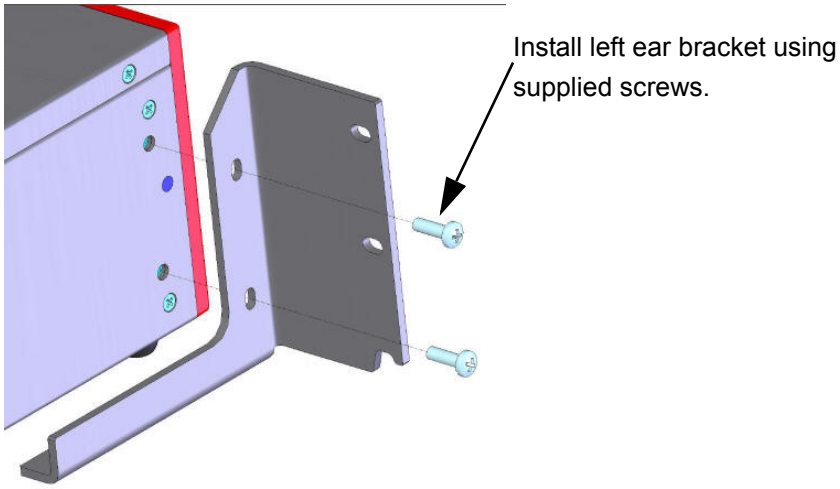
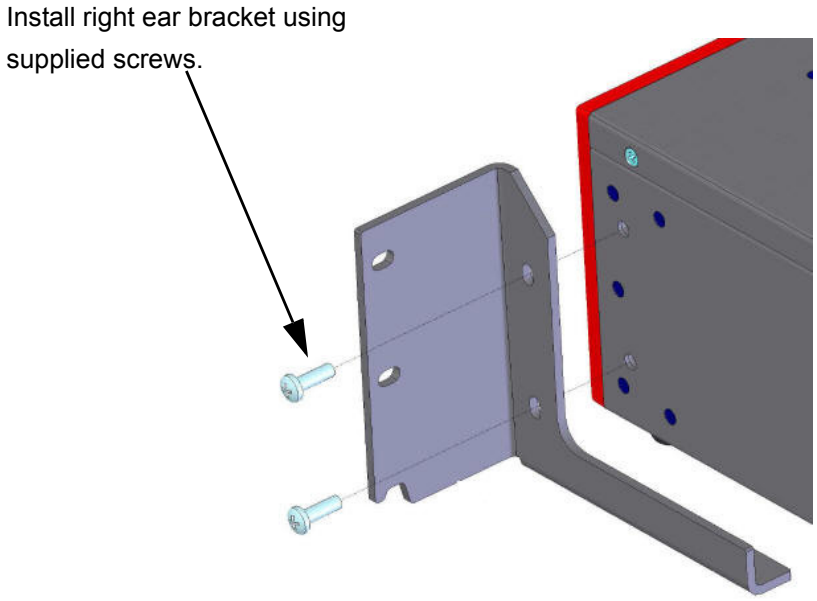


Figure 5-4. Install Right Ear Bracket



Hot-Swap Procedure

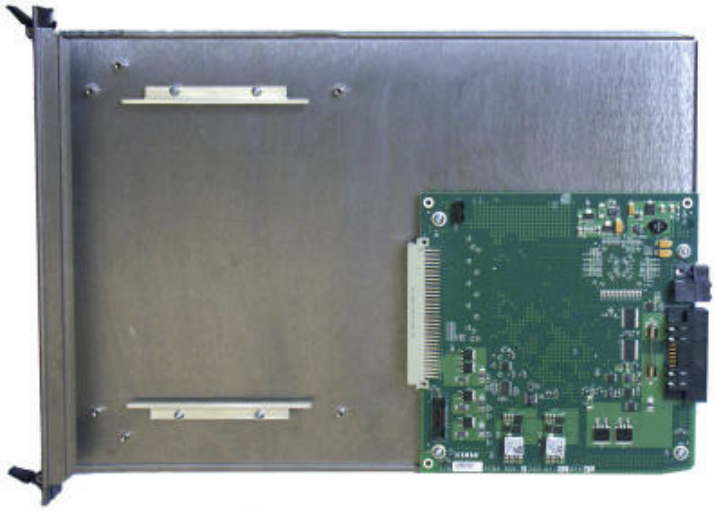
Each Optixia XM2 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D, *Hot-Swap Procedure*.

SFF Adapter Module

The Optixia XM adapter module allows legacy modules to be fit into the XM2 chassis. Figure 5-5 on page 5-13 shows an SFF adapter module.

Figure 5-5. SFF Adapter



A legacy module is inserted into the front of the adapter module and connects to the pins in the rear of the adapter. The entire assembly can then be inserted into either Optixia XM2 slot.

Once an adapter module is installed in a chassis, legacy load modules can be hot-swapped without removing the adapter module from the chassis.

Figure 5-6 on page 5-13 shows an SFF Adapter module with a legacy ATM card.

Figure 5-6. SFF Adapter with ATM Module

Table 5-3 on page 5-5 identifies the modules that can be used with the SFF Adapter.

Installing Filler Panels

The airflow in an Optixia XM2 chassis can be inefficient if a load module is installed in one slot and the other is left open. For best cooling results, filler panels are required. Filler panels must be used in situations where the slots in the chassis are not all in use.

An empty Optixia XM2 chassis includes:

- 1 ea. 1 slot wide XM2 Filler Panel/Air Baffle units (p/n 652-0648-04)

Prerequisites for Filler Panel Installation:

The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.

Filler Panel Installation Procedure:

ESD Caution: Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

Example: Slide the one-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with two of the supplied screws.

Caution: Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

Not using filler panels could cause random failures in port operations or damage installed modules.

Cooling Fan Speed Control

The XM2 chassis automatically senses the temperature of specified modules and adjusts the cooling fan speed. If the system and board heat load is low enough, the cooling fan operates at a lower (quieter) speed.

The following modules have thermal sensors that report temperature readings:

- LSM1000XMS(R)12
- LSM1000XMV(R)16/12/8/4
- LSM10GXM(R)3
- NGY LSM10GXM2/4/8(R), LSM10GXM2/4/8XP, LSM10GXM(R)2/4/8S, 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01, NGY-NP2/4/8, and NGY SFP+ 2/4/8.
- LavaAP40/100GE 2P and LavaAP40/100GE 2RP

Other modules control the fan speed by means of a fixed speed setting. For a list of supported modules, see Table 5-3 on page 5-5.

6 XG12 Chassis

This chapter provides details about the XG12 chassis—its specifications and features.

The XG12 Chassis is the next generation high performance platform capable of supporting all XM form factor load modules, including full chassis configurations of the Xcellon load modules. It is a 12-slot chassis with increased total power capacity available for all load modules and front-to-back airflow delivery along with increased bandwidth from the CPU to the load modules.

The chassis provides improved modularity and access to the major components to reduce downtime of a failed chassis and to reduce the probability of needing to remove a failed chassis from the test environment. The four separate modules that make up the chassis are shown in Table 6-1.

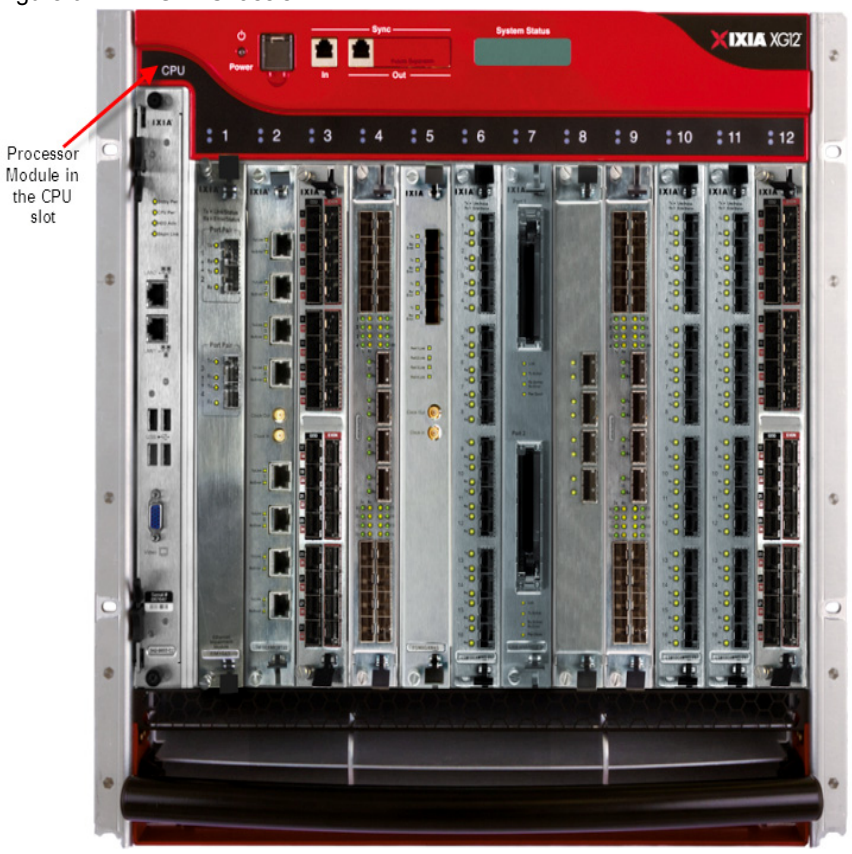
Table 6-1. XG12 Part Numbers and Modules

Part Number	Description
941-0017	XG12, 12-Slot Chassis Frame Module
942-0031	XG12, 12-Slot Chassis Fan Module
942-0032	XG12, 12-Slot Chassis Power Supply Module
942-0033	XG12, 12-Slot Chassis Processor Module

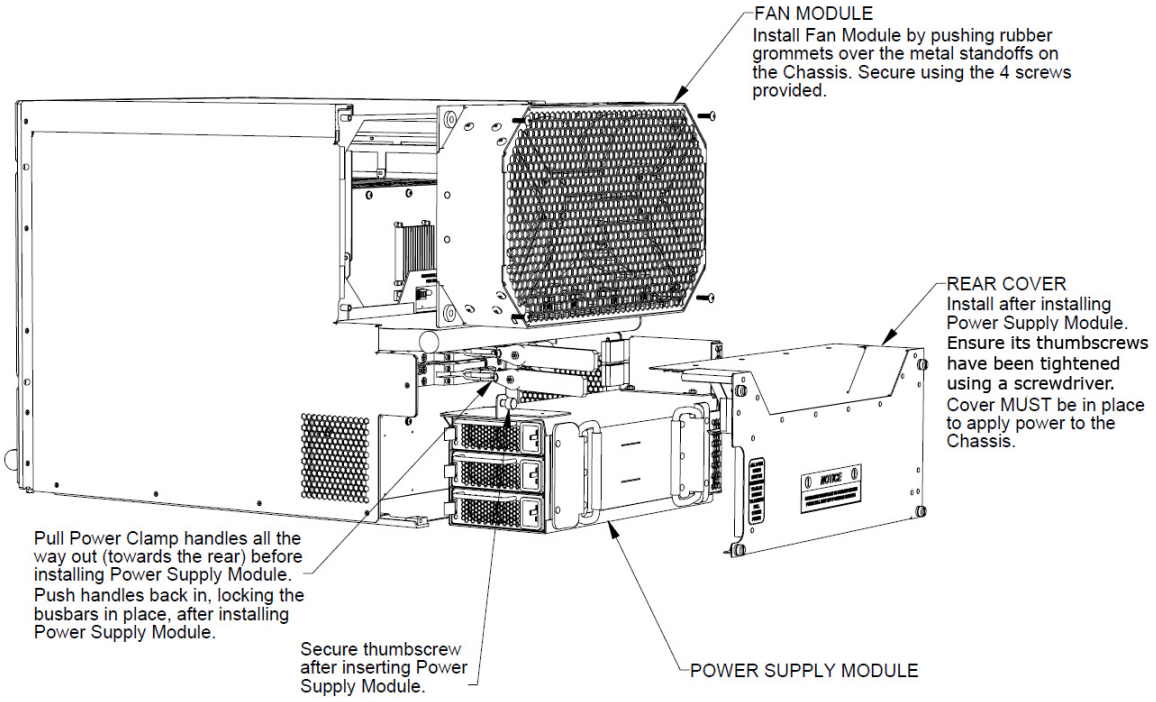
The XG12, shown in Figure 6-1, allows the hot-swapping of load modules, without requiring the chassis to be powered down. The Processor module for the XG12 chassis is not hot swappable.

The Processor Module is plugged into the front of the chassis. The power supplies and fans are accessible from the rear of the chassis. Each of the modular components is capable of being removed in the field and replaced with minimum downtime.

Figure 6-1. XG12 Chassis



The component modules of the XG12 chassis are shown in the following figure:



Specifications

The XG12 chassis specifications are contained in the following tables:.

Table 6-2. XG12 Processor Module Specifications

Processor Module	Field replaceable and removable processor card module with an Intel 2.26 GHz Core™ 2 Duo processor with 4 GB CPU memory, and 250 GB SATA hard drive
Memory	4GB
Hard Disk Drive	250GB
Operating System	Windows 7

Table 6-2. XG12 Processor Module Specifications

	Caution–Battery replacement There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions. **Note**: The serial number for the Processor Module is located on module itself. This is used as the overall chassis serial number.

Table 6-3. XG12 Chassis Specifications

Size	• 19.0 in. W x 19.21 in. H x 27.2 in. D • 48.26cm W x 48.79cm H x 69.09cm D • 11 rackmount units (11RU)
Load Module Slots	12 (compatible with Ixia XM form factor load modules)
Chassis Power	The chassis requires three single phase, 200-240VAC, 50/60Hz circuits, each capable of providing 3680 watts. These circuits must provide protection against over-currents, short circuits and earth faults for the XG12 chassis. A 20A circuit breaker for each circuit is also required. All three power cords must be plugged into their single phase 200-240VAC, 50Hz/60Hz power sources at the same time for correct operation of the chassis. **Note**: The chassis power supplies are interlocked with the rear cover which must be installed for them to be enabled. After removing or installing the rear panel, ensure thumbscrews have been tightened down with a 'Flat Blade' screwdriver. **Note**: The load module power is enabled by the Ixia server program. If it is not running, the load modules will not be powered on.
Power Cords	All three power cords are required to operate the XG12 chassis power supplies. Power Cord shipments: • Ixia provides three power cords that are configured and rated to meet the specifications of the target country where the chassis is being installed • For North American customers, the power cords have NEMA L6-20P plugs for attachment to the power source and IEC-60320-C19 connectors that attach to the XG12 chassis • For International shipments, the power cords supplied has plugs suitable for each destination country's power source and IEC-60320-C19 connectors that attach to the XG12 chassis • The XG12 chassis is CE marked and UL™ certified when using the 200-240VAC power cords supplied with the chassis. However, these certifications for the chassis safety approvals are only valid when the unit is operating from all three 200-240VAC main power sources

Chassis Weights	**Frame**: • 64 lbs. (29.1 kg) empty, component weight • 97 lbs. (44.1 kg) average shipping weight (with filler panels) **Fan module**: • 10.2 lbs. (4.63 kg) component weight • 17.3 lbs. (7.86 kg) average shipping weight **Power Supply module**: • 28 lbs. (12.72 kg) component weight • 35.1 lbs. (15.95 kg) average shipping weight **Processor module**: • 2.7 lbs. (1.23 kg) component weight • 8.5 lbs. (3.86 kg) average shipping weight **Warning**: Total chassis weight, without any load modules installed is 104.9 lbs. (47.6 kg). Do not attempt to lift the fully assembled chassis.
Fan Module	Field replaceable chassis fan assembly that is easily installed and removed.
Air flow Clearance	12 inches is required at the rear of the chassis. 24 inches of clearance is preferred.
Power Supply Module	Field replaceable power supply module that is easily installed and removed. There are three 2825W power supplies in the Power Supply Module. Each power supply may be removed or replaced separately.
Timing Sources	Internal clock, synchronized with another Ixia chassis, GPS AFD-1unit, AFD2 IRIG-B unit or with the Timing Distribution Module.
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Operating temperature	41×F to 104×F, (5×C to 40×C) **Note**: Some high-density/high performance load modules require a lower maximum ambient operating temperature than the standard for the chassis. When a load module that requires the lower maximum operating temperature is installed in an XM chassis, the maximum operating temperature of the chassis is adjusted downward to match the maximum operating temperature of the load module. The operating temperature range specification is specified in the published datasheet for these load modules.
Storage temperature	41°F to 122°F, (5°C to 50°C)
Operating Humidity	0% to 85%, non-condensing

Storage Humidity	0% to 85%, non-condensing
Noise	The XG12 chassis running at maximum fan speed capacity may produce noise levels up to 86.5 dB(A). This is measured per the GR-63-CORE, Issue 1, paragraph 5.6.3 specification. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recommended maximum exposure levels for noise and ear protection devices. Shown below are the maximum XG12 chassis sound levels measured according to GR-63-CORE, Issue 1, Paragraph 5.6.3. • Front: 83.5 dB(A) • Left Side: 84.2 dB(A) • Rear: 86.5 dB(A) • Right Side: 84.4 dB(A)

Hearing Protection: The XG12 chassis generates noise levels above 80 dB(A). Ear protection must be worn. The use of appropriate ear protection is recommended to protect against hearing impairment. Consult local health and safety regulations for recommended maximum exposure levels for noise and ear protection devices.

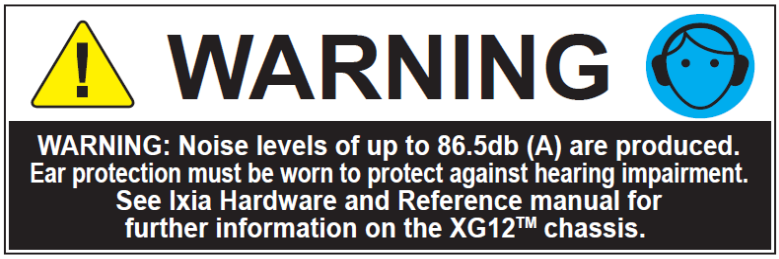
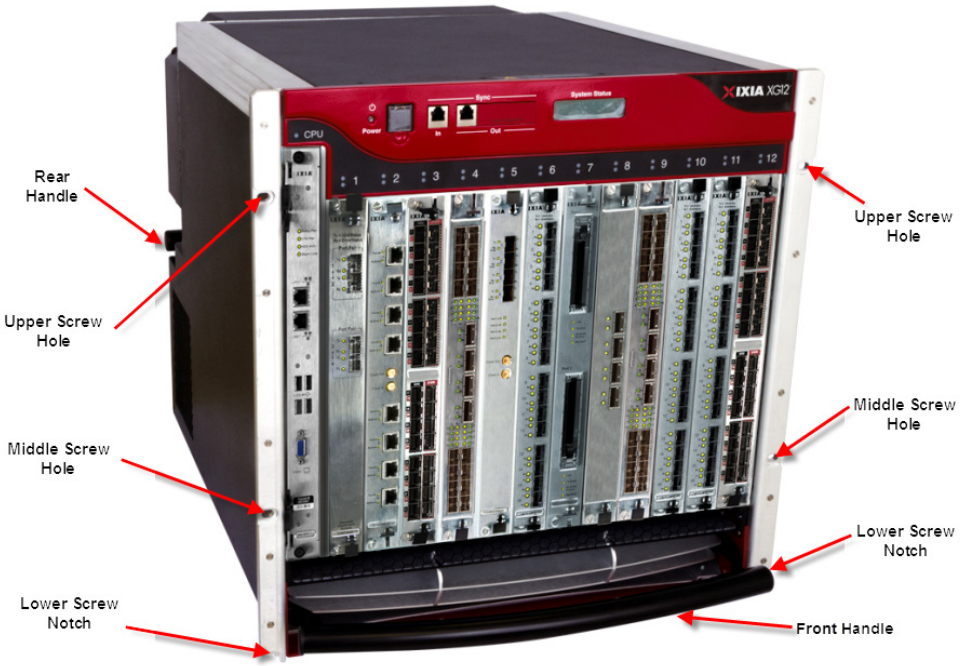


Table 6-4. XG12 Chassis controls and indicators

Front Panel Switches	On/Off momentary power push button
Monitor	HD-DB15 Super VGA
Ethernet	Two RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port.
USB	4 USB dual type A, 4-pin jack connectors
Sync In	Single Sync In jack with a 4-pin RJ11
Sync Out	Single Sync Out jack with a 4-pin RJ11
Front Panel Indicators	See *LEDs/LCD Display*.
	2 Paired LEDs above each slot position indicating Power and Active status.
	2x16 LCD on front panel indicating chassis information.

Figure 6-2. Safety Features



XG12 chassis installation precautions:

- The chassis should be installed in the rack before installing the power supply module, fan module and load modules, thereby reducing the weight of the chassis.

- The two lower bolts used to secure the chassis to a rack can be used to hold the chassis frame in place while securing all of the other bolts (See Figure 6-2).
- Secure the chassis to rack face with all six bolts. Fully depress power supply clamps when installing power supply module.
- Secure the power supply module thumb bolt when installing power supply module.
- Install the rear power supply cover before applying AC power.

  Note: After removing or installing this cover, ensure that the thumbscrews are tightened down with a 'Flat Blade' screwdriver.
- Do not use the chassis without installing the Fan module.
- Do not use the chassis without installing the Processor module.
- Do not leave unused slots open. Use the filler panels to cover the un-used slots. See Installing Filler Panels for more information.
- Do not block the front air intake.
- A minimum air flow clearance of 12 inches is required. 24 inches of air flow clearance is preferred at the rear of the chassis.
- Operator intervention may be required to power cycle the XG12 chassis or restart a software program in the event the XG12 chassis operation is upset or stopped by electrostatic discharge.

LEDs/LCD Display

The XG12 chassis has front panel LEDs for each load module slot.

Table 6-5. XG12 LEDs

Label	Color	Description
Power	Green	When the Power LED is flashing, the board is being detected or initialized. The Power LED is illuminated when the board is powered..
In Use	Green	The Active LED is illuminated when a user has taken ownership of the load module.

LCD Display

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, master/subordinate, and chassis status.

CPU Slot LED Definitions

The specifications of LEDs for the Processor module and the LEDs above the Processor module slot are shown in the following table:

ESD Discharge Warning: Operator intervention may be required to power cycle the unit or restart a software program in the event the unit is upset by electrostatic discharge.

Table 6-6. LED Specifications

	LED	Color	Description
On the chassis front face	CPU card Slot LED	Yellow	The backplane is initializing.
		Green	The backplane has initialized
Processor module - front panel	Stdby Pwr LED	Green	5V Stand-by power is available
	CPU Pwr LED	Green	CPU Card power is available
	HDD Act LED		
	Bkpln Link LED	Green	PCIe link to backplane is up
Processor module - Ethernet LEDs for each management port	Link LED	Green	Port has link
	Act LED		Flashes when port has activity

Supported Modules

The modules that are supported on the XG12 are listed in the following table.

Table 6-7. Supported Modules

Family	Module	Function
XM Form Factor (XMFF) load modules	Xcellon-Flex™ High density 10GbE products	• Xcellon-FlexAP10G16S 10 Gigabit Ethernet LAN Load Module, L2-7 Accelerated Performance, a 1-slot module with 16-ports of SFP+ interfaces • Xcellon-FlexFE10G16S 10 Gigabit Ethernet LAN Load Module, L2-3 Full Emulation Performance, a 1-slot module with 16-ports of SFP+ interfaces
	Xdensity™ Ultra-high density 10GbE	Xdensity, XDM10G32S, Ultra-high density, 10-Gigabit Ethernet load module with 32-ports of SFP+ interfaces and L2-3 data plane support
	Xcellon-Flex™ High density 10GbE and 40 GE products	• Xcellon-FlexAP10/4016SQ 10/40 Gigabit Ethernet Accelerated Performance Load Module, 16-Ports of SFP+ interfaces and 4-ports of QSFP 40 GE interfaces with full performance L1-7 support • Xcellon-FlexFE40G4Q 40 Gigabit Ethernet Full Emulation Load Module, 4-ports of QSFP 40 GE with L1-3 support
	K2 Higher Speed Ethernet product line	• HSE40GETSP1-01, 40-Gigabit Ethernet Load Module, 1-port, 2-slots, with the CFP MSA interface • HSE100GETSP1-01, 100- Gigabit Ethernet Load Module, 1-port, 2-slots, with the CFP MSA interface • HSE40/100GETSP1-01 Dual-Speed, 1-port, 2-slots, with CFP MSA interface • HSE40/100GETSPR1-01, Dual Speed, 40 and 100-Gigabit Data Plane Ethernet Load Module, 1-port, 2-slots, with the CFP MSA interface • HSE40GEQSFP1-01, 40-Gigabit Ethernet Load Module, 1-port, 1-slot with the QSFP+ pluggable interface for multimode fiber, 850nm, or QSFP+ copper cables
	Xcellon Ultra™ High Performance Application Test product line	Xcellon-Ultra NP-01, Application Network Processor Load Module, 1-10G XFP port and/or 12-Ports of Dual-PHY (SFP fiber and RJ45 copper) 10/100/1000 Mbps

Table 6-7. Supported Modules

Family	Module	Function
	NGY High Density 10 Gigabit Ethernet product line	• LSM10GXMR2/4/8-port, reduced performance, load modules with the XFP interface • LSM10GXM2/4/8XP-port, Extra performance, load modules with the XFP interface • LSM10GXM2S/4S/8S-port, Extra performance, load modules with the SFP+ interface • LSM10GXM2S/4S/8S-port, reduced performance, load modules with the SFP+ interface • LSM10GXM2GBT/4GBT/8GBT-port, Extra performance, load modules with the 10GBASE-T interface • LSM10GXM2GBT/4GBT/8GBT-port, reduced performance, load modules with the 10GBASE-T interface
	Fibre Channel load module products	• FCMGXM4S-01, 4-Port Fibre Channel Load Module, with 2Gbps, 4Gbps, and 8Gbps support, SFP+ interface • FCMGXM8S-01, 8-Port Fibre Channel Load Module, with 2Gbps, 4Gbps, and 8Gbps support, SFP+ interface
	ImpairNet Load module products	• ImpairNet EIM1G4S Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces • ImpairNet EIM10G4S 10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces
	Voice Quality module	VQM0001, Resource module, for real time quality of voice measurement. Must purchased with VQM0001-B1, Solution Bundle, Resource module with IXLOAD-PESQ and IXLOAD-AUDIO-CODECS software license
	NGY NP High Density 10GbE Application Test product line	• NGY-NP8-01, 10 Gigabit Application Network Processor Load Module, 8-Port LAN/WAN, SFP+ interface • NGY-NP4-01, 10 Gigabit Application Network Processor Load Module, 4-Port LAN/WAN, SFP+ interface • NGY-NP2-01, 10 Gigabit Application Network Processor Load Module, 2-Port LAN/WAN, SFP+ interface

Table 6-7. Supported Modules

Family	Module	Function
	High Density Gigabit Ethernet product line	• LSM1000XMVDC 4/8/12/16-port, full performance, load modules with dual-phy SFP fiber and 10/100/1000Mbps RJ45 copper • LSM1000XMVR4/8/12/16-port, reduced performance, load modules with dual-phy SFP fiber and 10/100/1000Mbps RJ45 copper • LSM1000XMSP12-01, Gigabit Ethernet, Load Module, 12-Ports Dual-PHY (SFP fiber and RJ45 copper) 10/100/1000 Mbps
Standard Form Factor (SFF) load modules for XG12 chassis **Note**: Requires 944-0007 Adapter Card for XM Chassis installations	Gigabit Ethernet TX, TXS, STX and STXS products	• LM100TX8, 100MB Ethernet Load Module, 8-Port 10/100Mbps, L2-3 data plane support only • LM100TXS8, 10/100Mbps Ethernet Load Module, 8-Port RJ45, 64MB Port CPU memory • LM100TXS2, 10/100Mbps Ethernet Load Module, 2-Port RJ45, 64MB Port CPU memory • LM1000STX4, Gigabit Ethernet Load Module, 4-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, L2-3 data plane support only • LM1000STX2, Gigabit Ethernet Load Module, 2-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, L2-3 data plane support only • LM1000STXS2, Gigabit Ethernet Load Module, 2-Port Dual-PHY (RJ45 and SFP) 10/100/1000 MbpsLM1000STXS4-256, Gigabit Ethernet Load Module, 4-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps
	10 Gigabit Ethernet LSM products	• LSM10G1-01, 10 Gigabit Ethernet Load Module, 1-Port, Full L2-7 support, requires interface adapter module Interchangeable interface adapter modules for SFP+, 10GBASE-T, XENPAK, X2, and CX4 interfaces for the LSM10G1-01
	Application and Encryption Test product line	• AFM (Auxiliary Function Module): AFM1000SP-0 • ALM (Application Load Module): ALM1000T8 • ELM (Encryption Load Module): ELM1000ST2 • Gigabit Ethernet Content Processing Module (CPM), 8-port RJ-45 10/100/1000 Ethernet

Table 6-7. Supported Modules

Family	Module	Function
	10-Gigabit UNIPHY and MacSec products	• MSM10G1- 10 Gigabit Ethernet OC192 Load Module, 1-port Multi Services Module with an XFP interface, supports 10GE LAN/WAN and optional OC-192c POS • LSM10GMS1-01, 10 Gigabit Ethernet Load Module, 1-Port, LAN/WAN, Full performance and supports 802.1ae Media Access Control Security (MacSec) L2 security, including GCM/AES128
	Packet over SONET and ATM products	• MSM2.5G1-01, OC48 Load Module, 1-Port 2.5G Multi Service Module supporting OC48c, Supports POS, Full L2-7 support • LM622MR, OC3/OC12 ATM/POS, Load Module, 2-port ATM/Packet over SONET (POS); Full L2-7 Support. Supports 622 and 155 Mbps data rates • LM622MR-512, OC3/OC12 ATM/POS, Load Module, 2-port ATM/Packet over SONET (POS), Full L2-7 Support. Supports 622 and 155 Mbps data rates, 512MB Port CPU memory • OC3OC12PHY, OC3/OC12 ATM/POS Adapter, Dual-SC optical connector, Single-port OC-3/OC-12 PHY 1310nm Multimode; For the LM622MR or LM622MR-512) load modules
	Power over Ethernet (IEEE802.3 af)	• PLM1000T4-PD (20W), Gigabit Ethernet Load Module, 4-Port PoE, supports 10/100/1000 Mbps Ethernet, and emulates up to 4 powered devices • LSM1000POE4-02 (30W), Gigabit Ethernet Load Module, 4-Port PoE, supports 10/100/1000 Mbps Ethernet, and emulates up to 4 powered devices

Hot-Swap Procedure

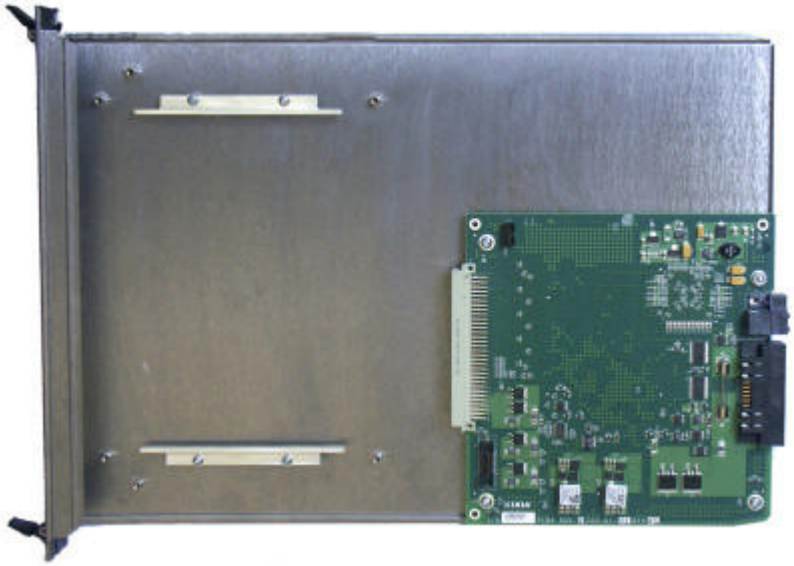
Each XG12 chassis provides the ability of removing and reinstalling a load module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or remaining load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D Hot-Swap Procedure.

SFF Adapter Module

The XG12 adapter module allows Ixia Standard Form Factor (SFF) load modules to be adapted into the XG12 chassis. Figure 6-3 shows an SFF adapter module.

Figure 6-3. SFF Adapter



A SFF load module is inserted into the front of the adapter and connects to the pins in the rear of the adapter. The entire assembly can then be inserted into any XG12 chassis slot.

Once an adapter module is installed in a chassis, SFF load modules can be hot-swapped without removing the SFF load module from the chassis.

Figure 6-4 shows an SFF Adapter module with a legacy ATM card.

Figure 6-4. SFF Adapter with ATM Module

Table 6-7 identifies the modules that can be used with the SFF Adapter.

Cooling Fan Speed Control

The XG12 chassis automatically monitors and measures the temperature of installed load modules. The XG12 automatically adjusts the fan speed to maintain proper cooling.

Rack Mount Cautions

Caution: If this unit is installed in a network equipment rack, please observe the following precautions.

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or the front of the chassis, and leave approximately 12 inches of space, 24 inches preferred, for the back of the unit for proper ventilation. The air flow clearance should be 12 inches on the front.

c: Mechanical Loading: Mount the chassis so that is it level in the rack and that a hazardous condition is not caused. Please install all six mounting bolts.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In Addition, Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

f: Replacement of the power supply cord must of the same type cord and plug configuration that was shipped with the unit.

7 Optixia X16 Chassis

This chapter provides details about Optixia X16 chassis—its specifications and features.

The Optixia X16 Chassis has 16 slots for support of up to 16 single wide load modules. The Optixia X16 supports all high power load modules with enhanced power supplies and cooling. The Optixia X16 was specifically designed to allow the hot-swapping of modules, without requiring a restart of the chassis. The Optixia X16 is shown in *Figure 7-1*.

Caution: This equipment is intended to be installed and maintained by Service Personnel.

Figure 7-1. Optixia X16 Chassis

The Optixia family of chassis has improved data throughput between Load Modules and the chassis. Two methods of data throughput improvements is used: High Speed IxBus and Module to Module data transfer.

The Optixia chassis provides improved modularity of major components to reduce downtime of a failed chassis and reduce the probability of needing to remove a failed chassis from the test environment. Among the modular features provided are:

- Power supplies
- Motherboard and support components (RAM, Hard Drive)
- Backplane power control and interface

Each of the modular components is capable of being removed in the field and replaced with minimum downtime for the customer.

Note: In the event of indications of inadequate power, remove load modules starting from the low-number slots (slot 1, 2, 3), then working upward toward slot 16 until the problem is solved.

Warning: To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Specifications

X16 Chassis

Optixia X16 computer and chassis specifications are contained in *Table 7-1*.

Table 7-1. Optixia X16 Specifications

CPU	Intel Pentium 4, 3.0 GHz
	**Caution-Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	2 GB
Disk	80GB Sata Disk DVD Drive
Operating System	Windows XP Professional
Physical	
Load Module Slots	16
Size	17.5"w x 14.5"h x 20.5"d (44.5cm x 36.8cm x 52.1cm)
Weight (empty)	47lbs (21kg)
Avg. Shipping Wt.	51lbs (23kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted.
Power	100-240V 60/50Hz 16-8A

Table 7-1. Optixia X16 Specifications

	Caution: The X16 unit requires the building installation to be fitted with a separate circuit fitted with a 20A circuit breaker.
	Caution: The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.
	Caution: Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.
Front Panel Switches	On/Off momentary power push button
Front Panel Connectors	
Mouse	PS/2 6-pin DIN for external mouse
Keyboard	PS/2 6-pin DIN for external keyboard
Monitor	HD-DB15 Super VGA for external monitor
Printer	Female DB25 parallel port for external printer
Ethernet	RJ-45 10/100/1000Mbps Gigabit Ethernet Management Port
Serial	2 male DB9 ports
USB	4 USB dual type A, 4-pin jack connectors
Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Line In/Line Out/Mic	3.5mm mini-TRS stereo jacks
Back Panel Switches/ Connectors	Power On/Off rocker switch
Power	Male receptacle (IEC 60320-C19)
Front Panel Indicators	See *LEDs/LCD Display* on page 5
	2 Paired LEDs above each slot position indicating Power and Active status
	LCD on front panel to display chassis information

LEDs/LCD Display

The Optixia X16 has the following set of front panel LEDs, for each load module slot:

Table 7-2. Optixia X16 LEDs

Label	Color	Description
Power	Green	For each load module slot, the Power LED is illuminated when the board is being powered. When the Power LED is flashing, the board is being detected or initialized.
In Use	Green	For each load module slot, the In Use LED is illuminated when a Load Module in a particular slot is owned by you.

LCD Display

An LCD display is provided on the chassis to indicate the status of the chassis without an external display device (monitor). The LCD operates in two modes:

- Startup: The LCD displays messages from IxServer to indicate the operation of IxServer as it initializes.
- Run: The LCD display provides chassis information. Information displayed includes chassis name, IxOS version, IP address, and chassis status.

Supported Modules

The modules that are supported on the Optixia X16 are listed in *Table 7-3*.

Table 7-3. Optixia X16 Supported Modules

Gigabit Ethernet TXS family	10/100/1000 Ethernet Load Modules
TXS8	10/100 Ethernet Load Module
ALM1000T8	Special 10/100/1000 Ethernet Load Module
CPM1000T8	Special 10/100/1000 Ethernet Load Module
ELM1000ST2	Special 10/100/1000 Ethernet Load Module
LM622MR	ATM/POS Load Module
LSM1000POE4-02	4-port PoE Load Module
2.5G MSM POS	OC-48c Load Module
10GE LSM	10 Gigabit Ethernet Load Module, including 10GE LSM MACSec
10G MSM	LAN/WAN/POS Multimode Load Module
PLM1000P4-PD	Power over Ethernet Load Module

Hot-Swap Procedure

Each Optixia X16 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D, *Hot-Swap Procedure*.

Installing Filler Panels

The airflow in an Optixia X16 chassis can be inefficient if high density load modules are installed in a few slots and the rest of the chassis is left open. For best cooling results, filler panels are required. It is required that filler panels are used in situations where the slots in the chassis are not all in use.

An empty Optixia X16 chassis includes:

- Three 4-slot wide X16 Filler Panel units (p/n 652-0118-01)
- Two 1-slot wide X16 Filler Panel units (p/n 652-0117-01)
- Screws for attaching the panel faceplates to the chassis

Prerequisites for Filler Panel Installation:

- The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.
- The chassis should be placed in a horizontal position, in a well-lighted work area.

Filler Panel Installation Procedure:

ESD Caution: Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

1. To install a 4-slot filler panel:

   Example: Slide the 4-slot filler panel, with the Ixia logo at the top, into Slots 1 through 4. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with 4 of the supplied screws.

2. .To install a 1-slot filler panel:

   Example: Slide the 1-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with 2 of the supplied screws.

Caution: Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

Not using filler panels could cause random failures in port operations or damage installed modules..

Rack Mount Cautions

Caution: If this unit is installed in a Rack Mount, observe the following precautions:

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced. Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Chassis frame should be screwed down to racks to ensure proper grounding path. In Addition, Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

f: Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.

8 Optixia XL10 Chassis

This chapter provides details about Optixia XL10 chassis—its specifications and features.

Optixia XL10 is a highly modular design intended for long-term continuous use and ease of maintenance. The modular design allows for the replacement of load modules and power supplies without the need to take the chassis offline. The number and position of load modules may similarly be changed without taking the chassis offline. All of the critical components of an Optixia XL10 chassis may be removed without removing the chassis from its rack mount. Upgrades to the power supply and processing components are also possible through simple module interchange while the Optixia XL10 remains rack mounted.

The chassis supports 240 ports of 10/100/1000Mbps modes.

The Optixia XL10 chassis has 10 slots for Optixia XL10 Load Modules. The Optixia XL10 power is organized with two separate AC inputs which in turn feed 1-4 1200W power supplies. To use Optixia XL10 in a minimal power configuration, power supplies number 1 and 2 are installed for use with up to 5 blades. Power supplies number 3 and 4 are installed for use with all 10 blades.

Note: In the event of indications of inadequate power, remove load modules starting from the low-number slots (slot 1, 2, 3), then working upward toward slot 10 until the problem is solved.

Caution: This equipment is intended to be installed and maintained by Service Personnel.

The Optixia XL10 is shown in *Figure 8-1* on page 8-2.

Warning: To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Figure 8-1. Optixia XL10 Chassis

Warning Multiple Sources of Supply. Disconnect All Sources before Servicing	**Avertissement** Présence de plusieurs sources d'alimentation électrique. Débrancher toutes les sources d'alimentation avant intervention	**Achtung** Mehrfachstromquellen! Alle Versorgungskabel vor Wartung entfernen.	警告 複数のパワーサプライがありますので、保守する際には必ず全ての電源ケーブルを抜いてください

Warning High Touch Current. Earth Connection Essential Before Connecting Supply	**Avertissement** Fort courant de contact Raccordement à la Terre impératif Avant branchement de l'alimentation	**Achtung** Stellen Sie eine sichere Erdverbindung her, bevor Sie die Stromquelle anschließen.	警告 高漏洩電流に気を 付け、適切に設置 してから電源を 接続してください

Specifications

XL10 Chassis

Optixia XL10 computer and chassis specifications are contained in *Table 8-1*.

Table 8-1. Optixia XL10 Specifications

CPU	Intel Celeron 1.2 GHz
	**Caution-Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	2 GB
Disk	IDE disk: 20 GB, removable
Operating System	Windows XP Professional
CD-ROM	Integrated CD-ROM drive
Physical	
Load Module Slots	10
Size	17.5”w x 35.5”h x 22.5”d (44.5cm x 90.5cm x 57.5cm)
Weight (empty)	150lbs (68kg)
Avg. Shipping Wt.	160lbs (72.5kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	10% to 90%, non-condensing
Storage	5% to 95%, non-condensing
Power	Line cord 1: 200-240V 60/50Hz 15A Line cord 2: 200-240V 60/50Hz 15A **Note**: Both power cords must be connected to the AC power source to provide sufficient power to the chassis.

Table 8-1. Optixia XL10 Specifications

	Caution: The socket/outlets used to power the unit must be installed near the equipment and be easily accessible because the power plug may be used to disconnect the unit from the power source.
	Caution: The chassis' safety approvals (UL and CE) are only valid when the unit is operating from 200-240VAC mains.
	Caution: Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.
Clearance	Front and Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted
Front Panel Switches	On/Off momentary power push button
Front Panel Indicators	System Power (behind sliding door) LEDs: System System Ready System Fault System Temperature CPU Power Standby Power GPS Enabled* Time Stamp 1, 2, 3* Satellite Lock* Arm OK Lock Sync Master Ext. Sync. CDROM * = optional features
Front Panel Connectors	
Mouse	PS/2 6-pin DIN with or without Y-connector, for external mouse
Keyboard	PS/2 6-pin DIN with or without Y-connector, for external keyboard
Video	HD-DB15 Super VGA for external monitor
Parallel (Printer)	Female DB25 parallel port for external printer
10/100 Ethernet	RJ-45 10/100Mbps Fully integrated PC with 10/100 NIC.
Com 1 (Serial)	1 male DB9 serial port
USB	4 USB dual type A, 4-pin jack connectors

Table 8-1. Optixia XL10 Specifications

Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Trigger In	BNC
Power	2 male receptacles (IEC 60320-C19)

Supported Modules

The modules that are supported on the Optixia XL10 are listed in Table 8-2..

Table 8-2. Optixia XL10 Supported Modules

Module	SFF - Requires Adapter	Function
OLM1000STXS24		24-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Optixia XL10 full-featured Load Module (does not include transceivers)
OLM1000STX24		24-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Ethernet Optixia XL10 Load Module (does not include SFP transceivers); Reduced features - NO support for routing protocols, Linux SDK, and L4-7 applications
LSM10GXL6-02		6-port 10GE LAN/WAN, single slot, full featured load module for Optixia XL10. Supports routing/bridging protocols, Linux SDK, and L4-7 applications. Requires 6 XFP transceivers (not included - options are either 948-0003 (XFP-850), XFP-1310, or XFP-1550)

Hot-Swap Procedure

Each Optixia XL10 chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis.

The hot-swap procedure is detailed in Appendix D, *Hot-Swap Procedure*.

Installing Filler Panels

The airflow in an Optixia XL10 chassis can be inefficient if a load module is installed in one slot and the other is left open. For best cooling results, filler panels are required. Filler panels must be used in situations where the slots in the chassis are not all in use.

An empty Optixia XL10 chassis includes:

- 7 ea. 1 slot wide XL10 Filler Panel/Air Baffle units (p/n 652-0517)

Prerequisites for Filler Panel Installation:

The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.

Filler Panel Installation Procedure:

ESD Caution: Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

Example: Slide the one-slot filler panel, with the Ixia logo at the top, into the correct slot. The panel slides in on the slot rails in the chassis. Secure the faceplate of the filler panel to the chassis with two of the supplied screws.

Caution: Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

Not using baffles could cause random failures in port operations or damage installed modules.

Rack Mount Cautions

Caution: If this unit is installed in a Rack Mount, observe the following precautions:

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced.
Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

f: Replacement of the power supply cord must be conducted by a Service Person. The same type cord and plug configuration shall be utilized.

9 IXIA 1600T Chassis

This chapter provides details about Ixia 1600T chassis—its specifications and features.

The Ixia 1600T Chassis has 16 slots for support of up to 16 single wide load modules, or eight double-wide load modules. The Ixia 1600T supports all high power load modules with enhanced power supplies and cooling. The Ixia 1600T was specifically designed to support OC-192c and 10 Gigabit Ethernet load modules. The Ixia 1600T is shown in the following figure.

Figure 9-1. Ixia 1600T Chassis

Warning: To prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Specifications

1600T Chassis

Ixia 1600T computer and chassis specifications are contained in the following table.

Table 9-1. IXIA 1600T Specifications

CPU	Intel Celeron 1.2Ghz
	**Caution-Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	1 GB
Disk	IDE disk: 20 GB
Operating System	Windows XP Professional
Physical	
Load Module Slots	16
Size	17.5”w x 15.7”h x 20.4”d (44.5cm x 39.9cm x 52cm)
Weight (empty)	47lbs (21kg)
Avg. Shipping Wt.	51lbs (23kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Bottom: 1 in (2.5cm). Top and sides: none.
Power	100-240V 60/50Hz 16-10A

Table 9-1. IXIA 1600T Specifications

Fuse	250V 20A Fast Acting
Front Panel Switches	On/Off momentary power push button
Back Panel Switches	On/Off rocker switch
Front Panel Indicators	Power, Standby, Master, External Clock See *LEDs* on page 5.
Back Panel Connectors	
Power	Male receptacle (IEC 60320-C19).
Mouse	PS/2 6-pin DIN with or without Y-connector, for external mouse.
Keyboard	PS/2 6-pin DIN with or without Y-connector, for external keyboard.
Monitor	HD-DB15 Super VGA for external monitor.
Printer	Female DB25 parallel port for external printer.
Ethernet	RJ-45 10/100Mbps
Serial	2 male DB9 ports
USB	2 USB dual type A, 4-pin jack connectors.
Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Audio Line In Line Out Mic In	3 3.5mm mini-TRS
Trigger In	BNC

LEDs

The IXIA 1600T has the following set of front panel LEDs:

Table 9-2. IXIA 1600T LEDs

Label	Color	Description
Power	Green	The power LED is illuminated when the chassis is using power.
Standby	Yellow	The standby LED indicates that the chassis is in standby mode. Standby mode is defined as: the chassis is plugged into an active power outlet, the chassis power block switch is active (or 'On'), and the system power is not on. Pressing the front panel Power On/Off button enables system power and start the system.
Master	Green	This LED is illuminated during chassis power up. After IxServer is loaded, the LED is only illuminated when the chassis is enabled in Master Mode. Master Mode indicates that the chassis operates based on its local system clock and it is not dependent upon any external synchronization. In a chassis chain this LED is illuminated on the first chassis in the chain. All other chassis downstream receive their clock from the Master chassis and therefore does not illuminate this LED.
External Sync	Green	This LED is illuminated during chassis power up. After the IxServer load the LED is only illuminated when the chassis detects an external synchronization clock. The external synchronization clock is used to synchronize to an adjacent chassis when defining a chassis chain. This LED does not indicate that a chassis is a device in a chain. It only indicates that a clock signal has been detected on the line.

Installing Filler Panels

When using the IXIA 1600T for fewer than eight OC192 modules, it is best to redirect the airflow to the installed load modules to optimize operating conditions. Consequently, 1-slot and 4-slot 1600T cover plates have been designed to redirect the airflow to the installed load modules from empty slots.

The following components are included with each IXIA 1600T:

- Three 4-slot wide 1600T Filler Panel units (p/n 652-0118)
- Two 1-slot wide 1600T Filler Panel units (p/n 652-0117)
- Screws for attaching the panel faceplates to the chassis

Prerequisites for Filler Panel Installation:

Warning: Power to the chassis must be OFF.

- The technician should use industry-standard grounding techniques, such as wrist and ankle grounding straps, to prevent damage to electronic components on any Ixia Load Modules.
- The chassis should be placed in a horizontal position, in a well-lighted work area.
- The Load Module(s) must have been previously installed, per the instructions before application of power.

Insert one or more OC192 or 10GE modules into the chassis. Other load modules may be installed at any location

Table 9-3. Slot Preferences for Installing Multiple OC192 Load Modules

Module	Slots	Filler Panels Required
1st	11 & 12	(3) 4-slot and (2) 1-slot
2nd	5 & 6	(3) 4-slot
3rd	8 & 9	(2) 4-slot and (2) 1-slot
4th	14 & 15	(1) 4-slot and (4) 1-slot
5th	2 & 3	(6) 1-slot
6th	1 & 2	(4) 1-slot (shift the 5th module to slots 3 & 4)
7th	7 & 8	(2) 1-slot (shift the 3rd module to slots 9 & 10)
8th	13 & 14	None (shift the 4th module to slots 15 & 16)

The filler panels are required when there are empty slots in the chassis. However, any other Ixia load modules, such as 10/100, Gigabit, OC12/3c, and OC48c, can be installed in the chassis, alongside the OC192c load modules. First, insert the OC192c load modules into the respective slots, as described in the second column of the table above. Second, install any other load modules in any empty slots. Last, fill the remaining slots with the filler panels.

Filler Panel Installation Procedure:

ESD Caution: Use industry-standard grounding techniques to prevent Electrostatic Damage to the delicate electronic components on the Ixia Load Modules.

To install a filler panel, do the following:

1. Verify that the chassis is powered **OFF** and the power cable is unplugged.
2. To install a 4-slot filler panel, slide the 4-slot filler panel, with the Ixia logo at the top, into Slots 1 through 4, or as indicated in the Slot Preference table above.

The panel slides in on the slot rails in the chassis.

3. Secure the faceplate of the filler panel to the chassis with 4 of the supplied screws.
4. To install a 1-slot filler panel, slide the 1-slot filler panel, with the Ixia logo at the top, into the correct slot, per the Slot Preference table above.

   The panel slides in on the slot rails in the chassis.
5. Secure the faceplate of the filler panel to the chassis with 2 of the supplied screws.

Caution: Use extreme care to prevent damage to delicate electronic components on an adjacent load module.

Not using filler panels could cause random failures in port operations or damage installed modules..

Rack Mount Cautions

Caution: If this unit is installed in a Rack Mount, observe the following precautions:

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced.
Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

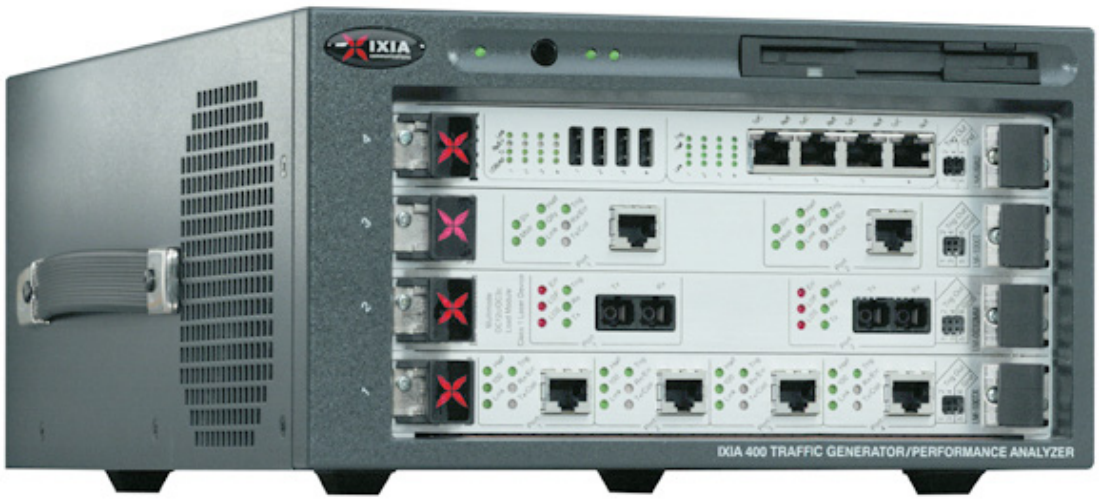
10 IXIA 400T Chassis

This chapter provides details about Ixia 400T chassis—its specifications and features.

The IXIA 400T is shown in Figure 10-1. The IXIA 400T chassis has 4 slots for Ixia Load Modules, but may also be used to support the high-powered load modules, including all OC192 and 10GE modules. The IXIA 400T Chassis is specifically designed to accommodate up to 2 OC192/10GE Load Modules and up to 3 TXS8, TXS4 or SFPS4 Load Modules. It has an enhanced power supply, providing more than twice the power of the original IXIA 400T. Additional cooling fans have been added to the 400T to meet the requirements of the high-powered modules.

Note: The Ixia 400T must only be operated in the horizontal position as shown in Figure 10-1.

Figure 10-1. Ixia 400T Chassis



Warning: In order to prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Specifications

400T Chassis

The computer specifications are contained in the following table.

Table 10-1. IXIA 400T Specifications

CPU	Intel Celeron 1.2Ghz
	**Caution-Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	512 MB
Disk	IDE disk: 250 GB
Operating System	Windows XP Professional
Physical	
Load Module Slots	4
Size	10.25”w x 5.75”h x 16”d (26.1cm x 14.6cm x 40.6cm)
Weight (empty)	10lbs (4.5kg)
Avg. Shipping Wt.	16lbs (7.3kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted.

Table 10-1. IXIA 400T Specifications

Power	100-240 V 60/50 Hz 4-2 A **Note**: The CPU monitors each card's power requirements and refrains from applying power to the backplane if the card's required load would cause the total power to exceed 350W.
Fuse	4.0A 250V Time Lag
Front Panel Switches	Momentary Standby Power push button
Back Panel Switches	Power On/Off rocker switch
Front Panel Indicators	Power, Master, External Clock
Rear Panel Connectors	
Power	Male receptacle (IEC 320-C13)
Keyboard/Mouse	PS/2 6-pin DIN with Y-connector, for external mouse and/or keyboard You **must** use the supplied Y-cable when using the PS/2 mouse.
Monitor	HD-DB15 Super VGA for external monitor
Printer	Female DB25 parallel port for external printer
Ethernet	2 each RJ-45 10/100Mbps Fully integrated PC with 10/100 NIC
Com 2	1 male DB9 serial port
USB	2 USB dual type A, 4-pin jack connectors
Sync In	4-pin RJ11
Sync Out	4-pin RJ11
Trigger In	BNC connector

Use of Filler Panels

Proper cooling of the cards in the Ixia 400T requires that the Ixia 400T chassis is always mounted in a horizontal position and that the filler panels are installed in the unused slots. High powered cards available for use in the Ixia 400T chassis include all variants of the OC192 load modules, all variants of the 10GE load modules, and all variants of the ALM1000T8. Refer to *Installing Filler Panels* on page 5 for instructions on the installation of filler panels.

Rack Mount Cautions

Caution: If this unit is installed in a Rack Mount, observe the following precautions:

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced.
Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

11 IXIA 250 Chassis

This chapter provides details about Ixia 250 chassis—its specifications and features.

The IXIA 250 is a Field Service Unit (FSU) chassis with a built-in 10/100/1000 port and an additional two slots for Ixia Load Modules, which may be high-powered modules. The IXIA 250 is shown in the following figure.

Note: The Ixia 250 must only be operated in the horizontal position as shown in Figure 11-1.

Figure 11-1. IXIA 250 Chassis

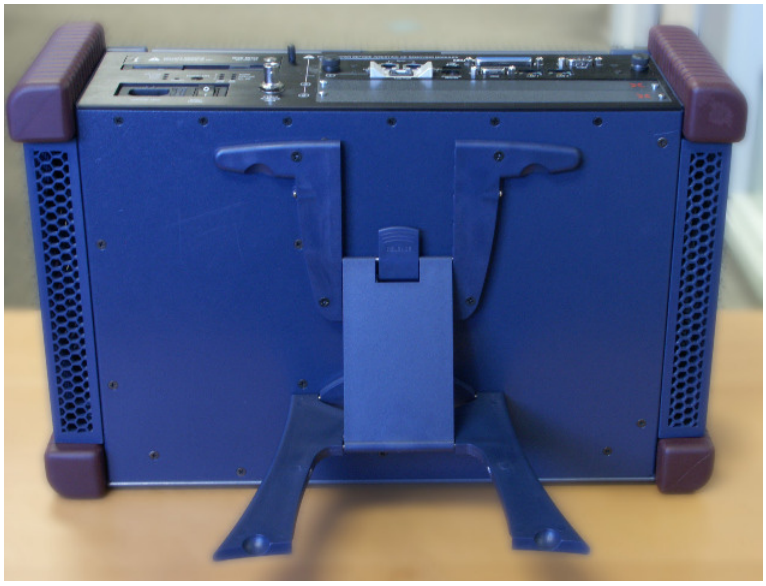
Operation

Setup

The IXIA 250 incorporates an adjustable support, shown collapsed in Figure 11-2 and extended in Figure 11-3.

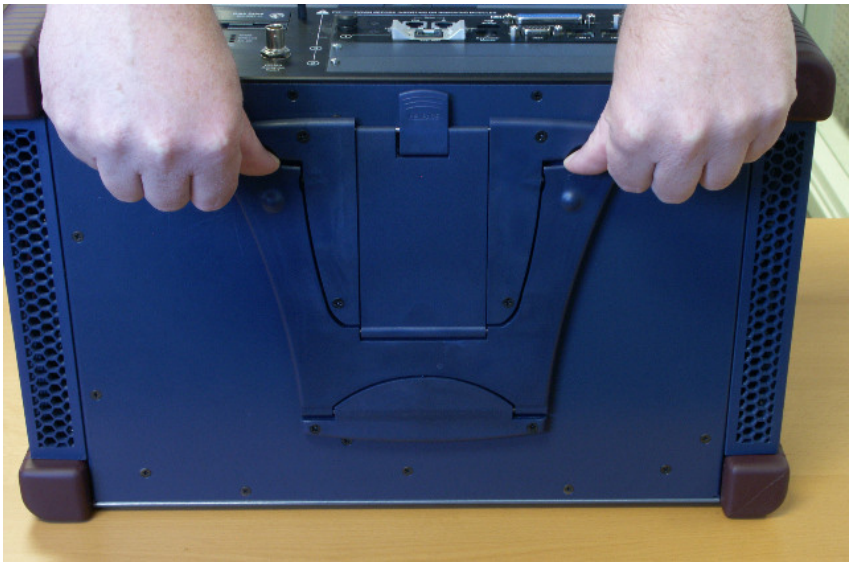
Figure 11-2. IXIA 250 Integrated Support (Collapsed)

Figure 11-3. IXIA 250 Integrated Support (Extended)



The support is extended by placing your thumbs at the upper left and right corners of the cutouts and pushing down as shown in Figure 11-4. Ensure that the stand is stable in one of its available locking positions.

Figure 11-4. IXIA 250 Integrated Support Operation



The keyboard is released by pressing on the button at the top of the chassis, as shown in Figure 11-5.

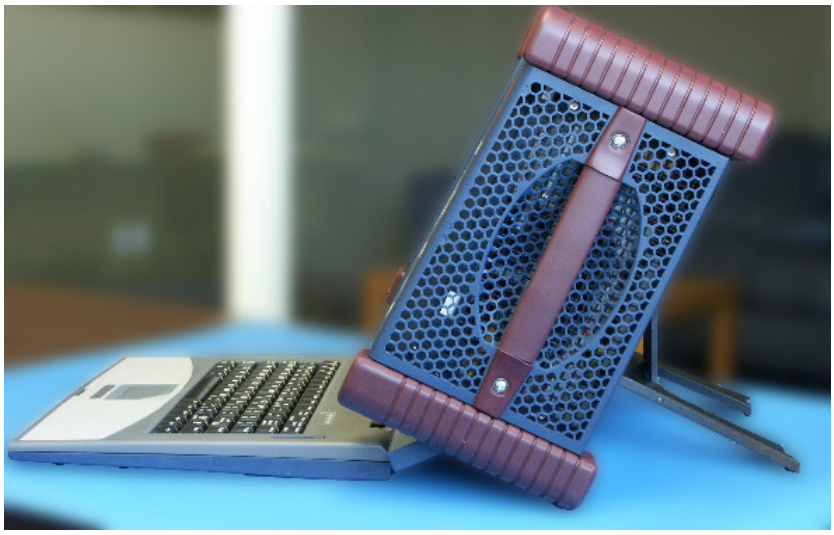
Figure 11-5. IXIA 250 Keyboard Release

Unfold the keyboard and press down on the hinge until it lies flat.

Caution: The Ixia 250 can only be operated in the horizontal position shown in Figure 11-6 on page 11-4.

Warning: In order to prevent accidental injury to personnel, do not leave unused SFP (or SFP+) ports on load modules uncovered. When transceivers are not installed, end caps must be used. For details, see *Use End Caps on Open Ports* on page xxx.

Figure 11-6. IXIA 250 Keyboard



Caution: Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

Power is applied to the unit by plugging it in and toggling the '1/0' switch as shown in the following figure.

Figure 11-7. IXIA 250 Power

This applies power to the chassis, but does not turn on the computer within. The separate *Standby* switch must be pressed, as shown in *Figure 11-8*. This may also be used to put the computer into standby mode at a later time. Should the IXIA 250 experience a power failure, it does not automatically start the operating system.

Figure 11-8. IXIA 250 Standby Switch

Computer Operation

The computer on the IXIA 250 is operated as any other computer system running Windows 2000 Server. The keyboard is used for all typed input. The touchpad at the bottom of the keyboard, as shown in the following figure, is used to position the cursor and click the left and right mouse buttons.

Figure 11-9. IXIA 250 Keyboard and Touchpad

Move around the touchpad, following the cursor on the screen. Use the buttons under the touchpad as you would use the left and right mouse buttons on a

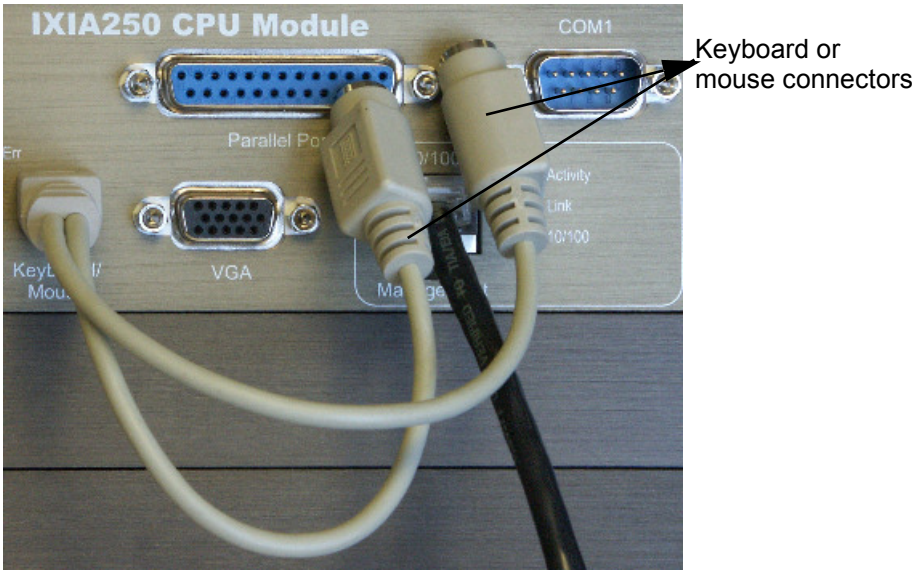
mouse. Double tapping on the touchpad is equivalent to a double-mouse click. Pressing in the shaded area at the top-right of the touchpad is equivalent to a right mouse button click.

The intensity of the LCD screen is controlled by the slide switch at the upper right corner of the keyboard.

In addition to the use of the touchpad, an external mouse may be connected to the *Keyboard/Mouse* port at the back of the chassis. Furthermore, the LCD screen is touch sensitive and may be used as an alternative to the touchpad or mouse. Touching the screen is equivalent to pressing and holding the left mouse button at that point and taking your finger off the screen is equivalent to releasing the mouse button.

An external keyboard may be attached to the *Keyboard/Mouse* port at the back of the chassis. When both an external mouse and keyboard are required, they may be attached with the use of the supplied 'Y' adapter, as shown in Figure 11-10. Attach the keyboard and mouse to either connector.

Figure 11-10. IXIA 250 Keyboard/Mouse 'Y' Adapter



The rear panel of the IXIA 250 contains additional connectors for external devices. This is shown in *Figure 11-12* and further explained in *Table 11-1*.

Table 11-1. IXIA 250 Computer Connections

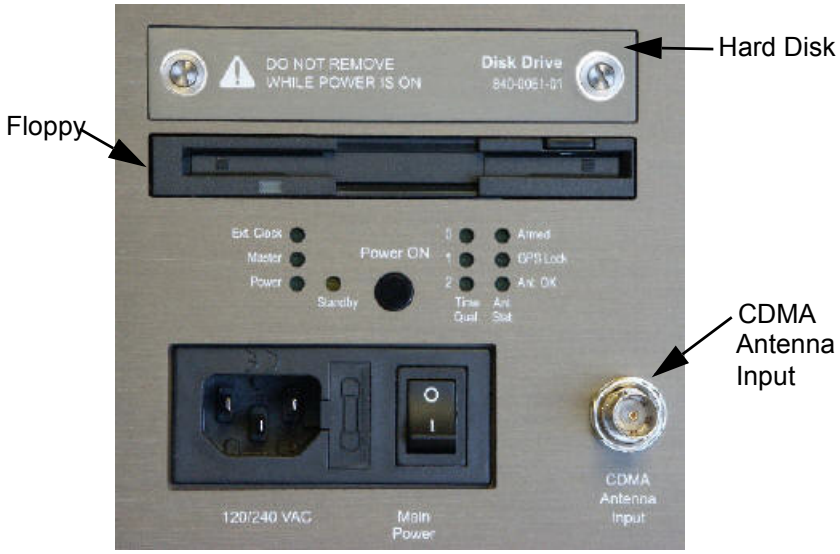
Connector	Usage
Keyboard/Mouse	Used to connect an external mouse and/or keyboard.
VGA	An external monitor may be attached to this connector. The monitor must have at least a 1024 x 768 resolution.
Parallel Port	May be used for an external printer.

Table 11-1. IXIA 250 Computer Connections

COM1	May be used to communicate with an external serial device.
10/100 Management	Two 10/100 Ethernet ports may be used for remote management of the chassis. Three LEDs are provided: *Activity, Link,* and *10/100*. *Link* and *10/100* glow a steady green when link has been established and the port is operating in 100 Mbps mode, respectively. The *Activity* light blinks green as data is sent or received.

A floppy drive and access to the hard disk is provided on the left rear of the chassis, as shown in the following figure.

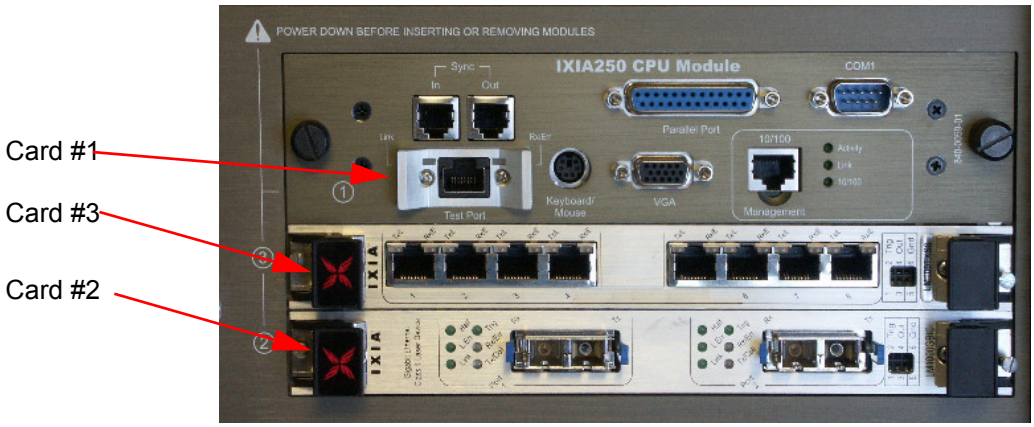
Figure 11-11. IXIA 250 Floppy and Hard Drive Access



Test Operation

Device testing may be accomplished using the built-in port or by plugging in additional Ixia load modules. The following figure shows two additional boards in an IXIA 250 chassis.

Figure 11-12. IXIA 250 with Additional Load Modules



The IXIA 250 accepts any two single-wide or one double-wide load modules. See the remaining chapters of this manual for a discussion of available load modules. When using Ixia software to access the load modules, the cards are numbered as shown in Figure 11-12. That is, the built-in port is card number 1, the lower card in the chassis is card number 2, and the card above that is card number 3.

When the IXIA 250 is ordered with the Gigabit-only option, then one of two optional connectors may be attached to the *Test Port.* The connectors are either copper (RJ-45) or fibre optic SFP module. The module to which the connector is

attached is hot-swappable. Merely press the release tabs on either side of the connector and pull out the connector.

Sync-in/Sync-out connectors are provided to daisy chain the IXIA 250 with other chassis.

When the CDMA option is installed, an appropriate antenna should be attached to the rear panel, as shown in Figure 11-11. Refer to *Ixia 100 Chassis* for a full discussion of the use of the CDMA feature. LEDs are provided to indicate the status of the CDMA time lock; the aforementioned chapter has a discussion of their interpretation.

Specifications

Ixia 250 Chassis

Ixia 250 computer and chassis specifications are contained in Table 11-2.

Table 11-2. IXIA 250 Specifications

CPU	Intel Celeron 850Mhz
	**Caution-Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Memory	512 MB
Disk	Removable IDE disk: 20 GB
Operating System	Windows 2000 Server
Keyboard	Integrated keyboard
Mouse	Integrated touchpad
Integrated Display	12.1 inch TFT active matrix LCD panel • 1024 x 768 resolution • Touchscreen • Adjustable brightness
Physical	
Load Module Slots	2-accepts single or double-wide module
Size	17.5” x 11.25” x 7” (44.5cm x 28.5cm x 17.8cm)
Weight (empty)	20 lb. (9 kg)
Avg. Shipping Wt.	22 lb. (10 kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing

Table 11-2. IXIA 250 Specifications

Storage	0% to 85%, non-condensing
Clearance	Rear: 4 in (10 cm); fan openings should be clear of all cables or other obstructions. Sides: 2 in (5 cm) unless rack mounted.
Power	100-240V 60/50Hz 3.0-1.5A
Fuse	3.15A 250V Fast Acting
Front Panel Switches	LCD brightness slide switch (on built-in keyboard)
Back Panel Switches	Power On/Off rocker switch
	Momentary Power-On switch
Back Panel Indicators	Power, Master, External Clock, CDMA status
Back Panel Connectors	
Power	Male receptacle (IEC 320-C19)
Keyboard/Mouse	1 PS/2 6-pin DIN connector with Y-connector cable, for external mouse and/or keyboard
Monitor	HD-DB15 Super VGA for external monitor
Printer	Female DB25 parallel port for external printer
Ethernet	RJ-45 10/100Mbps dual port
Com 1	Male DB9 serial port
Test port	RJ-45 or SFP
Sync In/Out	two 4-pin RJ11 (provided by Ixia)
CDMA Antenna	BNC connector (only on 250-CDMA)

Test System

The test system specifications are contained in *Table 11-3* on page 11-12.

Table 11-3. IXIA 250 Test System Specifications

Built-in Load Module	One port of LM1000TXS4 load module with 10/100/1000 capability. Refer to *Chapter 16, IXIA 10/100/1000 Load Modules* for a description of the port characteristics. Load module must be ordered with a copper or SFP connector. This port is available as card 1, port 1 in Ixia software.
Load Module Slots	Any of Ixia's single-wide or double-wide modules may be used. Load modules are hot-swappable. These cards are available as cards 2 and 3 in Ixia software.
CDMA	Optional CDMA clock synchronization module.

12 Ixia 100 Chassis

Ixia 100

The IXIA 100 provides the means for accurate worldwide timing using GPS or CDMA antenna inputs. The IXIA 100 chassis has 1 slot for an Ixia Load Module and includes either an integral GPS unit (IXIA 100 GPS) or CDMA unit (IXIA 100 CDMA). The IXIA 100 is shown in the following figure.

Figure 12-1. Ixia 100 Chassis

The IXIA 100 with integrated Global Positioning System (GPS) or Code-Division Multiple Access (CDMA) technology is designed for distributed end-to-end measurements of key metrics, including point-to-point latency and jitter.

IXIA 100 Specifications

The IXIA 100 chassis specifications are contained in the following table.

Table 12-1. Ixia 100 Chassis Specifications

Physical	
Load Module Slots	1
Size	17.5”w x 1.75”h x 20.15”d (44.5cm x 4.5cm x 38.1cm)
Weight	14lbs (6.4kg)
Avg. Shipping Wt.	16lbs (7.3kg)
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 104°F, (5°C to 40°C) **Note**: Some high-density/high performance load modules may require a lower operating temperature; if this is the case, the operating temperature is specified in the load module datasheet.
Storage	41°F to 122°F, (5°C to 50°C)
Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
Power	100-240V 60/50Hz 1.5-0.75A
Front Panel Switches	On/Off momentary power push button
Front Panel Indicators	Power, Satellite Lock, Time Stamp
Front Panel Connectors	
Mouse & Keyboard	PS/2 6-pin DIN
Monitor	HD-DB15 Super VGA
Printer	Female DB25 parallel port
Ethernet	RJ-45 10/100Mbps Fully integrated PC with 10/100 NIC
Com 1	2 male DB9 ports
Back Panel Connectors	
Power	Male receptacle (IEC 320-C19)

Rack Mount Cautions

Caution: If this unit is installed in a Rack Mount, observe the following precautions:

a: Elevated Operating Ambient Temperature: If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient temperature. Therefore, consider installing the equipment in an environment that is compatible with the maximum allowable ambient temperature specified for the chassis (40° C).

b: Reduced Air Flow: Install the equipment in a rack so that the amount of air flow required for safe operation of the equipment is not reduced.
Do not block the back or sides of the chassis, and leave approximately two inches of space around the unit for proper ventilation.

c: Mechanical Loading: Mount the equipment in the rack so that a hazardous condition is not caused due to uneven mechanical loading.

d: Circuit Overloading: Consider the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Pay attention to equipment nameplate ratings when addressing this concern.

e: Reliable Earthing: Maintain reliable earthing (grounding) of rack-mounted equipment. Pay special attention to supply connections other than direct connections to the branch circuit (such as use of power strips).

13 XOTN Chassis Unit

This chapter provides details about the XOTN chassis—its specifications and features.

The XOTN chassis unit is a part of the XOTN system. This system allows you to use IxNetwork protocols and scalable data plane test capabilities to test Optical Transport Network (OTN) devices. It provides flexible mapping of Ethernet frames to different OTN rates and structures according to ITU-T G.709.

Each system comprises an XOTN chassis unit, a USB cable, power cord, CFPs, and software. The XOTN ports are configured and managed by the IxNetwork application and can be used with any XM K2 load module (40Gb/s or 100Gb/s).

To test OTN devices, you must connect the XOTN chassis unit to a load module on the Client side, a DUT on the OTN side, and an XM chassis to centrally manage the XOTN chassis units using IxNetwork. Refer to *XOTN Installation Guide* for installation information and the online help for configuration information.

An XOTN system allows you to convert a 40Gb/s or 100Gb/s Ethernet signal to an Optical Channel Transport Unit (OTU3 or OTU4) signal and vice versa. On the Transmit side, XOTN can generate a PRBS pattern or transmit an Ethernet client signal from IxNetwork. The XOTN chassis unit converts the Ethernet traffic into an OTU3 (43.01Gb/s) or OTU4 (112Gb/s) signal; then transmits it to your OTN DUT. On the Receive side, XOTN receives OTU3 or OTU4 signals from your OTN DUT, converts the signal to 40Gb/s or 100Gb/s Ethernet, then transmits the received traffic to IxNetwork for further analysis. This means you can perform all IxNetwork Ethernet tests on your OTN enabled DUT. You also get detailed OTN statistics on the traffic passing through the XOTN unit.

About OTN Technology

The Optical Transport Network (OTN) emerged in the late 1990's as a "digital wrapper" around client signals before they are transported over a WDM (Wavelength-division multiplexing) network. Since then, the amount of traffic, particularly data and video, has increased significantly, placing higher demands

on the edge and core networks. This has been a major driver for the IP-optical integration. There is now an increasing need for a technology to replace the performance monitoring and fault-handling characteristics of SONET/SDH.

The OTN with G.709 framing has emerged as a way to add management capabilities directly to wavelengths. Using this technology, a client signal can be mapped directly into an optical network rather than requiring costly protocols, such as SONET/SDH, to provide the administrative functions.

The XOTN chassis unit is shown in the following figure:

Figure 13-1. XOTN Chassis

The Part Number of XOTN chassis is 941-0030.

Specifications

XOTN Chassis Unit

The XOTN chassis unit specifications are contained in *Table 13-1*.

Table 13-1. XOTN Specifications

	**Caution–Battery replacement** There is danger of explosion if battery is incorrectly replaced. Do not attempt to replace the battery. Return to Ixia Customer Service for replacement with the same or equivalent type of battery. Ixia disposes of used batteries according to the battery manufacturer's instructions.
Physical	
Size	• Width: 441.8 mm (17.394”) • Height: 88.1 mm (3.469”) • Depth: 500 mm (19.685”)
Weight	11.5 kg (25.3 lb)
Environmental	
Operating Temperature	5°C to 35°C (41°F to 95°F)
Location	Indoor use only
Power	Maximum: 5A@115Vac 3A@230Vac
AC Voltage	90 ~ 264Vac, Full Range Input Mains supply voltage fluctuations not to exceed +/- 10% of specified nominal voltage. Transient overvoltages are specified by Installation category II.
Frequency	47 ~ 63Hz

14 Ixia GPS Auxiliary Function Device (AFD1)

This chapter provides details about Ixia GPS Auxiliary Function Device—its specifications and features.

The IXIA Auxiliary Function Device 1 (AFD1) provides the means for accurate worldwide timing using GPS technology. The IXIA AFD1 is shown in *Figure 14-1*.

Figure 14-1. Ixia AFD1

The IXIA AFD1 with integrated Global Positioning System (GPS) is designed for distributed end-to-end measurements of key metrics, including point-to-point latency and jitter.

The Ixia AFD1 GPS receiver is controlled by an Ixia chassis through a USB port. Chassis timing is provided by connecting the Sync Out of the AFD1 to the Sync In of the chassis. This configuration then enables the chassis to operate as a subordinate in a virtual chassis chain, with the Ixia AFD1 as the master.

Figure 14-2 on page 14-2 shows the AFD1 in operation with other chassis in a local chassis chain. Multiple local chassis chains can be collected through GPS into a virtual chassis chain.

Figure 14-2. AFD1 in a Chassis Chain

The IxExplorer GUI displays the status of the GPS interface to you. Figure 14-3 shows the Chassis Properties dialog with status information. The connection is determined to be either *locked* or *unlocked*. In the Locked state, the chassis is locked to GPS time (GMT) within 150nS. In the unlocked state, the AFD1 GPS hardware operates to acquire the minimum number of satellites required to achieve accurate GPS timing.

Caution: A chassis connected to an AFD1 chassis does not operate properly if set to Synchronous time source, unless the sync cable is disconnected.

The process of generating the Lock status for the AFD1 consists of getting GPS time lock and then synchronizing the internal clock to the GPS clock. The AFD1 does not enter the 'Lock' state until both of these conditions are met. In the unlocked state, the chassis in the unlocked chain are not accurately time synchronized to the rest of the chain.

In operation, once a chassis chain is constructed and the chassis are synchronized, you can clear the timestamps to provide a baseline time for all chassis in the chain. The chain operations are then locked until such time that the GPS lock is lost by a member of the chain. Data sent from one port in the chain to another provides one-way latency measurements by subtraction of the transmit time stamp from the receive time stamp.

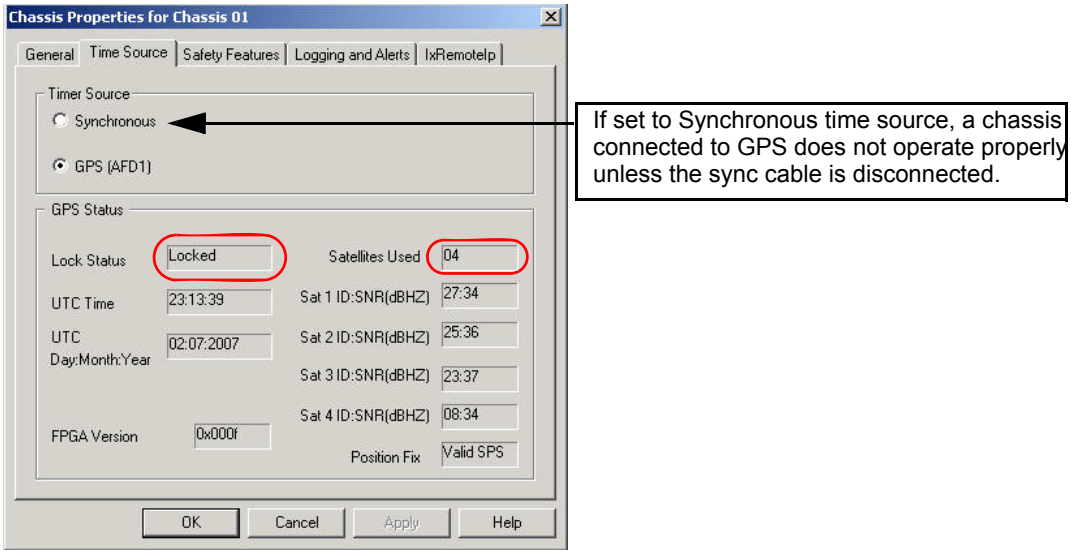
For large or very remote chassis chains, the chassis chain properties provide an offset delay. This delay is defaulted to five seconds. For chassis chains where the communication delays are significant, as in worldwide or large chains, a longer delay should be selected to allow for setup communication delays. The delay is the time of a particular chassis operation (for example, start transmit, stop transmit) plus the configured delay for any synchronous operation. When an operation for the entire chain is executed, this delay is added to the operation. A dialog opens indicating that the operation is in process when the delays are significant.

The chassis time is taken from any chassis with a GPS interface attached. The setup for the chassis chain requires that all chassis in the chain be locked. This is indicated in the IxExplorer GUI. The IxExplorer GUI also provides antenna information such as satellite strength, to enable installation of the antenna in a location with a good 'view' of the satellites.

The critical operation for a virtual chain is the reset of the System Time Stamps. All other actions are dependent on the synchronous execution of this operation.

To reset time stamps for a GPS-connected system, the reset operation needs to be executed for the chassis chain, and not for the individual chassis.

Figure 14-3. Chassis Properties AFD1-Time Source



AFD1 Setup

The AFD1 Kit:

The AFD1 kit comes with cables and items required to install and connect the AFD1 in a lab. The AFD1 kit does not include the cable and antenna for permanent installation at a particular site. The antenna and cable kits need to be ordered separately after a site survey determines the site requirements.

The kit contains the following items:

- AFD1 chassis
- AFD1 chassis rack mount ears
- 3-foot sync cable
- 6-foot USB cable
- Window antenna

The AFD1 installation uses the USB cable for communication and power. The Ixia chassis automatically detects the connections.

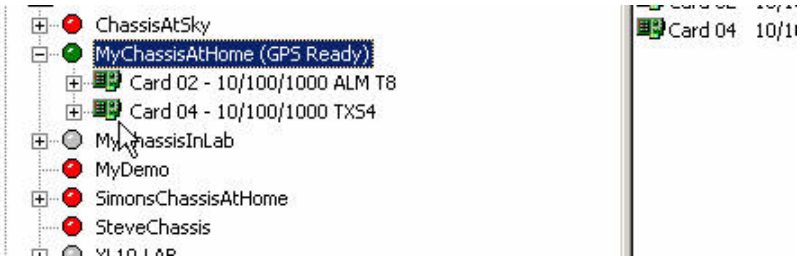
The window antenna is included in the kit for demo use only and does not reliably provide a stable lock environment. For permanent installations, order either the 75-foot or 200-foot cable and antenna kits.

Successful GPS Synchronization in IxExplorer

In the Chassis Properties dialog of IxExplorer, after selection of GPS as the timer source, the satellites used are displayed. In Figure 14-3 on page 14-3, satellite 04 is being used and the status is ‘locked’. In the chassis tree view of IxExplorer

(Figure 14-4), the chassis status is shown as 'GPS Ready' if it has successfully locked onto satellite signal. The highlighted chassis is GPS enabled and ready.

Figure 14-4. Chassis Tree View in IxExplorer

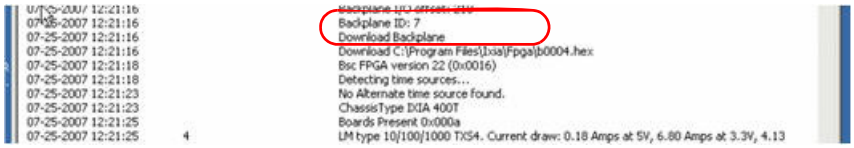


Enabling/Installing GPS Based Synchronization

This procedure to set the time source needs to be followed only for the initial installation of the AFD1 GPS unit. Thereafter, upon subsequent restarts, the chassis and AFD1 unit starts fully operational.

1. Start the chassis without attaching the AFD1 GPS unit. Note the message regarding timing source, as shown in the following figure.

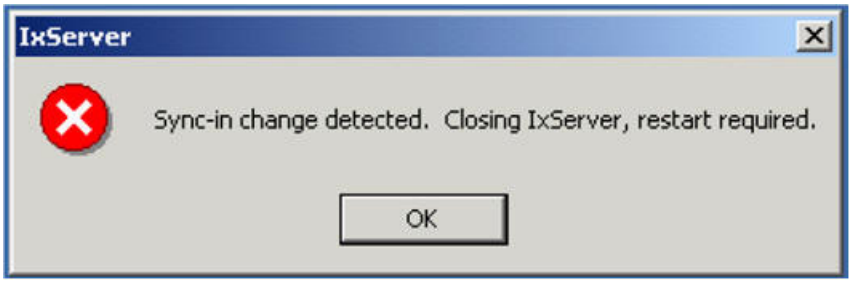
Figure 14-5. IxServer Start Log Before Attaching AFD1



2. Attach the AFD1 GPS unit by plugging in the USB and the Sync cables.

   When the chassis detects the GPS (AFD1) unit, it prompts to restart the IxServer, as shown in the following figure.

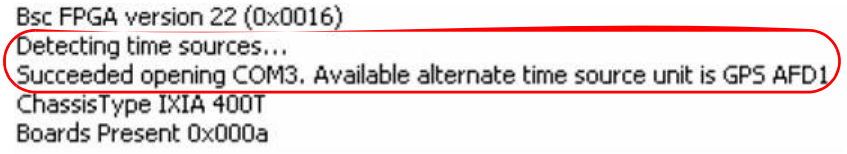
Figure 14-6. Sync-In Detection Prompt



3. Click **OK** to restart IxServer.

   IxServer restarts, then detects GPS as the timing source and configures the chassis as a subordinate, since the chassis is receiving its timing through sync cable from the ADF1 GPS source. The expected log messages are shown in Figure 14-7 and Figure 14-8.

Figure 14-7. IxServer Log - GPS AFD1 Detected



GPS AFD1 is detected and COM3 port is indicated as the communication channel between chassis and AFD1.

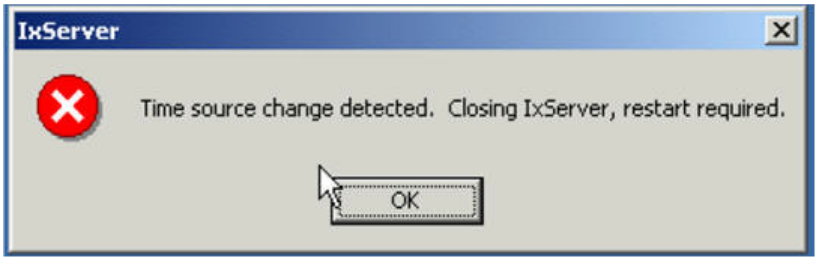
Figure 14-8. IxServer Log - Chassis Configured as Slave to AFD1

The chassis is configured as a subordinate to AFD1.

4. Open IxExplorer. In the **Chassis Properties** dialog box select GPS (AFD1) timer source, as shown in Figure 14-3 on page 14-3.

   Upon selection of GPS option, IxServer must be closed and restarted for the changes to take effect, as the prompt in Figure 14-9 shows.

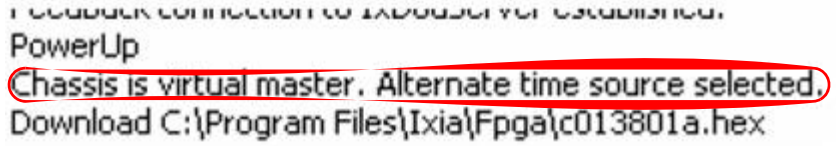
Figure 14-9. Time Source Change Detection Prompt



5. Click OK to restart IxServer.

   Once IxServer is restarted, the IxServer Log shows the AFD1 GPS unit is detected as the time source and the chassis is designated as 'Virtual Master' rather than subordinate (Figure 14-10).

Figure 14-10. IxServer Log - Chassis is Virtual Master



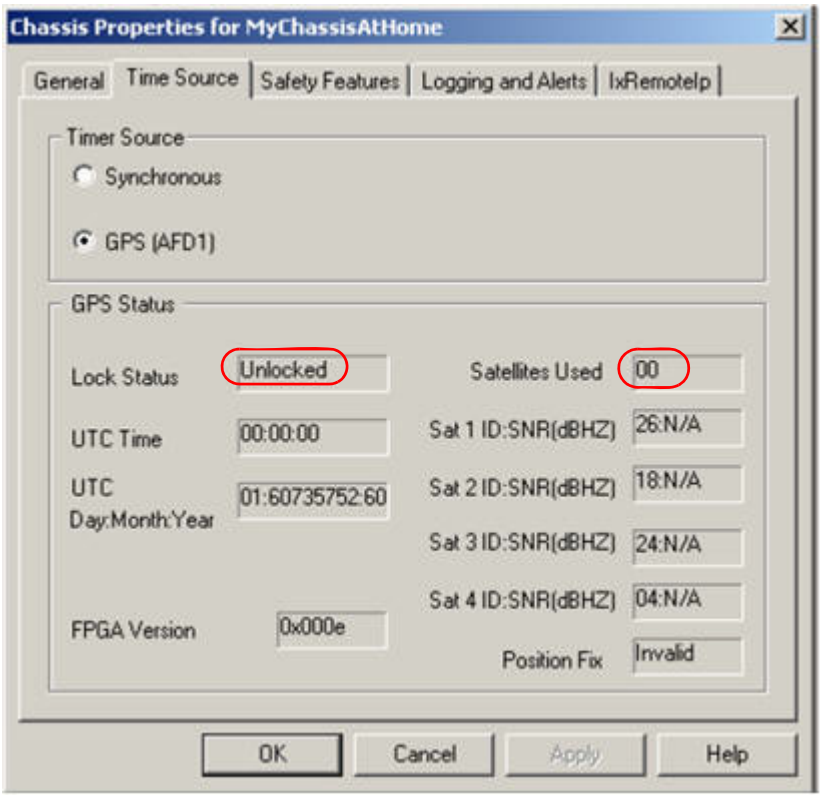
6. Check IxExplorer for GPS status, as shown in Figure 14-3 on page 14-3. Satellite details changes periodically showing satellite number and signal strength. A good signal strength has SNR reading of more than 35.

Now the chassis is ready for operation based on GPS time source.

Troubleshooting—GPS Unit 'Not Ready'

If, after completing installation by following the steps above, there is no GPS information and the status is 'Unlocked' in the Time Sources tab of Chassis Properties in IxExplorer (Figure 14-11 on page 14-6), then follow the steps mentioned here to ensure that the ADF1 unit comes up fully functional.

Figure 14-11. Chassis Properties AFD1 - Unsuccessful GPS Status



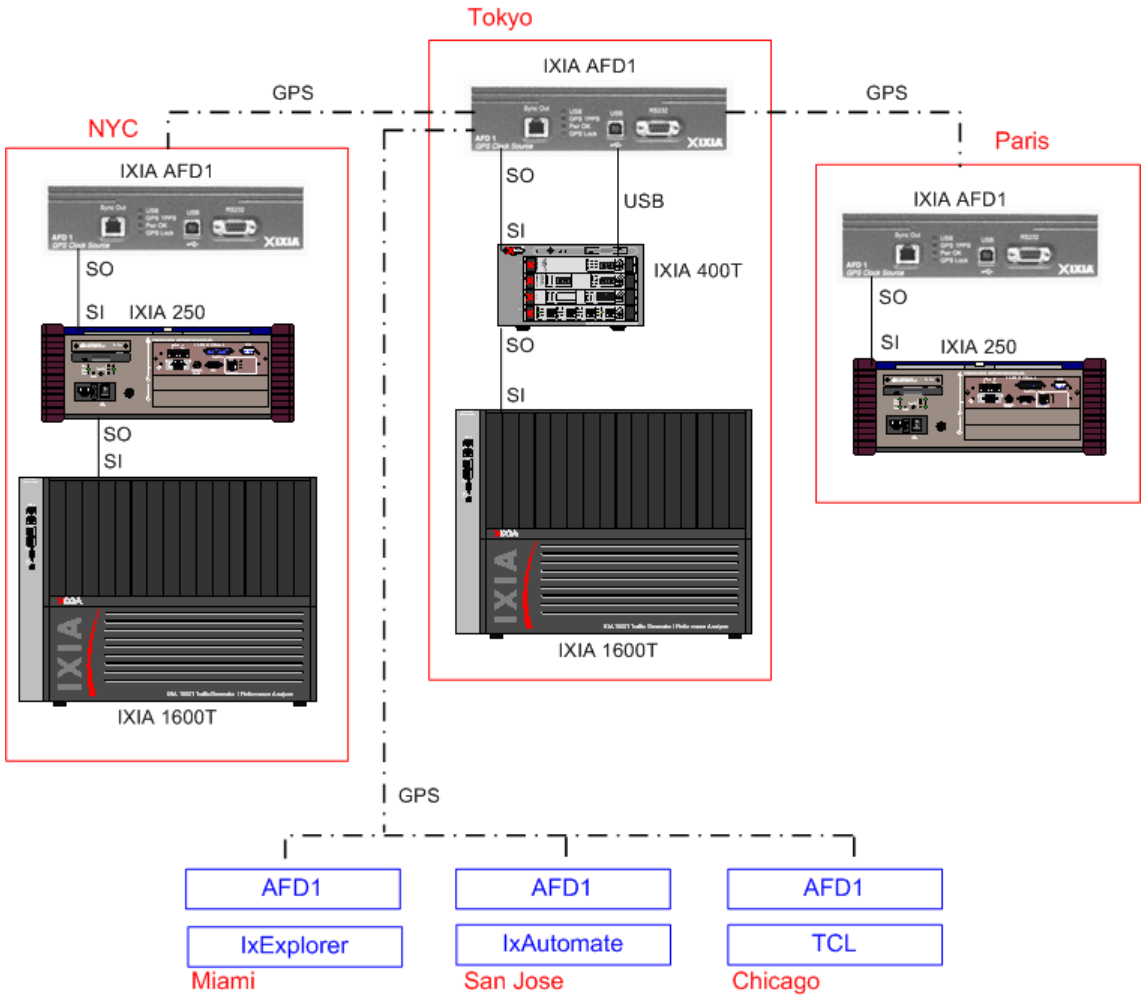
1. Ensure that the GPS Antenna has good positioning. Position the antenna outdoors with a clear view of the sky. Refer to Appendix C, *GPS Antenna Installation Requirements*.
2. Ensure that the antenna cabling is correctly fitted. Reseat the coaxial cable into the AFD1 unit.

   Allow five to 10 minutes to see GPS reception become established. A full lock requires three stable satellites.

Worldwide Synchronization

Two or more Ixia chassis connected to a time reference may be distributed worldwide forming a virtual chassis chain based on GPS and/or CDMA timing. One possible configuration is shown in *Figure 14-12* on page 14-7.

Figure 14-12. Worldwide Deployment of Synchronized Chassis



The ports on all of the chassis may be shared by one or more Ixia software users located likewise anywhere in the world. Where GPS and CDMA sources are used, all of the sources must have good quality time values in order for the trigger to be transmitted.

Once the timing features of the chassis is configured, operating a worldwide set of Ixia chassis is the same as local operation. The Ixia hardware and software program the clocks such that they all send a master trigger pulse to all Ixia chassis, within a tolerance of ±150 ns with GPS and ±100 us for CDMA.

Ixia chassis timing operates by resetting at a fixed time-of-day on all chassis from one source, and then maintaining the time accuracy through various different means. *Table 14-1* on page 14-8 describes the full set of options available and their approximate relative accuracies.

Table 14-1. Summary of Timing Options

Available on Devices	Timing Option	Time of Day Accuracy	Frequency Source	Frequency Accuracy
All Chassis	GPS	150 nanoseconds from GMT	Ixia AFD1	Stratum 1
Ixia 100, 400T, 1600T	Synchronous	N/A	Internal PC clock	1 microsecond/second
Ixia 250	CDMA	100 microseconds from GMT	CDMA	Stratum 2
Ixia 100	CDMA	100 microseconds from GMT	CDMA	Stratum 2
Ixia 100	GPS (with attached antenna)	150 nanoseconds from GMT	GPS	Stratum 1

Calculating Latency Accuracy for AFD1 (GPS)

Use the following calculation for latency accuracy for AFD1 (GPS) setups.

Latency A to B = Lab

Latency B to A = Lba

Transmit path A to B = T1

Transmit path B to A = T2

Time at A = Ta

Time at B = Tb

Time Absolute = T

Time Error at any site = Terr

Lab=Ta+T1-Tb

Lba=Tb+T2-Ta

Delta L = Lab – Lba

Delta L = Ta+T1-Tb – (Tb+T2-Ta)

Delta L = T1-T2+2(Ta-Tb)

Delta L = 2(Ta – Tb)

If Ta = T+/-Terr and Tb = T+/-Terr

Then

Delta L= 2(T+/-Terr – T+/-Terr)

Delta L= 2(|Terr|+|Terr|)

Delta L = 4Terr

Front Panel LEDs

The AFD1 has the following front panel LEDs:

Table 14-2. AFD1 LEDs

Label	Color	Description
USB	Green	Indicates that the docnnection is enabled, and blinks with USB activity.
GPS 1PPS	Green	Indicates that the '1 Pulse Per Second' heartbeat is being generated by the GPS hardware. The GPS hardware has acquired at least one satellite and is receiving time information.
Pwr OK	Green	The AFD1 power has been validated.
GPS Lock	Green	Indicates that the GPS hardware has acquired a fix and that the 1PPS timing is valid. It also Indicates that the internal PLL has locked to the 1PPS signal. Testing is invalidated if the GPS Lock signal is not illuminated.

IXIA AFD1 Specifications

The IXIA AFD1 specifications are contained in *Table 14-3* on page 14-9.

Table 14-3. Ixia AFD1 Specifications

General	
Physical	
Size	9.6"x7"x2.9" (with feet, 2.70" without feet)
Weight	3.15 lb
Avg. Shipping Wt.	6 lbs
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 122°F, (5°C to 50°C)
Storage	41°F to 122°F, (5°C to 50°C)
Power	Worst case power = 2.5W
	5V regulated source
Humidity	

Table 14-3. Ixia AFD1 Specifications

Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing
GPS Functionality	
Clock	12.5Mhz System clock
Pulse Width	80 ns
Rear Panel Switches	Reset switch
Front Panel Indicators	USB, GPS PPS, Pwr OK, GPS Lock
Front Panel Connectors	
USB Port	Type B
Sync Out	RJ14
Back Panel Connectors	
Antenna	SMA
Power	(not used) 2.0mm Power jack

15 Ixia IRIG-B Auxiliary Function Device (AFD2)

The IXIA Auxiliary Function Device 2 (AFD2) provides the means for accurate worldwide timing using Inter-Range Instrumentation Group (IRIG-B) technology. The ADF2 decodes the GPS **satellite**s and time information and sends out a pulse to the Optixia chassis. The IXIA /AFD2 is shown in *Figure 15-1*.

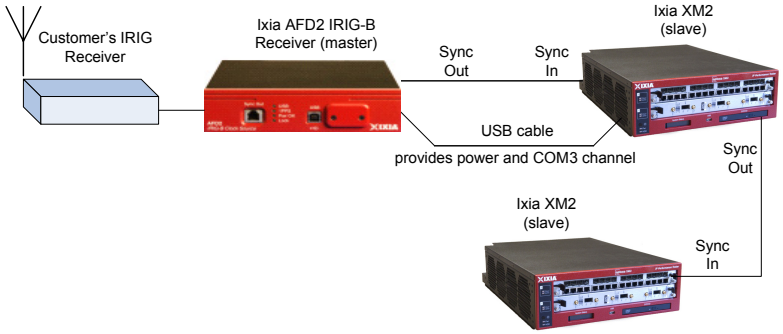
Figure 15-1. Ixia AFD2

The IXIA AFD2 with integrated IRIG-B is designed to provide 12.5 MHz GPS clock with a programmable 80 ns sync pulse to the Optixia chassis.

The Ixia AFD2 IRIG-B receiver is controlled by an Ixia chassis through a USB port. Chassis timing is provided by connecting the Sync Out of the AFD2 to the Sync In of the chassis. This configuration then enables the chassis to operate as a subordinate in a virtual chassis chain, with the Ixia AFD2 as the master.

Figure 15-2 on page 15-2 shows the AFD2 in operation with other chassis in a local chassis chain. Multiple local chassis chains can be collected through IRIG-B into a virtual chassis chain.

Figure 15-2. AFD2 in a Chassis Chain



The IxExplorer GUI displays the status of the IRIG-B interface to the user. Figure 15-3 shows the Chassis Properties dialog with status information. The connection is determined to be either *locked* or *unlocked*. In the Locked state, the chassis is locked to IRIG-B time within 150nS. In the unlocked state, the AFD2 IRIG-B hardware operates to lock its VCXO to 1PPS pulse.

Caution: A chassis connected to an AFD2 chassis does not operate properly if set to Synchronous time source, unless the sync cable is disconnected.

The process of generating the Lock status for the AFD2 consists of getting IRIG-B time lock and then synchronizing the internal clock to the IRIG-B 1PPS pulse. The AFD2 does not enter the 'Lock' state until the VCXO lock condition is met. In the unlocked state, the chassis in the unlocked chain are not accurately time-synchronized to the rest of the chain.

In operation, once a chassis chain is constructed and the chassis are synchronized, you can clear the timestamps to provide a baseline time for all chassis in the chain. The chain operations are then locked until such time that the IRIG-B lock is lost by a member of the chain. Data sent from one port in the chain to another provides one-way latency measurements by subtraction of the transmit time stamp from the receive time stamp.

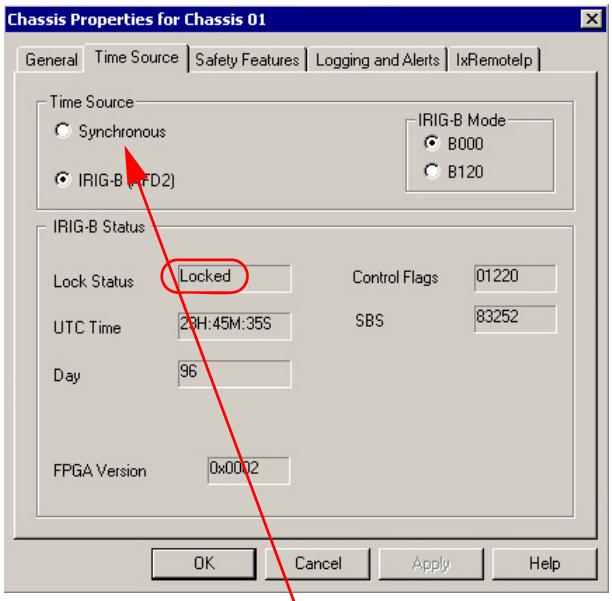
For large or very remote chassis chains, the chassis chain properties provide an offset delay. This delay is defaulted to 5 seconds. For chassis chains where the communication delays are significant, as in worldwide or large chains, a longer delay should be selected to allow for setup communication delays. The delay is the time of a particular chassis operation (for example, start transmit, stop transmit) plus the configured delay for any synchronous operation. When an operation for the entire chain is executed, this delay is added to the operation. A dialog opens indicating that the operation is in process when the delays are significant.

The chassis time is taken from any chassis with a IRIG-B interface attached. The setup for the chassis chain requires that all chassis in the chain be locked. This is indicated in the IxExplorer GUI.

The critical operation for a virtual chain is the reset of the System Time Stamps. All other actions are dependent on the synchronous execution of this operation.

To reset time stamps for a IRIG-B-connected system, the reset operation needs to be executed for the chassis chain, and not for the individual chassis.

Figure 15-3. Chassis Properties AFD2 - Time Source



If set to Synchronous time source, a chassis connected to IRIG-B does not operate properly unless the sync cable is disconnected.

.

Table 15-1. Chassis Properties, Time Source Tab

Section	Field/Control	Description
Time Source	Synchronous	
	IRIG-B (AFD2)	
IRIG-B Mode	B000	B000 is straight TTL serial output (from the IRIG-B receiver)
	B120	B120 is amplitude modulation (AM) (from the IRIG-B receiver)
IRIG-B Status	Lock Status	Locked = locked to IRIG-B 1PPS input (from IRIG-B receiver)
	UTC Time	UTC Time (display only) in HH:MM:SS comes from the IRIG-B receiver
	Day	Increments from 1 to 366
	Control Flags	These are vendor-specific flags that are passed-through from the IRIG-B receiver

Table 15-1. Chassis Properties, Time Source Tab

Section	Field/Control	Description
	SBS	Straight Binary Seconds from 1 to xxx each day, starting at midnight. Resets to 0 each midnight.
	FPGA Version	FPGA version

AFD2 Setup

The AFD2 Kit:

The AFD2 kit comes with cables and items required to install and connect the AFD2 in a lab. The AFD2 kit does not include the IRIG receiver and antenna for permanent installation at a particular site.

The kit contains these items:

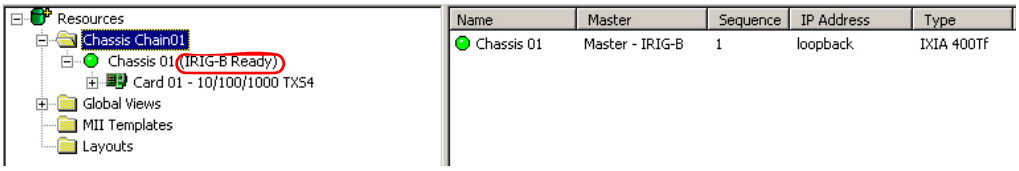
- AFD2 chassis
- AFD2 chassis rack mount ears
- 3-foot sync cable
- 6-foot USB cable

The AFD2 installation uses the USB cable for communication and power. The Ixia chassis automatically detects the connections.

Successful IRIG-B Synchronization in IxExplorer

In the Chassis Properties dialog of IxExplorer, after selection of IRIG-B as the timer source, the IRIG-B status is displayed. In Figure 15-3 on page 15-3, the status is ‘locked’ to the 1PPS signal coming from the IRIG-B receiver. In the chassis tree view of IxExplorer (Figure 15-4), the chassis status is shown as ‘IRIG-B Ready’ if it has successfully locked onto the 1PPS signal.

Figure 15-4. Chassis Tree View in IxExplorer



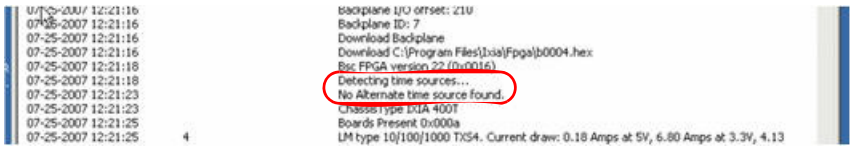
Enabling/Installing IRIG-B Based Synchronization

This procedure to set the time source needs to be followed only for the initial installation of the AFD2 IRIG-B unit. Thereafter, upon subsequent restarts, the chassis and AFD2 unit starts up fully operational.

1. Set up the antenna and IRIG-B receiver (not supplied by Ixia).

2. Connect the 1PPS and IRIG-B outputs from the IRIG-B receiver to the AFD2.
3. Connect the sync and USB cables between AFD2 and the Ixia chassis. On the front panel of the AFD2,
   - the Pwr OK indicator lights solid,
   - the 1PPS indicator blinks to indicate the signal from the IRIG-B receiveris good, and
   - the Lock indicator lights solid.
4. Start the chassis. After starting completely, the IxExplorer resource tree is displayed as shown in Figure 15-4 on page 15-4.
5. Note the message regarding timing source, as shown in Figure 15-5.

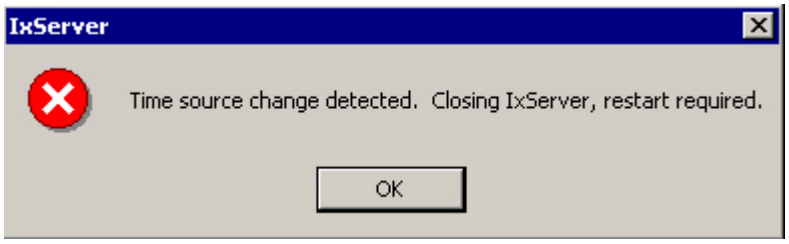
Figure 15-5. IxServer Start Log Before Attaching AFD2



Changing Time Source

Any time the clock source is switched, IxServer must be restarted. When the chassis is switched from Synchronous time source to IRIG-B, or vice-versa, the following message is displayed as shown in Figure 15-6.

Figure 15-6. Time Source Change Detection Prompt

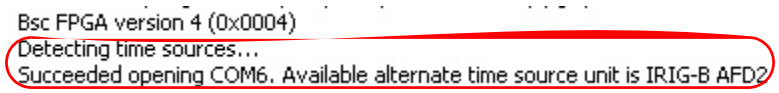


You are prompted to restart the IxServer. In this example, the time source was changed from synchronous to IRIG-B.

1. Click **OK** and then manually restart IxServer.

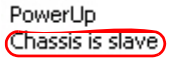
   IxServer restarts, then detects IRIG-B as the timing source and configure the chassis as a subordinate, since the chassis is receiving its timing through sync cable from the AFD2 IRIG-B source. The expected IxServer log messages are shown in Figure 15-7 and Figure 15-8.

Figure 15-7. IxServer Log - IRIG-B AFD2 Detected



IRIG-B AFD2 is detected and COM6 port is indicated as the communication channel between chassis and AFD2.

Figure 15-8. IxServer Log - Chassis Configured as Slave to AFD2



The chassis is configured as a subordinate to AFD2.

Troubleshooting— IRIG-B Unit 'Not Ready'

If, after completing installation by following the steps above, there is no IRIG-B information and the status is 'Unlocked' in the Time Sources tab of Chassis Properties in IxExplorer (Figure 15-3 on page 15-3), then one of the following conditions needs to be corrected.

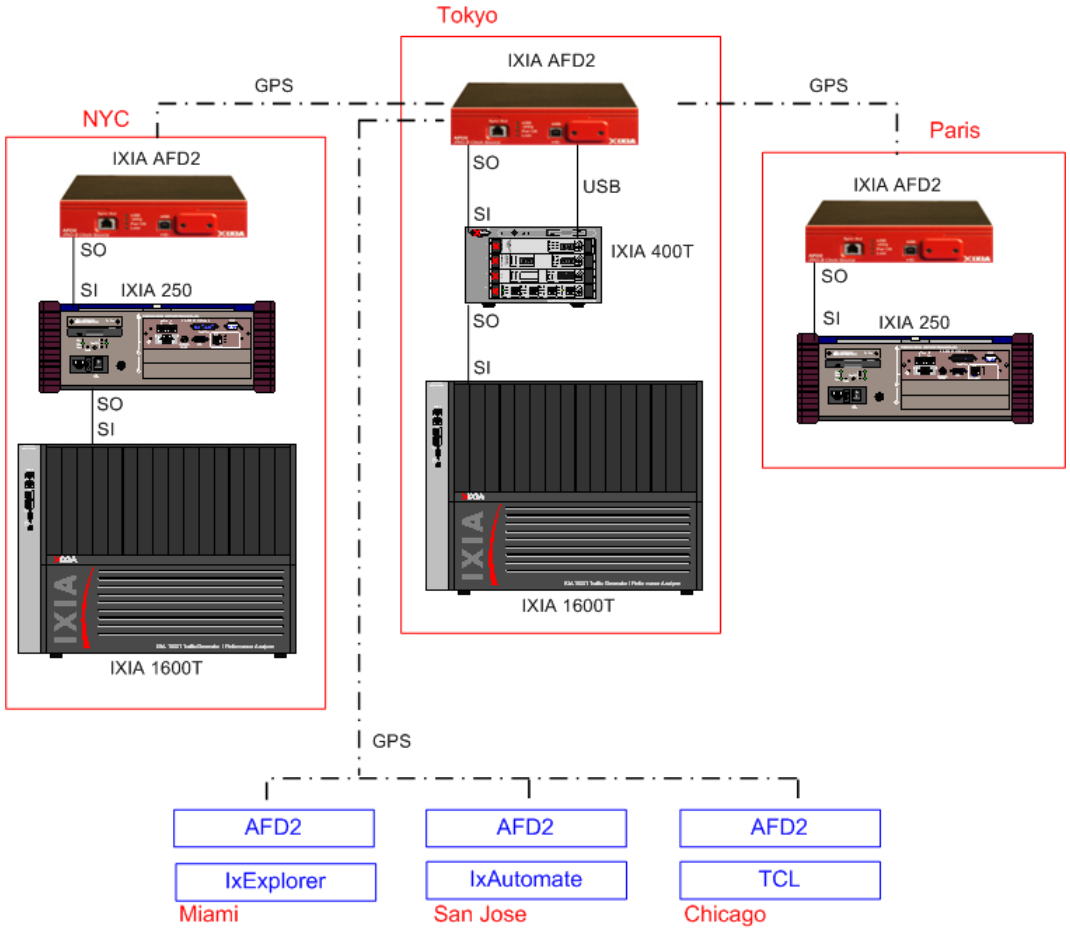
1PPS signal is not connected: check cabling between AFD2 and the IRIG-B receiver.

IRIG-B Mode B000 has been selected, but the IRIG-B receiver is sending B120 signal (or vice versa): change the selection in the Time Sources tab of Chassis Properties in IxExplorer (Figure 15-3 on page 15-3), and see if the status is corrected ('Locked') after a short interval.

Worldwide Synchronization

Two or more Ixia chassis connected to a time reference may be distributed worldwide forming a virtual chassis chain based on IRIG-B and/or CDMA timing. One possible configuration is shown in *Figure 15-9* on page 15-7.

Figure 15-9. Worldwide Deployment of Synchronized Chassis



The ports on all of the chassis may be shared by one or more Ixia software users located likewise anywhere in the world. Where IRIG-B and CDMA sources are used, all of the sources must have good quality time values in order for the trigger to be transmitted.

Once the timing features of the chassis is configured, operating a worldwide set of Ixia chassis is the same as local operation. The Ixia hardware and software program the clocks such that they all send a master trigger pulse to all Ixia chassis, within a tolerance of ±150 ns with IRIG-B and ±100 us for CDMA.

Ixia chassis timing operates by resetting at a fixed time-of-day on all chassis from one source, and then maintaining the time accuracy through various

different means. *Table 15-2* on page 15-8 describes the full set of options available and their approximate relative accuracies.

Table 15-2. Summary of Timing Options

Available on Devices	Timing Option	Time of Day Accuracy	Frequency Source	Frequency Accuracy
All Chassis	IRIG-B/GPS	150 nanoseconds from GMT	Ixia AFD2	Stratum 1
Ixia 100, 400T, 1600T	Synchronous	N/A	Internal PC clock	1 microsecond/second
Ixia 250	CDMA	100 microseconds from GMT	CDMA	Stratum 2
Ixia 100	CDMA in-built	100 microseconds from GMT	CDMA	Stratum 2
Ixia 100	GPS in-built	150 nanoseconds from GMT	GPS	Stratum 1

Calculating Latency Accuracy for AFD2 (IRIG-B)

Use the following calculation for latency accuracy for AFD2 (IRIG-B) setups.

Latency A to B = Lab

Latency B to A = Lba

Transmit path A to B = T1

Transmit path B to A = T2

Time at A = Ta

Time at B = Tb

Time Absolute = T

Time Error at any site = Terr

Lab=Ta+T1-Tb

Lba=Tb+T2-Ta

Delta L = Lab – Lba

Delta L = Ta+T1-Tb – (Tb+T2-Ta)

Delta L = T1-T2+2(Ta-Tb)

Delta L = 2(Ta – Tb)

If Ta = T+/-Terr and Tb = T+/-Terr

Then

Delta L= 2(T+/-Terr – T+/-Terr)

Delta L= 2(|Terr|+|Terr|)

Delta L = 4Terr

Front Panel LEDs

The AFD2 has the following front panel LEDs:

Table 15-3. AFD2 LEDs

Label	Color	Description
USB	Green	Indicates that the connection is enabled, and glows solid with USB activity.
1PPS	Green	Indicates that the '1 Pulse Per Second' heartbeat is being generated by the IRIG-B hardware.
Pwr OK	Green	The AFD2 power has been validated.
Lock	Green	Indicates that the internal PLL has locked to the 1PPS signal. Testing is invalidated if the IRIG-B Lock signal is not illuminated.

IXIA AFD2 Specifications

The IXIA AFD2 specifications are contained in *Table 15-4* on page 15-9.

Table 15-4. Ixia AFD2 Specifications

General	
Physical	
Size	9.6"x7"x2.9" (with feet, 2.70" without feet)
Weight	3.15 lb
Avg. Shipping Wt.	6 lbs
Shipping Vibration	FED-STD-101C, Method 5019.1/5020.1
Environmental	
Temperature	
Operating	41°F to 122°F, (5°C to 50°C)
Storage	41°F to 122°F, (5°C to 50°C)
Power	Worst case power = 2.5W
	5V regulated source
Humidity	
Operating	0% to 85%, non-condensing
Storage	0% to 85%, non-condensing

Table 15-4. Ixia AFD2 Specifications

IRIG-B Functionality	Bit rate is 100 pps and frame rate is 1fps for both code formats. 1pps pulse provides the precise time refrence.
IRIGB000	DC level shift, pulse width coded with BCD, CF(control functions), SBS
IRIGB120	1kHz carrier sine wave amplitude modulated with BCD, CF (control functions), SBS
Clock	12.5 Mhz GPS System clock
Pulse Width	80 ns
Rear Panel Switches	Reset switch
Front Panel Indicators	USB, 1PPS, Pwr OK, Lock
Front Panel Connectors	
USB Port	Type B
Sync Out	RJ14
Back Panel Connectors	
IRIG-in	BNC, IRIG-B code in
1PPS-in	BNC, 1PPS pulse in
Power	(not used) 2.0mm Power jack

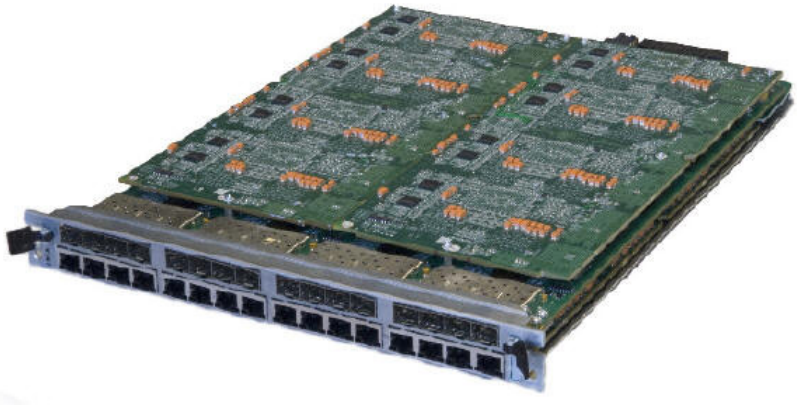
16 IXIA 10/100/1000 Load Modules

This chapter provides details about Ixia 10/100/1000 family of load modules—the specifications and features.

The 10/100/1000 family of load modules implements Ethernet interfaces that run at 10 Mbps, 100 Mbps, or Gigabit (1000 Mbps) speeds. Different numbers of ports and interfaces are available for the different board types. The specifications for these load modules are listed in *Table 16-2* on page 16-7. A representative selection of these load modules are pictured on the pages that follow.

A member of the 10/100/1000 family used on the Optixia XM12 and XM2 chassis, the LSM1000XMV16-01, is shown in *Figure 16-1* on page 16-1.

Figure 16-1. LSM1000XMV16-01 Load Module



Another member of the 10/100/1000 family used on the Optixia XM12 and XM2 chassis, the LSM1000XMS12-01, is shown in *Figure 16-2* on page 16-2.

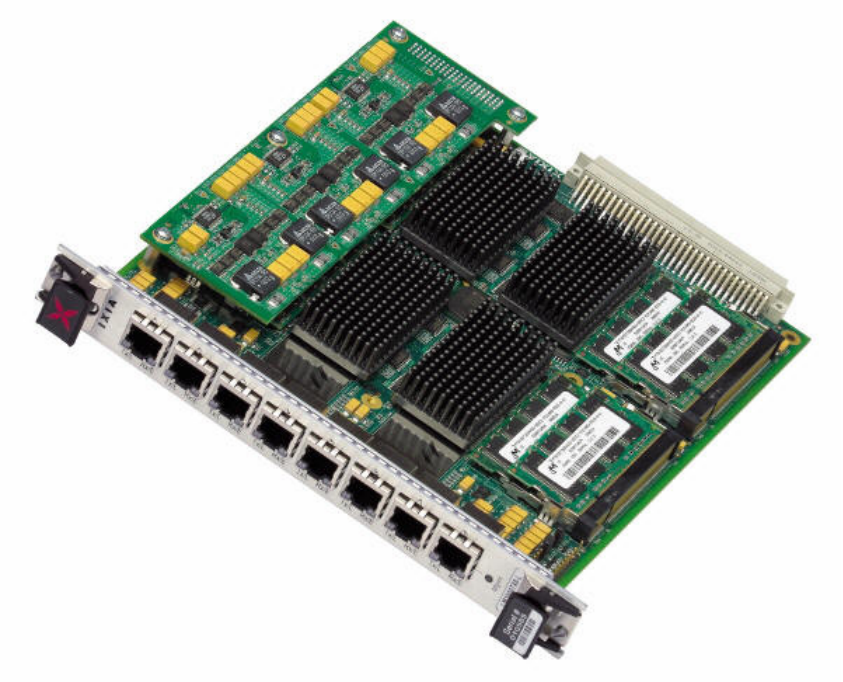
Figure 16-2. LSM1000XMS12-01 Load Module

Another of the modules in the 10/100/1000 family, the LM1000STXS4, is shown in *Figure 16-3*.

Figure 16-3. LM1000STXS4 Load Module

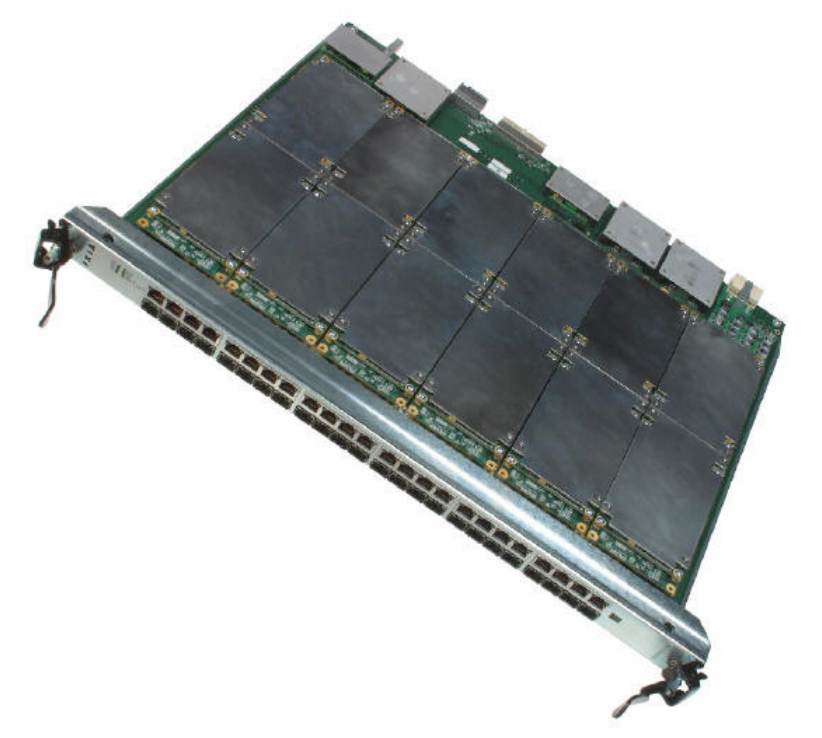
The application load module ALM1000T8 is an 8-port 10/100/1000 Mbps Base T Ethernet copper module which supports the Real World Traffic Suite (includes IxVPN, IxChariot, and IxLoad). This module also supports ARP, PING, and independent Linux SDK applications. The ALM1000T8 load module is shown in Figure 16-4.

Figure 16-4. ALM1000T8 Application Load Module



A member of the 10/100/1000 family used on the Optixia XL10 chassis, the OLM1000STX24, is shown in *Figure 16-5* on page 16-3.

Figure 16-5. OLM1000STX24 Load Module



Part Numbers

The part numbers are shown in *Table 16-1*. Items without a *Price List Names* entry are no longer available.

Table 16-1. Part Numbers for 10/100/1000 Modules

Load Module	Price List Names	Description
LSM1000XMV16-01	LSM1000XMV16-01	16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, 800MHz PowerPC Processor. 1 GB of processor memory per port. Does not include SFP transceivers. **Note**: In order to meet the emissions requirements of FCC part 15 Class A the RJ45 cables attached to this module's Ethernet ports must have ferrite beads (Fair-Rite 0431164281 or equivalent) present at both ends of the cable.
LSM1000XMVR16-01	LSM1000XMVR16-01	16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance, 400MHz PowerPC Processor. 256MB of processor memory per port. **Note**: In order to meet the emissions requirements of FCC part 15 Class A the RJ45 cables attached to this module's Ethernet ports must have ferrite beads (Fair-Rite 0431164281 or equivalent) present at both ends of the cable.
LSM1000XMV12-01	LSM1000XMV12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, 800MHz PowerPC Processor. 1 GB of processor memory per port. Does not include SFP transceivers.
LSM1000XMVR12-01	LSM1000XMVR12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance, 400MHz PowerPC Processor. 256MB of processor memory per port.
LSM1000XMV8-01	LSM1000XMV8-01	8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, 800MHz PowerPC Processor. 1 GB of processor memory per port. Does not include SFP transceivers.
LSM1000XMVR8-01	LSM1000XMVR8-01	8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance, 400MHz PowerPC Processor. 256MB of processor memory per port.
LSM1000XMV4-01	LSM1000XMV4-01	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, 800MHz PowerPC Processor. 1 GB of processor memory per port. Does not include SFP transceivers.
LSM1000XMVR4-01	LSM1000XMVR4-01	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance, 400MHz PowerPC Processor. 256MB of processor memory per port.

Table 16-1. Part Numbers for 10/100/1000 Modules

Load Module	Price List Names	Description
LSM1000XMS12-01	LSM1000XMS12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module. 256MB of processor memory per port. Does not include SFP transceivers. **Note**: In order to meet the emissions requirements of FCC part 15 Class A the RJ45 cables attached to this module's Ethernet ports must have ferrite beads (Fair-Rite 0431164281 or equivalent) present at both ends of the cable.
LSM1000XMSR12-01	LSM1000XMSR12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module, reduced performance. 256MB of processor memory per port. **Note**: In order to meet the emissions requirements of FCC part 15 Class A the RJ45 cables attached to this module's Ethernet ports must have ferrite beads (Fair-Rite 0431164281 or equivalent) present at both ends of the cable.
LSM1000XMSP12-01	LSM1000XMSP12-01	12-port Dual-PHY RJ45 10/100/1000 Mbps Gigabit Ethernet and SFP fiber. A 750FL or 750GL PowerPC Processor with a minimum of 256MB per port of CPU memory and 256KB of layer 2 cache running at 600MHz.
LSM1000XMVDC4-01	LSM1000XMVDC4-01	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC4-NG	LSM1000XMVDC4-NG	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC8-01	LSM1000XMVDC8-01	8-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC12-01	LSM1000XMVDC12-01	12-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM1000XMVDC16-01	LSM1000XMVDC16-01	16-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps. 1GB port CPU memory, full-featured L2-L7 with FCoE enabled; Fiber ports require SFP transceivers, options include SFP-LX, SFP-SX, and SFP-CU.
LSM10/100/1000XMVDC16NG	LSM10/100/1000XMVDC16NG The Part Number of this load module is 944-1072-01.	16-port XMVDC16NG load module is Ixia's Fusion-enabled version of the existing LSM XMVDC16 load module. These two load modules are physically similar. The hardware components and application specifications remain unchanged. The key difference is the IxN2X capability to run the load module in IxN2X mode.
LM1000STXS2	LM1000STXS2	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module. Does not include SFP transceivers.

Table 16-1. Part Numbers for 10/100/1000 Modules

Load Module	Price List Names	Description
LM1000STXS4	LM1000STXS4 LM1000STXS4-256	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet load module. -256 version has 256MB of processor memory per port. Does not include SFP transceivers. **Note**: In order to meet the emissions requirements of FCC part 15 Class A the RJ45 cables attached to this module's Ethernet ports must have ferrite beads (Fair-Rite 0431164281 or equivalent) present at both ends of the cable.
LM1000STX2	LM1000STX2	2-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Load Module. Supports Layer 2-3 stream generation only. No support for routing, Layer 4-7 applications and the Linux SDK. Does not include any SFP transceivers.
LM1000STX4	LM1000STX4	4-port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Load Module. Supports Layer2-3 stream generation only. No support for routing, Layer 4-7 applications and the Linux SDK. Does not include any SFP transceivers.
LM1000TX4	LM1000TX4	4-port 10/100/1000 Mbps Base-T Ethernet copper, reduced features. No support for routing protocols, Linux SDK, or L4-L7 applications.
LM1000TXS4	LM1000TXS4 LM1000TXS4-256	4-port 10/100/1000 Mbps Base-T Ethernet copper. -256 version has 256MB of processor memory per port.
LM1000T-5		2-port multilayer 10/100/1000 Mbps Base-T Ethernet.
ALM1000T8	ALM1000T8	8-port 10/100/1000 Mbps Base T Ethernet copper. Supports Real World Traffic Suite (includes IxVPN, IxChariot and IxLoad), and independent Linux-based SDK applications.
CPM1000T8	CPM1000T8	8-port 10/100/1000 Mbps Base T Ethernet copper. Supports Real World Traffic Suite (includes IxVPN, IxChariot and IxLoad), and independent Linux-based SDK applications, with 2GB of memory.
ELM1000ST2	ELM1000ST2	2-port Dual PHY (RJ45 and SFP) 10/100/1000 Mbps Ethernet Load Module featuring hardware-based high-speed IPSec encryption for use with IxVPN.
OLM1000STX24	OLM1000STX24	24-port 10/100/1000Mbps Dual-Phy (Copper/Fiber) for Optixia XL10, reduced features. No support for routing protocols, Linux SDK, or L4-L7 applications.
OLM1000STXS24	OLM1000STXS24	24-port 10/100/1000 Mbps Dual-Phy (Copper/Fiber) for Optixia XL10.
	SFP-LX	1310 nm LX SFP transceiver used with LM1000STX2, LM1000STX4, LM1000STXS2, LM1000STXS4, LM1000STXS4-256, OLM1000STX24, and OLM1000STXS24.

Table 16-1. Part Numbers for 10/100/1000 Modules

Load Module	Price List Names	Description
	SFP-SX	850 nm SX SFP transceiver used with LM1000STX2, LM1000STX4, LM1000STXS2, LM1000STXS4, LM1000STXS4-256, OLM1000STX24, OLM1000STXS24, LSM1000XMV(R)4-01, LSM1000XMV(R)8-01, LSM1000XMV(R)12-01, and LSM1000XMV(R)16-01.
LSM1000XMVDC4-NG		4-port LSM1000XMVDC4NG-01,GIGABIT ETHERNET LOAD MODULE

Specifications

The load module specifications are contained in *Table 16-2* on page 16-7 and Table 16-3 on page 16-8. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in the *Ixia Load Modules* on page 1-4.

Table 16-2. 10/100/1000 Load Module Specifications—Part 1

	ALM1000T8, CPM1000T8[1]	ELM1000ST2	LM1000T-5
# ports	8	2	2
-3 Card Available	N	N	N
Layer2/Layer3 Card?	N	N	N
Data Rate	10/100/1000 Mbps	10/100/1000 Mbps	10/100/1000 Mbps[2]
Connector	RJ-45 (copper)	RJ-45 (copper) and SFP (fiber)	RJ-45 (copper)
Interfaces	1000Base-T 100Base-TX 10Base-T	1000Base-X 1000Base-T 100Base-TX 10Base-T	1000Base-T 100Base-TX 10Base-T
Capture buffer size	N/A	N/A	4MB
Captured packet size	N/A	N/A	12-13k
Streams per port	N/A	N/A	255
Advanced scheduler streams per port	N/A	N/A	N/A
Flows per port	N/A	N/A	15872
Preamble size: min-max	N/A	N/A	2-254 bytes (10/100) 6-254 bytes (1000)
Frame size: min-max	N/A	N/A	12-9k bytes (10/100) 40-13k bytes (1000)
Inter-frame gap: min-max	N/A	N/A	10: 6400ns-1717s in 400ns steps 100: 640ns-171s in 40ns steps 1000:64ns-68sec in 16ns steps

Table 16-2. 10/100/1000 Load Module Specifications—Part 1

	ALM1000T8, CPM1000T8[1]	ELM1000ST2	LM1000T-5
Inter-burst gap: min-max	N/A	N/A	10: 6400ns-1717s in 400ns steps 100: 640ns-171s in 40ns steps 1000:64ns-68sec in 16ns steps
Inter-stream gap: min-max	N/A	N/A	10: 6400ns-1717s in 400ns steps 100: 640ns-171s in 40ns steps 1000:64ns-68sec in 16ns steps
Latency	N/A	N/A	20ns resolution

1. Due to power requirements, only one CPM1000T8 module can be used in a 250 or 400T chassis. Other modules can be used with the CPM1000T8 in the same chassis, but only one CPM1000T8 at a time (except MSM family of modules, which has the same limitation).
2. Odd frame sizes can cause diminishment in the actual data rate on this modules.

Table 16-3. 10/100/1000 Load Module Specifications—Part 2

	LM1000STX2 LM1000STX4 OLM1000STX24	LM1000STXS2 LM1000STXS4 LM1000STXS4-256 LSM1000XMS12-01 LSM1000XMSR12-01 LSM1000XMSP12-01 LSM1000XMV4/8/12/16-01 LSM1000XMVR4/8/12/16-01 LSM1000XMVDC4/8/12/16-01 OLM1000STXS24	LM1000TX4	LM1000TXS4 LM1000TXS4-256
# ports	2 (STX2) 4 (STX4) 24 (STX24)	2 (STXS2) 4 (STXS4) 4 (XMV(R)4) 4 (XMVDC4) 8 (XMV(R)8) 8 (XMVDC8) 12 (XMV(R)12) 12 (XMS12/XMSR12) 12 (XMSP12) 12 (XMVDC12) 16 (XMV16/XMVR16) 16 (XMVDC16) 16 (XMVDC16NG) 24 (STXS24)	4	4
-3 Card Available	N	N	N	N
Layer2/Layer3 Card?	Y	Y	Y	Y
Data Rate	10/100/1000 Mbps	10/100/1000 Mbps	10/100/1000 Mbps	10/100/1000 Mbps

Table 16-3. 10/100/1000 Load Module Specifications—Part 2

	LM1000STX2 **LM1000STX4** **OLM1000STX24**	**LM1000STXS2** **LM1000STXS4** **LM1000STXS4-256** **LSM1000XMS12-01** **LSM1000XMSR12-01** **LSM1000XMSP12-01** **LSM1000XMV4/8/12/16-01** **LSM1000XMVR4/8/12/16-01** **LSM1000XMVDC4/8/12/16-01** **OLM1000STXS24**	**LM1000TX4**	**LM1000TXS4** **LM1000TXS4-256**
Connector	Dual: RJ-45 (copper) and SFP (fiber)	Dual: RJ-45 (copper) and SFP (fiber) (1000 Mbps only)	RJ-45 (copper)	RJ-45 (copper)
Interfaces	1000Base-X 1000Base-T 100Base-TX 10Base-T	1000Base-X 1000Base-T 100Base-TX 10Base-T LSM1000XMV(R)4/8/12/16-01 and LSM1000XMVDC4/8/12/16-01 also have 100Base-FX	1000Base-T 100Base-TX 10Base-T	1000Base-T 100Base-TX 10Base-T
Ambient Operating Temperature Range		LSM1000XMV16-01 and LSM1000XMVR16-01 41°F to 86°F (5°C to 30°C) **Note**: Using these load modules in the XM2 or XM12 chassis lowers the chassis maximum operating temperature.		
Capture buffer size	8MB	8MB	8MB	8MB
Captured packet size	12-13k bytes	12-13k bytes	12-13k bytes	12-13k bytes
Streams per port	256	256 4K (LSM1000XMV full version only)	256	256
Number of streams in Packet Stream Mode (Non Data Center Mode)	N	(For LSM1000XMVDC4/8/12/16-01 card) 4096	N	N

Table 16-3. 10/100/1000 Load Module Specifications—Part 2

	LM1000STX2 **LM1000STX4** **OLM1000STX24**	**LM1000STXS2** **LM1000STXS4** **LM1000STXS4-256** **LSM1000XMS12-01** **LSM1000XMSR12-01** **LSM1000XMSP12-01** **LSM1000XMV4/8/12/16-01** **LSM1000XMVR4/8/12/16-01** **LSM1000XMVDC4/8/12/16-01** **OLM1000STXS24**	**LM1000TX4**	**LM1000TXS4** **LM1000TXS4-256**
Number of streams in Advanced Scheduler Mode (Non Data Center Mode)	N	(For LSM1000XMVDC4/8/12/16-01 card) Fast: 16 Medium: 240 Slow: 3584	N	N
Number of streams in Advanced Scheduler Mode (Data Center Mode)	N	(For LSM1000XMVDC4/8/12/16-01 card) Fast: 16 Medium: 240	N	N
Advanced scheduler streams per port	256	256	256	256
Flows per port	N/A	N/A	N/A	N/A
Preamble size: min-max (bytes)	2-61 (10/100) 8-61 (1000 fiber) 6-61 (1000 copper)	2-61 (10/100) 8-61 (1000 fiber) 6-61 (1000 copper)	2-61 (10/100) 8-61 (1000 fiber) 6-61 (1000 copper)	2-61 (10/100) 8-61 (1000 fiber) 6-61 (1000 copper)
Frame size: min-max	12-13k bytes	12-13k bytes	12-13k bytes	12-13k bytes
Inter-frame gap: min-max	**Basic Scheduler:** 10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps **Advanced Scheduler:** 10: 6400ns-1717.99s in 800ns steps 100: 640ns-171.799s in 80ns steps 1000: 64ns-68.719 in 16ns steps	**Basic Scheduler:** 10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps **Advanced Scheduler:** 10: 6400ns-1717.99s in 800ns steps 100: 640ns-171.799s in 80ns steps 1000: 64ns-68.719 in 16ns steps	**Basic Scheduler:** 10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps **Advanced Scheduler:** 10: 6400ns-1717.99s in 800ns steps 100: 640ns-171.799s in 80ns steps 1000: 64ns-68.719 in 16ns steps	**Basic Scheduler:** 10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps **Advanced Scheduler:** 10: 6400ns-1717.99s in 800ns steps 100: 640ns-171.799s in 80ns steps 1000: 64ns-68.719 in 16ns steps

Table 16-3. 10/100/1000 Load Module Specifications—Part 2

	LM1000STX2 LM1000STX4 OLM1000STX24	**LM1000STXS2 LM1000STXS4 LM1000STXS4-256 LSM1000XMS12-01 LSM1000XMSR12-01 LSM1000XMSP12-01 LSM1000XMV4/8/12/16-01 LSM1000XMVR4/8/12/16-01 LSM1000XMVDC4/8/12/16-01 OLM1000STXS24**	**LM1000TX4**	**LM1000TXS4 LM1000TXS4-256**
Inter-burst gap: min-max	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-16.7ms in 16ns steps **Advanced Scheduler**: 10: 0.419s 100: 0.0419s 1000: 0.0167s	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-16.7ms in 16ns steps **Advanced Scheduler**: 10: 0.419s 100: 0.0419s 1000: 0.0167s	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-16.7ms in 16ns steps **Advanced Scheduler**: 10: 0.419s 100: 0.0419s 1000: 0.0167s	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-16.7ms in 16ns steps **Advanced Scheduler**: 10: 0.419s 100: 0.0419s 1000: 0.0167s
Inter-stream gap: min-max	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps	10: 6400ns-429s in 800ns steps 100: 640ns-42.9s in 80ns steps 1000: 64ns-4.29s in 16ns steps
Normal stream min frame rate	10: 0.00238fps 100: 0.0238fps 1000: 0.238fps	10: 0.00238fps 100: 0.0238fps 1000: 0.238fps	10: 0.00238fps 100: 0.0238fps 1000: 0.238fps	10: 0.00238fps 100: 0.0238fps 1000: 0.238fps
Advanced stream min frame rate	10: 0.000582fps 100: 0.00582fps 1000: 0.0146fps	10: 0.000582fps 100: 0.00582fps 1000: 0.0146fps	10: 0.000582fps 100: 0.00582fps 1000: 0.0146fps	10: 0.000582fps 100: 0.00582fps 1000: 0.0146fps
Latency	20ns resolution	20ns resolution	20ns resolution	20ns resolution
Table UDF feature (based on minimum packet size 64K)	96K (full) 32K (reduced)	786K (LSM1000XMV) 96K others (full) 32K others (reduced)	96K	96K
Max Value List Entries	48K	48K	N/A	48K
Max Range List Entries[1]	6K	6K	N/A	6K

1. 192k memory is shared between value list entries (at 4 bytes per entry) and range list entries (at 32 bytes per entry).

ALM1000T8 and CPM1000T8

The ALM100T8 and CPM1000T8 has a feature that is non-conformant with the IEEE 802.3 specification. According to the specification, all 4 pairs of signals must be connected in gigabit copper mode for auto-negotiation to function. On the ALM100T8 and CPM1000T8, if auto-negotiation fails using all 4 pairs, auto-negotiation is attempted using only the two pairs used in 10/100 modes. This allows auto-negotiation to succeed even if gigabit mode is enabled for auto-negotiation and a 10/100 only cable is used.

Card LEDs

Each OLM1000STXS24 card incorporates a set of 8 LEDs, as described in Table 16-4.

Table 16-4. 10/100/1000 Card LEDs for OLM1000STXS24, OLM1000STX24

LED Label	Usage
48V	Green if 48V power is available to the board. Red if not available.
3.3V	Green if 3.3V power is available to the board. Red if not available.
2.5V	Green if 2.5V power is available to the board. Red if not available.
1.8V	Green if 1.8V power is available to the board. Red if not available.
Ready	The card is ready for operation.
Aux1	Not currently used.
Aux2	Not currently used.
Fault	Red if a fault is present on the board.

Each ELM1000ST2, LM1000STX2/4 and LM1000STXS2/4 card incorporates a single LED, as described in Table 16-5.

Table 16-5. 10/100/1000 Card LEDs for ELM1000ST2, LM1000STX2/4 and LM1000STXS2/4

LED Label	Usage
Trig	The value of the ‘OR’ function of all of the trigger out ports on the board. The LED’s color is orange.

The ALM1000T8 has a card-level ‘mgmt’ LED next to Port 8. This LED is not currently used.

Port LEDs

Each port on the ALM1000T8 module incorporates a set of 2 LEDs, as described in Table 16-6. The ALM1000T8 also has a card-level ‘mgmt’ LED next to Port 8; this LED is not currently used.

Table 16-6. ALM100T8 and CPM1000T8 Port LEDs

LED Label	Usage
Link/Tx (Upper LED)	Color is used to indicate the link speed: • 1000Mbps–Green • 100Mbps–Orange • 10Mbps–Yellow Flashing indicates transmit activity. Off if link is down.
Rx/Error (Lower LED)	Three conditions apply: • Full duplex or master (in 1000 Mbps case): Green with extended pulses off to indicate receive activity. • Half duplex or subordinate (in 1000 Mbps case): Off with extended green pulses to indicate receive activity. • Error: Overrides the other two modes, with extended orange pulses. • No link: Off.

Each LM1000T-5 port incorporates a set of 8 LEDs, as described in Table 16-7 on page 16-13.

Table 16-7. LM1000T-5

LED Label	Usage
Mstr	Green if the port is the master in a Gigabit connection.
Half	Green for half duplex operation.
1000	Green if the port is configured for Gigabit operation.
100	Green if the port is configured for 100 Mbps operation.
10	Green if the port is configured for 10 Mbps operation.
Tx/Col	Green during data transmission. Red during collisions.
Rx/Err	Green during error free reception. Red if errors are received.
Trig	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Each LM1000TXS4 port incorporates a set of 6 LEDs, as described in Table 16-8.

Table 16-8. Port LEDS for LM1000TXS4 and LM1000TX4

LED Label	Usage
Slave	On for subordinate mode in a Gigabit connection.
Half	Green for half duplex operation.
Link	Green for 1000 Mbps link, orange for 100 Mbps link, yellow for 10 Mbps link, and off for no link.
Tx/Col	Green during data transmission. Red during collisions.
Rx/Err	Green during error free reception. Red if errors are received.
Trigger	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Each OLM1000STXS24 port incorporates a set of 2 LEDs, as described in Table 16-9.

Table 16-9. Port LEDs for OLM1000STXS24, OLM1000STX24, LSM1000XMV4/8/12/16-01, and LSM1000XMS12-01

LED Label	Copper	Fiber
Link/Tx (Upper LED)	Color is used to indicate the link speed: • 1000Mbps–Green • 100Mbps–Orange • 10Mbps–Yellow Flashing indicates transmit activity. Off if link is down.	Green indicates link has been established and flashes during transmit activity.
Rx/Error (Lower LED)	Three conditions apply: • Full duplex or master (in 1000 Mbps case): Green with extended pulses off to indicate receive activity. • Half duplex or subordinate (in 1000 Mbps case): Off with extended pulses to indicate receive activity. • Error: Overrides the other two modes and pulses red. • No link: Off.	Green indicates link has been established and flashes during receive activity. Continuous red indicates a receive error.

Each ELM1000ST2, LM1000STX2, LM1000STX4, LM1000STXS2, LM1000STXS4, and LM1000STXS4-256 port incorporates a set of 6 LEDs, as described in Table 16-10 on page 16-15. The LEDs are arranged next to the two connectors associated with each port: Speed, Slave, and RJ45 Link/Tx/Coll are next to the RJ45 connector and Rx/Err, Half, and SFP Link/Tx/Coll are next to the SFP connector.

Table 16-10. Port LEDs for ELM1000ST2, LM1000STX2, LM1000STX4, LM1000STXS2, LM1000STXS4, and LM1000STXS4-256

LED Label	Usage
Speed	• Off for 10Mbps. • Orange for 100Mbps. • Green for 1000Mbps.
Slave	• On in slave or subordinate mode. • Off otherwise.
RJ45 Link/Tx	• Off if SFP is the active connector. • Steady Orange for no link. • Flashing Orange for link with collision. • Steady Green for link with no transmit. • Flashing green during transmit.
Rx/Err	• Flashes green on data receive. • Steady Red for error.
Half	• Green for half-duplex mode. • Off for full-duplex mode.
SFP Link/Tx/Coll	• Off if RJ45 is the active connector. • Steady Orange for no link. • Flashing Orange for link with collision. • Steady Green for link with no transmit. • Flashing green during transmit.

Trigger Out Values

The signals available on the trigger out pins for the LM1000T5 card is described in *Table 16-11*.

Table 16-11. LM1000T-5 Trigger Out Signals

Pin	Signal
1	Port 1: 10 ns high pulse for each packet matching User Defined Statistic 1
2	Port 2: 10 ns high pulse for each packet matching User Defined Statistic 1
3	Port 1: Low during transmit of frame, otherwise high
4	Port 2: Low during transmit of frame, otherwise high
5	Ground
6	Reserved

There is no trigger connector on the ALM100T8 and CPM1000T8.

The ELM1000ST2's triggers are not currently used.

The signals available on the trigger out pins for the LM1000TXS4, LM1000TX4, LM1000STXS4, LM1000STX4, LM1000STXS4-256, LM1000STXS2, and LM1000STX2 cards is described in *Table 16-12*.

Table 16-12. LM1000TXS4, LM1000TX4, LM1000STXS4, LM1000STX4, LM1000STXS4-256, LM1000STXS2, and LM1000STX2 Trigger Out Signals

Pin	Signal
1	660ns negative pulse when User Defined Statistic 1 is true.
2	660ns negative pulse when User Defined Statistic 1 is true.
3	660ns negative pulse when User Defined Statistic 1 is true.
4	660ns negative pulse when User Defined Statistic 1 is true.
5	Ground
6	Ground

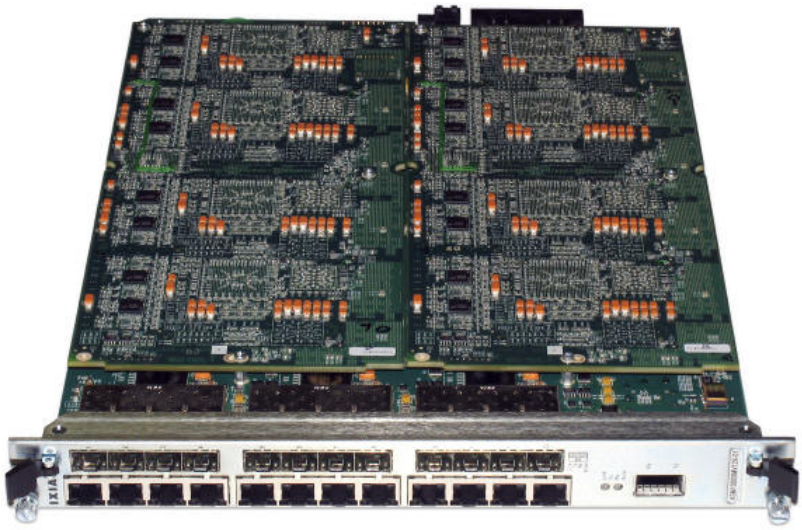
Statistics

Statistics for 10/100/1000 cards, under various modes of operation may be found in the Appendix B, *Available Statistics*.

17 IXIA 1GbE and 10GbE Aggregation Load Modules

Ixia's Gigabit and 10 Gigabit Ethernet application and streams modules ASM1000XMV12X is an Ethernet module with additional aggregation capability. It features 12 ports of 10/100/1000Mbps Ethernet configurable in either aggregation mode, stream mode, or as 1 port of 10GE aggregation. It can provide 144 GigE ports in the Optixia XM12 or 24 GigE ports in the Optixia XM2. The ASM1000XMV12X-01 module is shown in Figure 17-1.

Figure 17-1. ASM1000XMV12X-01 Application Load Module



The ASM1000XMV12X module offers complete Layer 2-7 network and application testing functionality in a single Optixia XM load module. The twelve Gig Ethernet ports may either be used individually or aggregated through a 10 Gigabit Ethernet port. This architecture allows the processing power and resources of up to twelve per-port CPUs to be combined into one physical port, providing the highest Layer 4-7 line-rate performance, unmatched in any other Layer 4-7 test solution. Each test port supports wire-speed Layer 2-3 traffic generation and analysis, high-performance routing/bridging protocol emulation, and true Layer 4-7 application traffic generation and subscriber emulation. Using 12 GbE ports per module, ultra-high density test environments can be created for

auto-negotiable 10/100/1000 Mbps Ethernet over copper as well as fiber. With 12 slots per Optixia XM12 chassis, up to 144 Gigabit Ethernet and 12 10GbE test ports are available in a single test system.

Application Layer Performance Testing

The Gigabit Ethernet ASM1000XMV12X module supports high performance testing of content-aware devices and networks through the Aptixia IxLoad application. IxLoad creates real-world traffic scenarios at the TCP/UDP (Layer 4) and Application (Layer 7) layers, emulating clients and servers for Web (HTTP, SSL), FTP, Email (SMTP, POP3, IMAP), Streaming (RTP, RTSP), Video (MPEG2, MPEG4, IGMP), Voice (SIP, MGCP), and services such as DNS, DHCP, LDAP and Telnet. Each GE XMV port can be independently configured to run different protocols and client/server scenarios.

Modes of Operation

The ASM1000XMV12X module can operate in three different modes providing a flexible, scalable and powerful layer 4-7 performance.

Non-Aggregated Mode

In this mode, the twelve 10/100/1000Mbps ports provide L2-L7 XMV functionality. Each port is capable of providing high performance packet generation and application layer testing by employing its own port CPU resources as well as the dedicated hardware stream engine. In this mode the 10GE Aggregation Port is disabled.

Gigabit Aggregated Mode

Gigabit Aggregated Mode allows the twelve PCPUs to be assigned to any of 12 GbE test ports through the switch fabric. Aggregation of the processing power allows application layer testing at line rate regardless of the test objective. A cluster of PCPU's can be assigned to any of the physical ports. Multiple clusters and their assigned physical ports can exist on the same module. Aptixia applications transparently configure the available PCPU resources and make the assignment to the physical port(s) to achieve the test objectives. This mode is exclusive to L4-7 testing and there is no support for hardware stream engine. In this mode the 10GE Aggregation Port is disabled.

10GE Aggregated Mode

In 10GE Aggregated Mode, all of the twelve PCPUs are assigned to the 10GE Aggregation Port through the switch fabric. Aggregation of the processing power allows application layer testing at line rate (10 Gbps). Aptixia applications transparently configure the PCPU resources to achieve the test objectives. This mode is exclusive to L4-7 testing and there is no support for hardware stream engine. In this mode the twelve Gigabit ports are disabled.

Flexible Packet Generation

Each ASM1000XMV12X test port is capable of generating precisely controlled network traffic at up to wire speed of the network interface using Ixia's IxExplorer test application. Up to millions of packet flows can be configured on

each port with fully customizable packet header fields. Flexible header control is available for Ethernet, IPv4/v6, IPX, ARP, TCP, UDP, VLANs, QinQ, MPLS, GRE, and many others. Payload contents can also be customized with incrementing/decrementing, fixed, random, or user-defined information. Frame sizes can be fixed, varied according to a pattern, or randomly assigned across a weighted range. Rate control can be flexibly defined in frames per second, bits per second, percentage of line rate, or inter-packet gap time.

Real-Time Latency

Packets representing different traffic profiles can be associated with Packet Group Identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time for each packet belonging to different groups. Measurable latencies include:

- Instantaneous latency and inter-arrival time where each packet is associated with one group ID
- Latency bins, where PGIDs can be associated with a latency range
- Latency over time, where multiple PGIDs can be placed in ‘time buckets’ with fixed durations
- First and last time stamps, where each PGID can store the timestamps of first and last received packets

Transmit Scheduler

There are two modes of transmission are available - Packet Stream and Advanced Stream Scheduler:

Packet Stream Scheduler

In Packet Stream Scheduler mode, the transmit engine allows configuration of up to 256 unique sequential stream groupings on each port. Multiple streams can be defined in sequence, each containing multiple packet flows defined by unique characteristics. After transmission of all packets in the first stream, control is passed to the next defined stream in the sequence. After reaching the last stream in the sequence, transmission may either cease, or control may be passed on to any other stream in the sequence. Therefore, multiple streams are cycled through, representing different traffic profiles to simulate real network traffic.

Advanced Stream Scheduler

In Advanced Stream Scheduler mode, the transmission of stream groupings is interleaved per port. For example, assume a port is configured with three streams. If Stream 1 is defined with IP packets at 20% of line rate, Stream 2 is defined with TCP packets at 50% of line rate, and Stream 3 is defined with MPLS packets at 30% of line rate, data on the port is transmitted at an aggregate utilization of 100% with interleaved IP, TCP, and MPLS packets.

Extensive Statistics

- Real-time 64-bit frame counts and rates
- Spreadsheet presentation format for convenient manipulation of statistics counters

- Eight Quality of Service counters (supporting 802.1p, DSCP, and IPv4 TOS measurements)
- Six user-defined statistics that use a trigger condition
- Extended statistics for ARP, ICMP, and DHCP
- Transmit stream statistics for frame counts and rate
- External logging to file for statistics and alerts
- Audible and visual alerts with user-definable thresholds

Data Capture

Each port is equipped with 64 MB of capture memory, capable of storing tens of thousands of packets in real time. The capture buffer can be configured to store packets based on user-defined trigger and filter conditions. Decodes for IPv4, IPv6, UDP, ARP, BGP-4, IS-IS, OSPF, TCP, DHCP, IPX, RIP, IGMP, CISCO ISL, VLAN, and MPLS are provided.

Data Integrity

As packets traverse through networks, IP header contents may change, resulting in the recalculation of packet CRC values. To validate device performance, the data integrity function of the Gigabit Ethernet ASM1000XMV12X module allows packet payload contents to be verified with a unique CRC that is independent of the packet CRC. This ensures that the payload is not disturbed as the device changes header fields.

Sequence and Duplicate Packet Checking

Sequence numbers can be inserted at a user-defined offset in the payload of each transmitted packet. Upon receipt of the packets by the Device Under Test (DUT), out-of sequence errors or duplicated packets are reported in real time at wire-speed rates. You can define a sequence error threshold to distinguish between small versus big errors, and the receive port can measure the amount of small, big, reversed, and total errors. Alternatively, you can use the duplicate packet detection mode to observe that multiple packets with the same sequence number are received and analyzed.

Routing/Bridging Protocol Emulation

Ixia's Gigabit Ethernet ASM1000XMV12X module supports performance and functionality testing using routing/bridging protocol emulation through the Aptixia IxNetwork and Aptixia IxAutomate applications. Protocols supported include IPv4/IPv6 routing (BGP-4, OSPF, IS-IS, and RIP), MPLS (RSVP-TE, LDP, L2 MPLS VPNs, L3 MPLS VPNs, and VPLS), multicast (IGMP, MLD, and PIM-SM), and bridging (STP, RSTP, MSTP). Highly scalable scenarios can be created emulating up to thousands of routers advertising millions of routes per test port. Up to wire-speed Layer 2/3 traffic can be automatically created to target routes and MPLS tunnels.

Part Numbers

The part numbers are shown in *Table 17-1*.

Table 17-1. Part Numbers for Gigabit Modules

Load Module	Price List Name	Description
ASM1000XMV12X-01	ASM1000XMV12X-01	10 Gigabit Ethernet, Application and Stream Load Module, 1-10G or 12-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, for OPTIXIA XM2 or OPTIXIA XM12 chassis; CPU with 1Gigabyte of memory per GbE port; On-Board Port Aggregation; GbE Fiber Ports REQUIRE SFP transceivers, options include SFP-LX or SFP-SX; and 10GbE port requires a XFP transceiver, options are either 948-0003 (XFP-850), XFP-1310, or XFP-1550
	SFP-SX	850nm SX SFP transceiver
	SFP-LX	SFP Transceiver - 1310nm LX
	XFP-850 (948-0003-01)	XFP 850nm Transceiver
	XFP-1550	XFP 1550nm Transceiver
	XFP-1310	XFP 1310nm Transceiver

Specifications

The load module specifications are contained in *Table 17-2* on page 17-5. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 17-2. Load Module Specifications

	ASM1000XMV12X-01
Number of ports	12 GbE (10/100/1000) + 10GbE
Maximum Ports per Chassis	144 GbE + 12 10GbE
Connector	RJ-45 and SFP for GbE ports; XFP for 10GbE port
Interfaces	Port 1 to port 12: 1000Base-X 100Base-FX 1000Base-T 100Base-TX 10Base-T Port 13: 10GBase-X
Port CPU	PowerPC 750GL x12 Port CPU Speed: 800 MHz Port CPU Memory: 1GB

Table 17-2. Load Module Specifications

	ASM1000XMV12X-01
Ambient Operating Temperature Range	41°F to 86°F (5°C to 30°C) **Note**: Using this load module in the XM2 or XM12 chassis lowers the chassis maximum operating temperature.
Connection rate (cps)	200K (in aggregated mode)
Layer 2-3 Routing Protocol and Emulation	Yes
Layer 4-7 Application Traffic Testing	Yes
Capture Buffer per Port	64MB
Number of Transmit Flows per Port (sequential values)	Bilions
Number of Transmit Flows per Port (arbitrary values)	98K
Number of Trackable Receive Flows per Port (PGIDs)	128K
Number of Stream Definitions per Port	Up to 4K in Packet Stream Mode (sequential) or Advanced Stream (interleaved) modes. Each Stream Definition can generate millions of unique traffic flows.
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
Receive Engine	Wire-speed packet filtering, capturing, real-time latency for each packet group, data integrity, and sequence checking.
User Defined Field (UDF) Features	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained. Value list = 48K; Range list = 6K.
Table UDF Feature	Comprehensive packet editing function for emulating large numbers of sophisticated flows. Up to 786K table UDF entries are supported on the XMV12X.
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse).
Data Field (per stream)	Fixed, increment (Byte/Word), decrement (Byte/Word), random, repeating, user-specified up to 13K bytes.

Table 17-2. Load Module Specifications

	ASM1000XMV12X-01
Statistics and Rates: Counter Size: 64-Bit	Link State, Line Speed, Frames Sent, Valid Frames Received, Bytes Sent/Received, Fragments, Undersize, Oversize, CRC Errors, VLAN Tagged Frames, User-Defined Stat 1, User- Defined Stat 2, Capture Trigger (UDS 3), Capture filter (UDS 4), User-Defined Stat 5, User-Defined Stat 6, 8 QoS counters, Data Integrity Frames, Data Integrity Errors, Sequence Checking Frames, Sequence Checking Errors, ARP, and Ping requests and replies.
Error Generation	CRC (Good/Bad/None), Undersize, Oversize.
Packet Flow Statistics	Real-time statistics to track up to 128K packet flows on the XMV12X with throughput and latency measurements.
Latency Measurements	20 ns resolution.
IPv4, IPV6, UDP, TCP	Hardware checksum generation.
Frame Length Controls	Fixed, random, weighted random, or increment by user-defined step, random, weighted random.
Applications	Aptixia IxLoad: Layer 4-7 performance testing of content-aware devices and networks. Aptixia IxNetwork: Integrated Layer 2-3 data/ control plane performance and functional testing, supporting routing, bridging, MPLS, and multicast protocols. Aptixia IxAutomate: Automation environment providing pre-built tests for Layer 2-7 data and control plane testing. IxExplorer: Layer 2-3 wire-speed traffic generation and analysis. IxChariot®: Emulated application performance testing over Layer 4. IxAccess: Broadband access performance testing, including PPPoX and L2TPv2/v3. IxVPN: Performance verification of IPSec devices and networks. Tcl API: Custom user script development for Layer 2-7 testing. Linux Software Development Kit (SDK): Custom user application development. Full TCP/IP connectivity through management interface (Telnet, FTP, and so on.)

Port LEDs

Each ASM1000XMV12X port incorporates a set of two LEDs, as described in Table 17-3. The 1GbE LEDs are used in Normal and 1GbE Aggregate modes. They behave identically in both modes, except that due to switch limitations, the 'CRC Error' LED is non-operational in 1GE Aggregate mode (that is, it never indicates error). The 1GE LEDs are disabled (always off) in 10GE Aggregate mode.

Table 17-3. 1GE Port LEDs for ASM1000XMV12X

LED Label	Copper	Fiber
1GE Link/Tx (Upper LED)	Color is used to indicate the link speed: • 1000Mbps–Green • 100Mbps–Orange • 10Mbps–Yellow Flashing indicates transmit activity. Off if link is down.	Green indicates link has been established and flashes during transmit activity. No link = off.
1GE Rx/ Error (Lower LED)	Three conditions apply: • Full duplex or master (in 1000 Mbps case): Green with extended pulses off to indicate receive activity. • Half duplex or subordinate (in 1000 Mbps case): Off with extended pulses to indicate receive activity. • Error: Overrides the other two modes and pulses red (supported only in Normal mode). • No link: Off.	Green indicates link has been established and flashes during receive activity. Continuous red indicates a receive error (supported only in Normal mode).

10GE LEDs are disabled (always off) in Normal and 1GE Aggregate modes. In 10GE Aggregate mode, the two LEDs behave as described in Table 17-4.

Table 17-4. 10GE Port LEDS for ASM1000XMV12X

LED Label	Usage
10GE Link/ Tx (Upper LED)	Green indicates link has been established. Flashes during transmit activity. No link = off.
10GE Rx/ Error (Lower LED)	Green indicates link has been established. Flashes during receive activity. No link = off.

Statistics

Statistics for 10/100/1000 cards, under various modes of operation may be found in the Appendix B, *Available Statistics*.

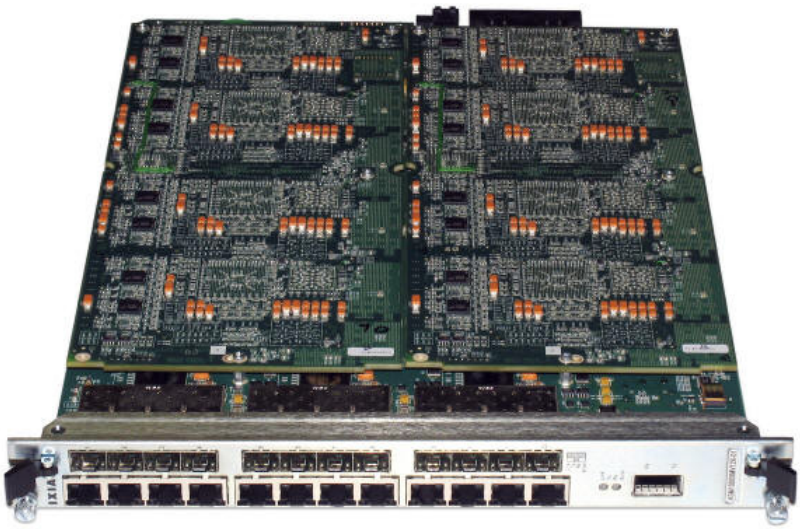
18 IXIA Network Processor Load Modules

This chapter provides details about Ixia's Xcellon-Ultra XP and Xcellon-Ultra NP load modules—the specificatons, features, and functionality. It also provides details on Xcellon-Ultra load module when it operates in IxN2X mode.

Ixia's Gigabit and 10 Gigabit Ethernet Network Processor load modules Xcellon-Ultra XP and Xcellon-Ultra NP. These are Ethernet modules with additional aggregation capability. Each features 12 ports of 10/100/1000Mbps Ethernet configurable in either aggregation mode, stream mode, or as 1 port of 10GE aggregation. The Xcellon-Ultra module can provide 144 GigE ports in the Optixia XM12 or 24 GigE ports in the Optixia XM2. The Xcellon-Ultra XP-01 module is shown in Figure 18-1.

IxN2X capability is added to the regular Xcellon-Ultra load module to use it in IxN2X mode. Xcellon-Ultra XP and NP and Xcellon-Ultra NG load modules share similar physical properties. In addition to the physical properties, Xcellon-Ultra NG supports IxN2X mode.

Figure 18-1. Xcellon-Ultra XP-01 Application Load Module



The Xcellon-Ultra module offers complete Layer 2-7 network and application testing functionality in a single Optixia XM load module. The twelve Gig Ethernet ports may either be used individually or aggregated through a 10 Gigabit Ethernet port. This architecture allows the processing power and resources of up to twelve per-port CPUs to be combined into one physical port, providing the highest Layer 4-7 line-rate performance, unmatched in any other Layer 4-7 test solution. Each test port supports wire-speed Layer 2-3 traffic generation and analysis, high-performance routing/bridging protocol emulation, and true Layer 4-7 application traffic generation and subscriber emulation. Using 12 GbE ports per module, ultra-high density test environments can be created for auto-negotiable 10/100/1000 Mbps Ethernet over copper as well as fiber. With 12 slots per Optixia XM12 chassis, up to 144 Gigabit Ethernet and 12 10GbE test ports are available in a single test system.

Application Layer Performance Testing

The Gigabit Ethernet Xcellon-Ultra module supports high performance testing of content-aware devices and networks through the Aptixia IxLoad application. IxLoad creates real-world traffic scenarios at the TCP/UDP (Layer 4) and Application (Layer 7) layers, emulating clients and servers for Web (HTTP, SSL), FTP, Email (SMTP, POP3, IMAP), Streaming (RTP, RTSP), Video (MPEG2, MPEG4, IGMP), Voice (SIP, MGCP), and services such as DNS, DHCP, LDAP and Telnet. Each GE XMV port can be independently configured to run different protocols and client/server scenarios.

Real-time Transport Protocol (RTP) Feature

For the Xcellon-Ultra XP and NP modules, the RTP engine built into the FPGA can generate and terminate audio streams (video and data traffic is an option, too). The RTP engine works together with the VoIP Peer signaling protocols present in IxLoad. On a physical port the traffic is a mixture of signaling traffic generated and analyzed by PCPU, RTP traffic generated by CPCU, and RTP traffic generated by hardware.

The RTP feature is selectable from the Port Properties—Operation Mode tab in IxExplorer. For details, see the *IxExplorer User Guide*, Chapter 18, topic *Port Properties for Xcellon-Ultra and ASM1000XMV12X Modules*.

Modes of Operation

The Xcellon-Ultra modules can operate in three different modes providing a flexible, scalable and powerful layer 4-7 performance.

Non-Aggregated (Normal) Mode

In this mode, the twelve 10/100/1000Mbps ports provide L2-L7 XMV functionality. Each port is capable of providing high performance packet generation and application layer testing by employing its own port CPU resources as well as the dedicated hardware stream engine. In this mode the 10GE Aggregation Port is disabled.

Gigabit Aggregated Mode

Gigabit Aggregated Mode allows the twelve PCPUs to be assigned to any of 12 GbE test ports through the switch fabric. Aggregation of the processing power allows application layer testing at line rate regardless of the test objective. A cluster of PCPU's can be assigned to any of the physical ports. Multiple clusters and their assigned physical ports can exist on the same module. Aptixia applications transparently configures the available PCPU resources and make the assignment to the physical port(s) to achieve the test objectives. This mode is exclusive to L4-7 testing and there is no support for hardware stream engine. In this mode the 10GE Aggregation Port is disabled.

10GE Aggregated Mode

In 10GE Aggregated Mode, all of the twelve PCPUs are assigned to the 10GE Aggregation Port through the switch fabric. Aggregation of the processing power allows application layer testing at line rate (10 Gbps). Aptixia applications transparently configure the PCPU resources to achieve the test objectives. This mode is exclusive to L4-7 testing and there is no support for hardware stream engine. In this mode the twelve Gigabit ports are disabled.

Flexible Packet Generation

Each Xcellon-Ultra test port is capable of generating precisely controlled network traffic at up to wire speed of the network interface using Ixia's IxExplorer test application. Up to millions of packet flows can be configured on each port with fully customizable packet header fields. Flexible header control is available for Ethernet, IPv4/v6, IPX, ARP, TCP, UDP, VLANs, QinQ, MPLS, GRE, and many others. Payload contents can also be customized with incrementing/decrementing, fixed, random, or user-defined information. Frame sizes can be fixed, varied according to a pattern, or randomly assigned across a weighted range. Rate control can be flexibly defined in frames per second, bits per second, percentage of line rate, or inter-packet gap time.

Real-Time Latency

Packets representing different traffic profiles can be associated with Packet Group Identifiers (PGIDs). The receiving port measures the minimum, maximum, and average latency in real time for each packet belonging to different groups. Measurable latencies include:

- Instantaneous latency and inter-arrival time where each packet is associated with one group ID
- Latency bins, where PGIDs can be associated with a latency range
- Latency over time, where multiple PGIDs can be placed in ‘time buckets’ with fixed durations
- First and last time stamps, where each PGID can store the timestamps of first and last received packets

Transmit Scheduler

There are two modes of transmission are available - Packet Stream and Advanced Stream Scheduler:

Packet Stream Scheduler

In Packet Stream Scheduler mode, the transmit engine allows configuration of up to 256 unique sequential stream groupings on each port. Multiple streams can be defined in sequence, each containing multiple packet flows defined by unique characteristics. After transmission of all packets in the first stream, control is passed to the next defined stream in the sequence. After reaching the last stream in the sequence, transmission may either cease, or control may be passed on to any other stream in the sequence. Therefore, multiple streams are cycled through, representing different traffic profiles to simulate real network traffic.

Advanced Stream Scheduler

In Advanced Stream Scheduler mode, the transmission of stream groupings is interleaved per port. For example, assume a port is configured with three streams. If Stream 1 is defined with IP packets at 20% of line rate, Stream 2 is defined with TCP packets at 50% of line rate, and Stream 3 is defined with MPLS packets at 30% of line rate, data on the port is transmitted at an aggregate utilization of 100% with interleaved IP, TCP, and MPLS packets.

Extensive Statistics

- Real-time 64-bit frame counts and rates
- Spreadsheet presentation format for convenient manipulation of statistics counters
- Eight Quality of Service counters (supporting 802.1p, DSCP, and IPv4 TOS measurements)
- Six user-defined statistics that use a trigger condition
- Extended statistics for ARP, ICMP, and DHCP
- Transmit stream statistics for frame counts and rate
- External logging to file for statistics and alerts
- Audible and visual alerts with user-definable thresholds

Data Capture

Each port is equipped with 64 MB of capture memory, capable of storing tens of thousands of packets in real time. The capture buffer can be configured to store packets based on user-defined trigger and filter conditions. Decodes for IPv4, IPv6, UDP, ARP, BGP-4, IS-IS, OSPF, TCP, DHCP, IPX, RIP, IGMP, CISCO ISL, VLAN, and MPLS are provided.

Data Integrity

As packets traverse through networks, IP header contents may change, resulting in the recalculation of packet CRC values. To validate device performance, the data integrity function of Gigabit Ethernet Xcellon-Ultra modules allows packet payload contents to be verified with a unique CRC that is independent of the packet CRC. This ensures that the payload is not disturbed as the device changes header fields.

Sequence and Duplicate Packet Checking

Sequence numbers can be inserted at a user-defined offset in the payload of each transmitted packet. Upon receipt of the packets by the Device Under Test (DUT), out-of sequence errors or duplicated packets are reported in real time at wire-speed rates. You can define a sequence error threshold to distinguish between small versus big errors, and the receive port can measure the amount of small, big, reversed, and total errors. Alternatively, you can use the duplicate packet detection mode to observe that multiple packets with the same sequence number are received and analyzed.

Routing/Bridging Protocol Emulation

Ixia's Gigabit Ethernet Xcellon-Ultra modules support performance and functionality testing using routing/bridging protocol emulation through the Aptixia IxNetwork and Aptixia IxAutomate applications. Protocols supported include IPv4/IPv6 routing (BGP-4, OSPF, IS-IS, and RIP), MPLS (RSVP-TE, LDP, L2 MPLS VPNs, L3 MPLS VPNs, and VPLS), multicast (IGMP, MLD, and PIM-SM), and bridging (STP, RSTP, MSTP). Highly scalable scenarios can be created emulating up to thousands of routers advertising millions of routes per test port. Up to wire-speed Layer 2/3 traffic can be automatically created to target routes and MPLS tunnels.

Part Numbers

The part numbers are shown in *Table 18-1*.

Table 18-1. Part Numbers for Network Processor Modules

Load Module	Price List Name	Description
Xcellon-Ultra XP-01	Xcellon-Ultra XP-01	10 Gigabit Ethernet, Application and Stream Load Module, 1-10G or 12-Port Dual-PHY (RJ45 and SFP) 10/100/1000 Mbps, for OPTIXIA XM2 or OPTIXIA XM12 chassis; 800MHz CPU with 1GB of memory per GbE port; On-Board Port Aggregation; GbE Fiber Ports REQUIRE SFP transceivers, options include SFP-LX or SFP-SX; and 10GbE port requires a XFP transceiver, options are either 948-0003 (XFP-850), XFP-1310, or XFP-1550
Xcellon-Ultra NP-01	Xcellon-Ultra NP-01	Same as version above but 1GHz CPU and 2GB of memory.
Xcellon-Ultra NG-01	Xcellon-Ultra NG-01	Same as above.
	SFP-SX	850nm SX SFP transceiver
	SFP-LX	SFP Transceiver - 1310nm LX
	XFP-850 (948-0003-01)	XFP 850nm Transceiver
	XFP-1550	XFP 1550nm Transceiver
	XFP-1310	XFP 1310nm Transceiver

Specifications

The load module specifications are contained in *Table 18-2* on page 18-6. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 18-2. Load Module Specifications

	Xcellon-Ultra XP-01 **Xcellon-Ultra NP-01** **Xcellon-Ultra NG-01**
Number of ports	12 GbE (10/100/1000) + 10GbE
Maximum Ports per Chassis	144 GbE + 12 10GbE
Connector	RJ-45 and SFP for GbE ports; XFP for 10GbE port
Interfaces	Port 1 to port 12: **1000Base-X** 100Base-FX **1000Base-T (Aggregate, Copper mode)** **10/100/1000Base-T (Aggregate, Copper mode)** 100Base-TX 10Base-T Port 13: 10GBase-X **10G LAN XFP**
Port CPU	Xcellon-Ultra XP PowerPC 750GL x12 Port CPU Speed: 800 MHz Port CPU Memory: 1GB Xcellon-Ultra NP PowerPC 750GX x12 Port CPU Speed: 1 GHz Port CPU Memory: 2GB Xcellon-Ultra NG PowerPC 750GX x12 Port CPU Speed: 1 GHz Port CPU Memory: 2GB
Ambient Operating Temperature Range	41°F to 86°F (5°C to 30°C) **Note**: Using this load module in the XM2 or XM12 chassis lowers the chassis maximum operating temperature.
Connection rate (cps)	200K (in aggregated mode)

Table 18-2. Load Module Specifications

	Xcellon-Ultra XP-01 Xcellon-Ultra NP-01 Xcellon-Ultra NG-01
Layer 2-3 Routing Protocol and Emulation	Yes
Layer 4-7 Application Traffic Testing	Yes
Capture Buffer per Port	64MB
Number of Transmit Flows per Port (sequential values)	Bilions
Number of Transmit Flows per Port (arbitrary values)	98K
Number of Trackable Receive Flows per Port (PGIDs)	128K
Number of Stream Definitions per Port	Up to 4K in Packet Stream Mode (sequential) or Advanced Stream (interleaved) modes. Each Stream Definition can generate millions of unique traffic flows.
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
Receive Engine	Wire-speed packet filtering, capturing, real-time latency for each packet group, data integrity, and sequence checking.
User Defined Field (UDF) Features	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained. Value list = 48K; Range list = 6K.
Table UDF Feature	Comprehensive packet editing function for emulating large numbers of sophisticated flows. Up to 786K table UDF entries are supported on the XMV12X.
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)
Data Field (per stream)	Fixed, increment (Byte/Word), decrement (Byte/Word), random, repeating, user-specified up to 13K bytes.

Table 18-2. Load Module Specifications

	Xcellon-Ultra XP-01 Xcellon-Ultra NP-01 Xcellon-Ultra NG-01
Statistics and Rates: Counter Size: 64-Bit	Link State, Line Speed, Frames Sent, Valid Frames Received, Bytes Sent/Received, Fragments, Undersize, Oversize, CRC Errors, VLAN Tagged Frames, User-Defined Stat 1, User- Defined Stat 2, Capture Trigger (UDS 3), Capture filter (UDS 4), User-Defined Stat 5, User-Defined Stat 6, 8 QoS counters, Data Integrity Frames, Data Integrity Errors, Sequence Checking Frames, Sequence Checking Errors, ARP, and Ping requests and replies.
Error Generation	CRC (Good/Bad/None), Undersize, Oversize
Packet Flow Statistics	Real-time statistics to track up to 128K packet flows on the XMV12X with throughput and latency measurements.
Latency Measurements	20 ns resolution.
IPv4, IPV6, UDP, TCP	Hardware checksum generation.
Frame Length Controls	Fixed, random, weighted random, or increment by user-defined step, random, weighted random.
Applications	Aptixia IxLoad: Layer 4-7 performance testing of content-aware devices and networks. Aptixia IxNetwork: Integrated Layer 2-3 data/control plane performance and functional testing, supporting routing, bridging, MPLS, and multicast protocols. Aptixia IxAutomate: Automation environment providing pre-built tests for Layer 2-7 data and control plane testing. IxExplorer: Layer 2-3 wire-speed traffic generation and analysis. IxChariot®: Emulated application performance testing over Layer 4. IxAccess: Broadband access performance testing, including PPPoX and L2TPv2/v3. IxVPN: Performance verification of IPSec devices and networks. Tcl API: Custom user script development for Layer 2-7 testing. Linux Software Development Kit (SDK): Custom user application development. Full TCP/IP connectivity through management interface (Telnet, FTP, and so on.)

Port LEDs

Each Xcellon-Ultra port incorporates a set of two LEDs, as described in Table 18-3. The 1GbE LEDs are used in Normal and 1GbE Aggregate modes. They behave identically in both modes, except that due to switch limitations, the 'CRC Error' LED is non-operational in 1GE Aggregate mode (that is, it never indicates error). The 1GE LEDs are disabled (always off) in 10GE Aggregate mode.

Table 18-3. 1GE Port LEDs for Xcellon-Ultra Modules

LED Label	Copper	Fiber
1GE Link/Tx (Upper LED)	Color is used to indicate the link speed: • 1000Mbps-Green • 100Mbps-Orange • 10Mbps-Yellow Flashing indicates transmit activity. Off if link is down.	Green indicates link has been established and flashes during transmit activity. No link = off.
1GE Rx/ Error (Lower LED)	Three conditions apply: • Full duplex or master (in 1000 Mbps case)—green with extended pulses off to indicate receive activity. • Half duplex or subordinate (in 1000 Mbps case)—off with extended pulses to indicate receive activity. • Error—overrides the other two modes and pulses red (supported only in Normal mode). • No link—off.	Green indicates link has been established and flashes during receive activity. Continuous red indicates a receive error (supported only in Normal mode).

10GE LEDs are disabled (always off) in Normal and 1GE Aggregate modes. In 10GE Aggregate mode, the two LEDs behave as described in Table 18-4.

Table 18-4. 10GE Port LEDS for Xcellon-Ultra Modules

LED Label	Usage
10GE Link/ Tx (Upper LED)	Green indicates link has been established. Flashes during transmit activity. No link = off.
10GE Rx/ Error (Lower LED)	Green indicates link has been established. Flashes during receive activity. No link = off.

Statistics

Statistics for Xcellon-Ultra cards, under various modes of operation may be found in the Appendix B, *Available Statistics*.

19 IXIA 40/100 Gigabit Ethernet Load Modules

This chapter provides details about Ixia's K2 40-Gigabit and 100-Gigabit Ethernet test modules—the specifications and features.

Ixia's K2 40-Gigabit and 100-Gigabit Ethernet test modules are the world's first IP network traffic generation and layer 2-7 measurement and analysis test solution. K2 load modules are engineered to meet the needs of product teams developing 40 Gb/s and 100 Gb/s network devices such as routers, switches, and communications devices. K2 modules can measure and analyze the performance of Higher Speed Ethernet (HSE) standard-compliant devices at line rate, and are compatible with Ixia's chassis and broad range of 10 Mbps, 100 Mbps, 1 Gbps, and 10 Gbps interfaces, allowing real-world, full product testing in a single box.

Ixia's 40 Gb/s and 100 Gb/s load modules provide network device developers the ability to test 40 GE and 100 GE hardware electronics at full line-rate operation. Early adopters of the HSE technology can use the Ixia test system to validate their compliance with the new PCS lane operation of the IEEE P802.3ba draft standard.

Ixia's K2 load modules are valuable to developers who are integrating firmware and software into new electronics hardware, or integrating optical transceivers into their network devices and systems. Ixia's HSE modules can be used to validate and benchmark the performance limits of these network devices by employing layer 2 and 3 stress testing, virtual scalability testing, and negative testing. Ixia's HSE load modules ensure that a network device is ready to interoperate with other manufacturers' devices that claim compliance to the IEEE P802.3ba draft standard, and facilitate interoperability testing between different vendors of network devices and equipment.

Figure 19-1. 100GE and 40GE LSM XMV Load Modules

Figure 19-2. 40GE LSM XMV QSFP Load Module

Key Features

Industry's first 40 Gb/s and 100 Gb/s Layer 2 through 7 IP test solutions:

- 6 ports per XM12 chassis (10 rack mount units)

  Compatible with XM12 (941-0002) and XM12 High Performance chassis (941-0009)

- 1 port per XM2 (941-0003) desktop chassis

Industry's first commercially available 100 Gb/s Physical Coding Sublayer (PCS) test system:

Provides the ability to check compliance to the IEEE P802.3ba draft standard for both Transmit and Receive sides

Generates and analyzes full 40 Gb/s and 100 Gb/s line rate traffic:

- Tracks and analyzes up to 1 million flows per port for;

- Real-time latency
- Inter-arrival time
- Packet loss
- Data integrity
- Sequence checking
- Packet capture

Ixia's 40 Gb/s and 100 Gb/s load modules are designed for comprehensive layer 2-7 testing with integrated data plane and control plane traffic generation and analysis.

Nomenclature

The LSM HSE family identifying numbers are shown in *Table 19-1*.

Table 19-1. LSM HSE Modules

Load Module	Model Number	Description
40GE LSM XMV1	HSE40GETSP1-01	1-port 40GE, 2-slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications (requires 40GE CFP MSA transceiver).
100GE LSM XMV1	HSE100GETSP1-01	1-port 100GE, 2-slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications (requires 100GE CFP MSA transceiver).
40/100GE LSM XMV	HSE40/ 100GETSP1-01	1-port, 2-slot, dual-speed, full-featured load module with CFP interface
40GE LSM XMV QSFP	HSE40GEQSFP1-01	1-port, 1-slot, full-featured load module with QSFP interface

Specification are given in Table 19-2..

Table 19-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Number of ports per module	1	1
Number of chassis slots per module	2	1
Maximum ports per chassis	XM12: 6 XM12 High Performance: 6 XM2: 1	
Supported transceivers	CFP MSA Pluggable	QSFP Pluggable

Table 19-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Data Rate	40 Gbps 100 Gbps	40 Gbps
Port CPU Speed and memory	1GHz/2 GB	1GHz/2 GB
Per-port Capture buffer	1.4 GB	700 MB
Interface protocol	40 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 100GBASE-R 100 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 40GBASE-R	40 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 100GBASE-R
Ambient Operating Temp. Range	41°F to 95°F (5°C to 35°C) **Note**: Ambient air temperature at the installation site for the system should not exceed 95°F (35°C).	41°F to 95°F (5°C to 35°C) **Note**: Ambient air temperature at the installation site for the system should not exceed 95°F (35°C).
Layer 2/3 routing protocol emulation	Yes	
Layer 4-7 application traffic testing	Yes	
Number of transmit flows per port (sequential)	Billions	
Number of transmit flows per port (arbitrary values)	1 million	
Number of trackable receive flows	1 million	
Captured packet size	49-14,000 bytes	49-14,000 bytes
Number of stream definitions per port	256 In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows. **Note**: In the Data Center mode, the number of transmit streams is 256.	256
Preamble size	8 bytes	8 bytes
Frame size: min-max (bytes)	49-14,000	49-14,000
Inter-frame gap: min-max	1.8ns - 21.99sec	1.8ns - 21.99sec
Inter-burst gap: min-max	1.8ns - 21.99sec	1.8ns - 21.99sec
Inter-stream gap: min-max	1.8ns - 21.99sec	1.8ns - 21.99sec
Normal stream frame rate	0.045 fps - full line rate	0.045 fps - full line rate

Table 19-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	**HSE40GEQSFP1**
Advanced stream min frame rate	0.091fps	0.091fps
Latency[1]	20 nanosecond resolution	20 nanosecond resolution
Table UDF Entries	1million Comprehensive packet editing function for emulating large numbers of sophisticated flows. Entries of up to 256 bytes, using lists of values, can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size, and a list of values in a table format.	1 million
Max Value List UDF entries	1 million entries for 32-bit and 24-bit, 2 million entries for 8 and 16-bit.	1 million entries for 32-bit and 24-bit, 2 million entries for 8 and 16-bit.
Max Range List UDF entries	N/A	N/A
Packet flow statistics	Track over 1 million flows	
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, data integrity, and sequence checking	
User defined field features	Fixed, increment, or decrement by user-defined step, value lists, range lists, cascade, random, and chained	
Filters	48-bit source/destination address, 2x128-bit user definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)	
Data field per stream	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained	

Table 19-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/ received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), user-defined stat 5, user-defined stat 6, 8 QoS counters, data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies	
Error generation	CRC (good/bad/none), undersize, oversize	
MDIO	Ability to calibrate and remove inherent latency from any MSAcompliant 40 Gb/s or 100Gb/s CFP transceiver	
Transmit line clock adjustment	Ability to adjust the parts per million (ppm) line frequency over a range of LAN mode: - 100 to +100 ppm	
Clock In/Out	The load module provides two female SMA coaxial connectors—one for clock input and one for clock output—to allow the device under test (DUT) to frequency-lock with the load module interface. See *Clock In/Out* on page 19-8.	

Table 19-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Layer 1 BERT capability	The load module supports the following BERT features on both 40 Gb/s and 100 Gb/s speeds: • User selected PRBS pattern for each PCS Lane • User selects from a wide range of PRBS data patterns to be transmitted (true and complement) • Send single, continuous, and exponentially controlled amounts of error injection • Wide range of statistics, including: Pattern Lock, Pattern Transmitted, Pattern Received, Total Number of Bits Sent and Received, Total Number of Errors Sent and Received, Bit Error Ratio (BER), Number of Mismatched 1's and 0's. • Lane Stats Grouping per lambda for SMF and MMF 40 Gb/s and 100 Gb/s based on IEEE802.3ba defined physical medium dependent (PMD).	
Physical Coding Sublayer (PCS) test features	IEEE P802.3ba compliant PCS transmit and receive side test capabilities.	
Per PCS lane, transmit lane mapping	Supports all combination of PCS lane mapping: Default, Increment, Decrement, Random, and Custom.	
Per PCS lane, skew insertion and deskew capability	User selectable from zero up to 3 microseconds of skew insertion on transmit side. Ability to measure deskew up to 6 microseconds on receive side.	
IPv4, IPv6, UDP, TCP	Hardware checksum generation, and verification.	
Frame length controls	Fixed, random, weighted random, or increment by user-defined step, random, weighted random.	
Preamble view	Allows to select to view the preamble in Packet View.	
Link Fault Signaling	Ability to select the option to have the transmit port ignore link faults from a remote link partner.	

1. Cancel Intrinsic Latency feature measures and/or removes the latency induced by the test equipment (not the DUT). See *Intrinsic Latency Adjustment* on page 19-9.

Port LEDs

Each 40/100GE port incorporates a set of LEDs, as described in the following tables.

Table 19-3. 40/100GE LSM Port LEDs

LED Label	Usage
Link	Green if Ethernet link is up (established) or the port is in a forced Link Up state, red if link is down. Link may be down due to no signal or no PCS lock.
Tx Active	Green indicates that Tx is active and frames being sent; red indicates Tx is paused; off indicates Tx is not active.
Rx Active	Green indicates that Rx is active and frames being received; red indicates Rx is paused; off indicates Rx is not active.
Rx/Error	Green indicates valid Rx frames are being received; red indicates error frames being received; off indicates no frames being received.
Attention	(Reserved for future use)
Pwr Good	Green when power is on, red if power fault occurs.

Clock In/Out

The load module provides coaxial connectors for clock input and clock output to allow the DUT to frequency-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in Table 19-4 to ensure proper performance of the load module.

The clock in/out electrical interface parameters are also defined in Table 19-4.

Table 19-4. Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
Clock Input	Frequency	161.13 MHz ±100ppm
	Duty cycle	50%
	Jitter	±150ps max. cycle to cycle, >1kHz
	Amplitude	Vpp = 4.0
	Impedance	50 ohm ± 5%, DC coupled
	Connector	Female SMA
Clock Output	Frequency	161.13 MHz +/-100ppm (Programmable ppm in Internal Clock Mode)
	Duty cycle	40 to 60%
	Jitter	20ps max cycle to cycle, >1kHz

Table 19-4. Clock In/Out Electrical Interface Parameters

Parameter	Characteristic
Amplitude	0.7Vpp min into 50 ohms, AC coupled output
Edge rates	200ps to 340ps (20% to 80%) into 50 ohms
Impedance	50 ohms +/-5%, AC coupled
Connector	Female SMA

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

Statistics

Statistics for 40/100GE LSM cards, under various modes of operation may be found in Table B-36 on page B-164.

Intrinsic Latency Adjustment

This option, when present and enabled, reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). For a specific transceiver, the system retrieves its pre-determined latency value and subtracts this from the measured overall latency. For an ‘unknown’ transceiver (not previously measured), it calculates and stores the intrinsic latency value.

On the **General** tab in **Port Properties**, the **Latency Calibration** option is only enabled for cards with transceivers that have not been pre-measured for intrinisic latency by Ixia. The **Latency Calibration** option is grayed-out if any one of the following conditions are present:

- there is no transceiver
- the transceiver is CFP and a value is found for it in the list of precalibrated values

The **Latency Calibration** option is enabled if the transceiver is CFP but no pre-calibrated value is found in the stored list. The **Latency Calibration** option is also enabled for transceivers that you have previously calibrated, so that the calibration measurement may be repeated (if desired).

Clicking the **Latency Calibration** option runs a Tcl script that measures intrinsic latency and stores the value in an .xml file. The .xml file contains the values that you have produced and saved. Each value is identified for a specific transceiver (per manufacturer, model, and serial number). You can run the calibrate process repeatedly with the same transceiver (if desired). Each new measurement overwrites the previous one for that transceiver.

Running the calibration measurement puts the port into a special loopback mode to measure intrinsic latency. When done, the port is put back into default normal mode. Any port configuration you have set before calibrating intrinsic latency, is lost as the port reverts to a default configuration.

The **Enable** check box is grayed out when no value exists in the system for the specific transceiver. If a value exists in the .xml file, then the **Enable** check box is available. Select the check box to enable the intrinsic latency adjustment.

After the intrinsic latency adjustment has been done, you may want to refresh the chassis or close and reopen the Port Properties dialog.

Multilane Distribution Configuration

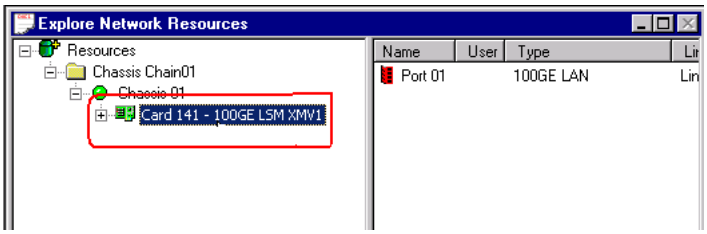
The Tx Lane tab allows to control the PCS (Physical Coding Sublayer) lane configuration and skew. It is part of the Port Properties for the module.

Note: The other tabs in the Port Properties page are described in the *IxExplorer User Guide*, as are the rest of the controls for the module.

To open the Tx Lane tab:

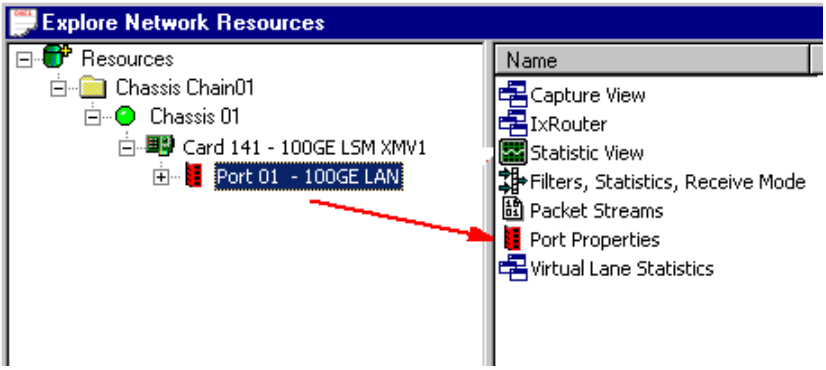
1. Select the 40 or 100GE LSM XMV1 module in the left pane of the IxExplorer window as shown in Figure 19-3.

Figure 19-3. Select Module



2. Expand the node, and select the Port object. In the right window pane, double-click the Port Properties object as shown in Figure 19-4.

Figure 19-4. Port and Port Properties



3. In the Port Properties dialog, select the Tx Lane tab. Use this tab to control the PCS lane order and the skew for each lane.

The Tx Lane tab is shown in Figure 19-5.

Figure 19-5. Tx Lane Tab

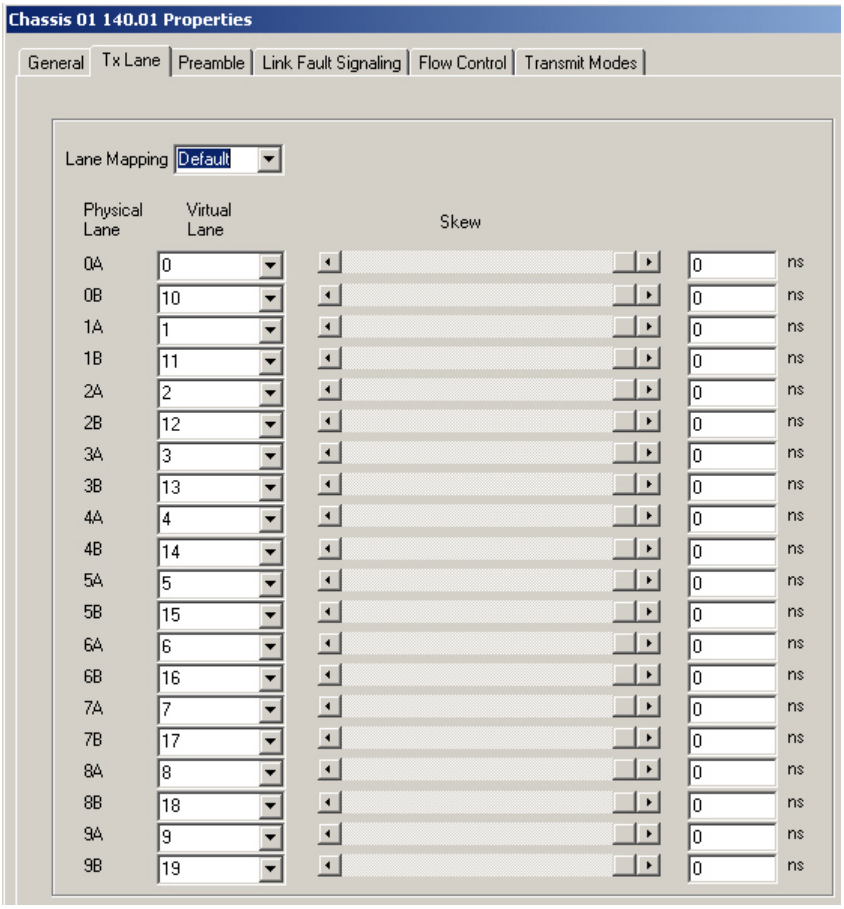


Table 19-5 explains the options in the Tx Lane tab page.

Table 19-5. Tx Lane Tab Configuration

Field	Description
Lane Mapping	Allows you to select a PCS lane ordering method. There are four options: • Default: The default ordering method. The default order is each physical port corresponds to 2 PCS lanes that are n and n+10, where n = physical lane number. • Increment: Orders the lanes from 0 to 19, straight down the list. • Decrement: Orders the lanes from 19 to 0, straight down the list. • Custom: Allows to put the lanes in any order by manually entering the numbers in the fields. The starting order is the last selected mapping.
Physical Lane	The physical lane identifier. The physical lane is paired with a corresponding PCS lane.

Table 19-5. Tx Lane Tab Configuration

Field	Description
PCS Lane	A number identifier for the PCS lane. The PCS lane is paired with a corresponding physical lane.
Skew	The skew slider is used to set a skew value for the PCS lane, in nanoseconds, on the transmit side. Lane Skew is the ability to independently delay one or more of the 20 PCS lanes. When the slider is moved, the nanoseconds field is correspondingly adjusted. You can also enter a nano second value directly into this field. When the slider is fully pushed to the right, the skew injected into the transmit stream is 0 (minimum). When the slider is pushed all the way to the left. the skew injected into the transmit stream is 3 uS (maximum).

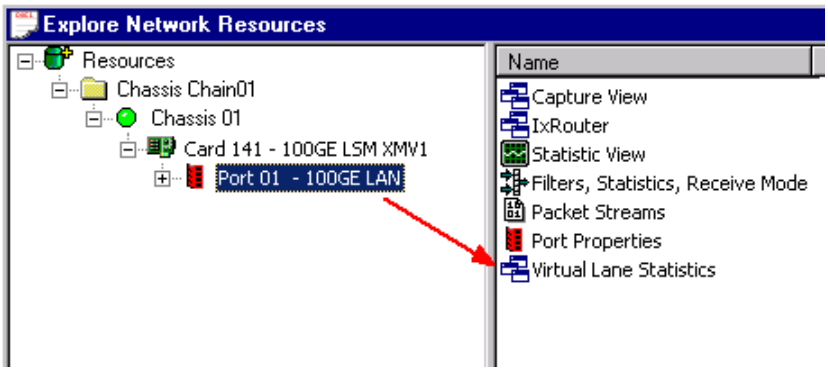
PCS Lane Statistics

The PCS lane statistics table allows to view the statistics for the configured PCS lanes.

To open the PCS lane statistics table:

1. Select the 40 or 100GE LSM XMV1 module in the left pane of the IxExplorer window as shown in Figure 19-3.
2. Expand the node, and select the Port object. In the right window pane, double-click the PCS lane statistics object as shown in Figure 19-6.

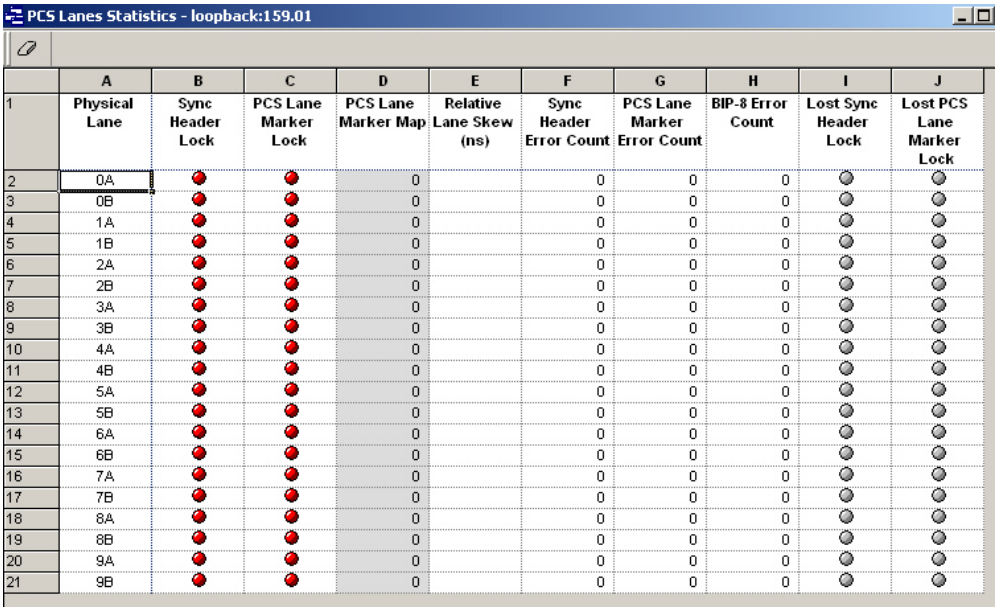
Figure 19-6. Port and PCS Lane Statistics



3. The PCS lane statistics table opens. Use this table to view the PCS lane statistics for each lane. The statistics are for the **receive** side.

The PCS lane statistics table is shown in Figure 19-7.

Figure 19-7. PCS Lane Statistics Table



	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0		0	0	0		
3	0B			0		0	0	0		
4	1A			0		0	0	0		
5	1B			0		0	0	0		
6	2A			0		0	0	0		
7	2B			0		0	0	0		
8	3A			0		0	0	0		
9	3B			0		0	0	0		
10	4A			0		0	0	0		
11	4B			0		0	0	0		
12	5A			0		0	0	0		
13	5B			0		0	0	0		
14	6A			0		0	0	0		
15	6B			0		0	0	0		
16	7A			0		0	0	0		
17	7B			0		0	0	0		
18	8A			0		0	0	0		
19	8B			0		0	0	0		
20	9A			0		0	0	0		
21	9B			0		0	0	0		

Table 19-6 explains the entries in the PCS lane statistics table.

Table 19-6. PCS Lane Statistics Data

Field	Description
Physical Lane	The identifier for the Receive physical lane. This is a tag/ fixed label to ID each lane.
Sync Header Lock	Indicates if the received PCS lane achieved sync-bit lock. Green indicates success, red failure.
PCS Lane Marker Lock	Indicates if the received PCS lane has achieved alignment marker lock. Green indicates success, red failure.
PCS Lane Marker Map	The PCS lane number identified by the alignment marker. This is only valid when PCS Lane Marker Lock is green.
Relative Lane Skew (ns)	Shows the actual skew in nanoseconds. Skew measurements are valid only when all lanes are locked with 20 unique lane markers. The first PCS Lane markers to arrive have skew of 0. All other lane skews are relative to them.
Sync Header Error Count	The number of synchronization bit errors received.
PCS Lane Marker Error Count	The number of incorrect PCS lane markers received while in PCS lane lock state.
BIP-8 Error Count	Bit interleaved parity error count. It detects the number of BIP-8 errors for a PCS lane.

Table 19-6. PCS Lane Statistics Data

Field	Description
Lost Sync Header Lock	When lit, indicates the loss of sync header lock since the last statistic was read. If colored gray, there is no error. If colored red, an error has occurred.
Lost PCS Lane Marker Lock	When lit, indicates the loss of PCS lane marker lock since the last statistic was read. If colored gray, there is no error. If colored red, an error has occurred.

20 IXIA 10 Gigabit Ethernet Load Modules

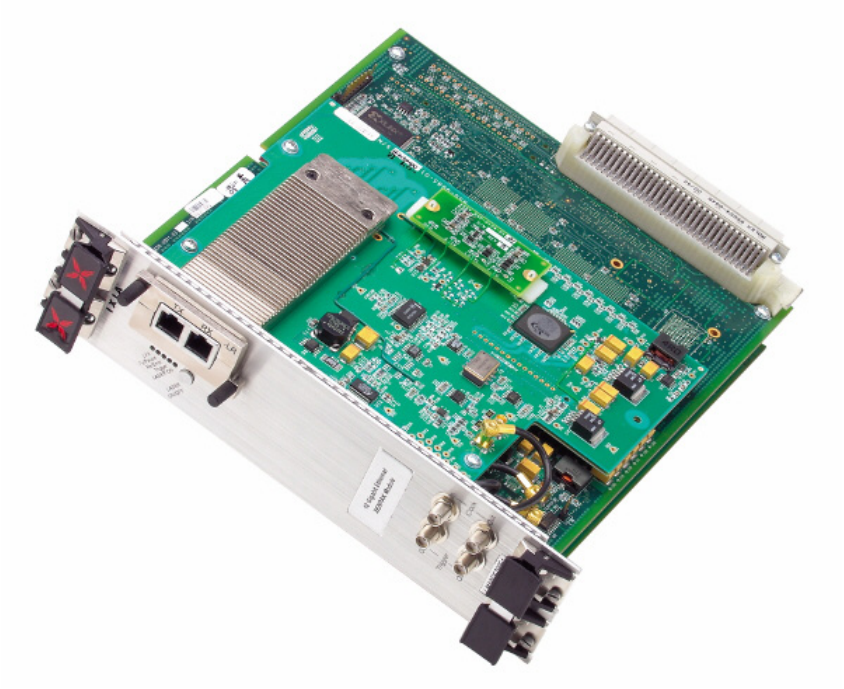
This chapter provides details about 10 Gigabit Ethernet (10GE) family of load modules—the specifications and features.

The 10 Gigabit Ethernet (10GE) family of load modules implements five of the seven IEEE 8.2.3ae compliant interfaces that run at 10Gbit/second. Cards are available which offer the following interfaces:

- 10GE LAN
- 10GE WAN
- XAUI
- XENPAK - with options for XPAK or X2 transceiver use.

Figure 20-1 on page 20-2 shows an LM10GEXENPAK module.

Figure 20-1. LM10GEXENPAK



In addition, two families of multimode card are available which offers combined 10GE LAN/WAN, OC192 POS, BERT, and FEC functionality. The features available for these load modules are described in Chapter 21, *IXIA 10GE LAN/WAN and OC 192 POS Load Modules*.

The full details for these families may be found at:

- *LSM 10GE Family* on page 20-2
- *10GE LAN Family* on page 20-21.
- *XAUI Family* on page 20-24
- *XENPAK Family* on page 20-29

LSM 10GE Family

The Ixia 10 Gigabit Ethernet LAN Service Module (LSM) offers unprecedented scalability, performance, and service testing flexibility. The Ixia 10GE LSM is Ixia's third-generation 10 Gigabit Ethernet solution. It is the industry's first six-port solution, and it offers a broad portfolio of edge/core testing solutions for the most demanding test environments including performance, scalability, and conformance testing of Layer 2-3, Routing Protocols, and high performance Layer 4-7 testing. It supports IPv4 and IPv6 wire-speed traffic generation, advanced analysis and IPv4 and IPv6 routing protocol emulation.

The Ixia 10GE LSM supports a comprehensive portfolio of service testing solutions for the next-generation service provider networks including Metro

Ethernet E-LAN and E-LINE services; and MPLS VPNs such as Layer 2 VPNs, Layer 3 RFC 2547 VPNs, and VPLS.

Figure 20-2. LSM10GXM8-01 NGY Load Module

Figure 20-3. LSM10GXL6-01 Load Module

Figure 20-4. LSM10GXM3-01 Load Module

Figure 20-5. LSM10GL1-01(XENPAK Carrier Card)

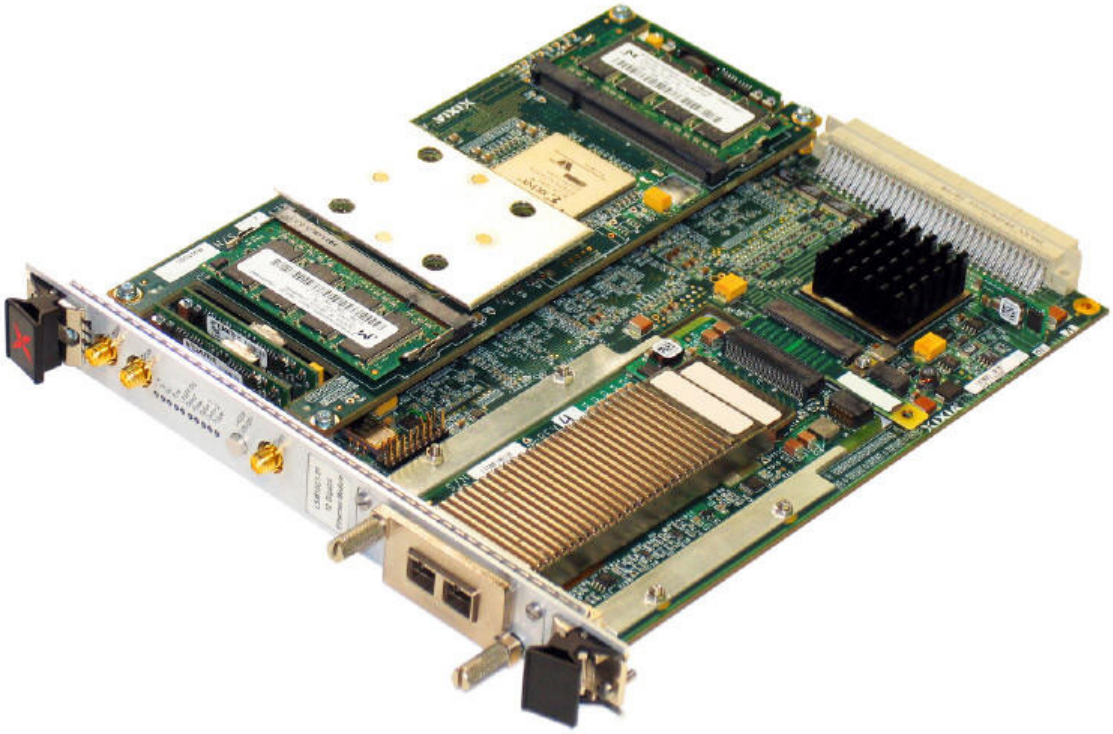
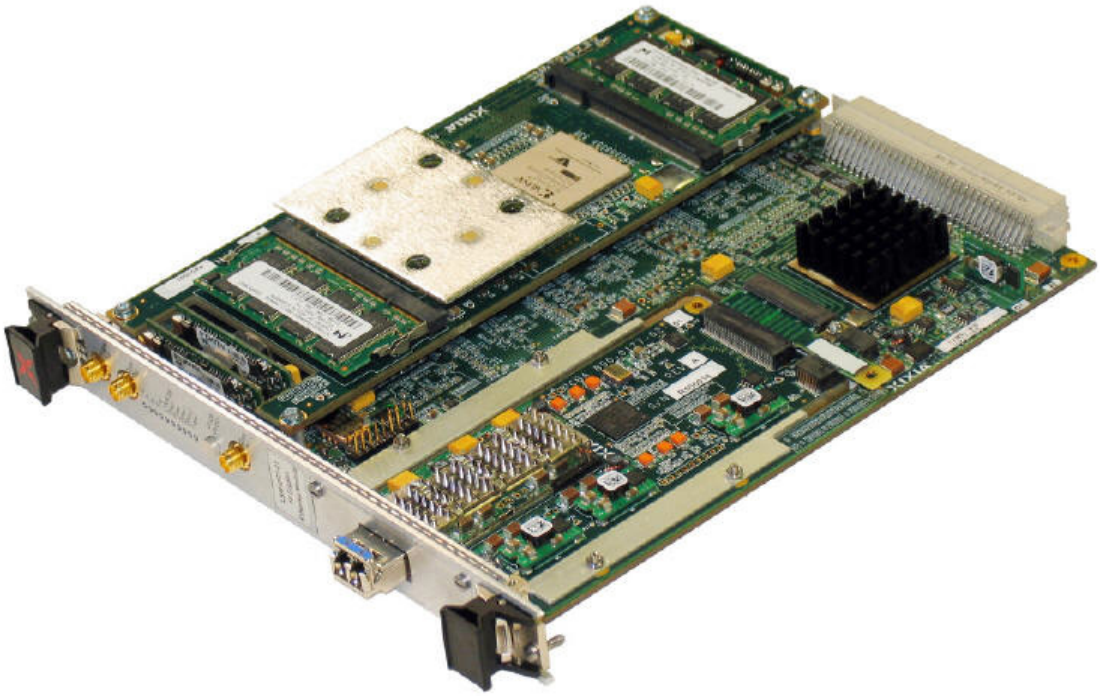


Figure 20-6. LSM10GMS-01(MACsec Carrier Card)

Figure 20-7. LSM10GL1-01 (XFP Carrier Card)



Part Numbers

The LSM family part numbers are shown in *Table 20-1*.

Table 20-1. 10GE LSM modules

Load Module	Part Number	Description
10GE LSM	LSM10G1-01	1-port 10GE, single slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications (requires XENPAK or XFP adapter and matching transceiver).
10GE LSM LAN XFP	LSM10GL1-01	1-port, single slot, L2/L3 only, does not support routing protocols and L4-7 applications (requires XENPAK or XFP adapter and matching transceiver).
10GE LSM MACSec	LSM10GMS-01	1-port 10GE, single slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications. Supports MACSec functionality for stream generated traffic. XFP LAN/WAN carrier card is integrated.
10GE LSM XL6	LSM10GXL6-01, -02	6-port 10GE, single slot, full featured LAN load module for Optixia XL10. Supports routing protocols, Linux SDK, and L4-7 applications (does not include XFP transceivers).
10GE LSM XM3	LSM10GXM3-01	3-Port 10GE, single slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications.
10GE LSM XMR3	LSM10GXMR3-01	3-Port 10GE, single slot, reduced-featured load module. Supports Linux SDK and L4-7 applications.
10GE LSM XM8	LSM10GXM8-01	NGY 8-port 10GE, single slot, full-featured load module 800MHz, 512MB. Full L2/7 support. Linux SDK, and L4-7 applications.
10GE LSM XMR8 10GE LSM XMR8 10GBASE-T	LSM10GXMR8-01 LSM10GXMR8GBT-01	NGY 8-port 10GE, 400MHz, 128MB single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version.
10GE LSM XM8XP 10GE LSM XM8 10GBASE-T	LSM10GXM8XP-01 LSM10GXM8GBT-01	NGY 8-port 10GE, 800MHz, 1GB, Extra Performance. Includes 10GBASE-T version.
10GE LSM XM8S	LSM10GXM8S-01	NGY 8-port 10GE, LAN/WAN, SFP+ interface with 1GB RAM per port; for OPTIXIA XM12-02 and OPTIXIA XM2-02 chassis; full L2/7 support. Requires one or more SFP+ transceiver options: 10GBASE-SR, 10GBASE-LR, 10GBASE-LRM, or 10GSFP+Cu.

Table 20-1. 10GE LSM modules

Load Module	Part Number	Description
10GE LSM XMR8S	LSM10GXMR8S-01	Same as 10GE LSM XM8S but reduced L2/3 support with limited L3 routing.
NGY-NP8-01	NGY-NP8-01	10 Gigabit Application Network Processor Load Module, 8-Port LAN/WAN, SFP+ interface.
10GE LSM XM4	LSM10GXM4-01	NGY 4-port 10GE, single slot, full-featured load module 800MHz, 512MB. Full L2/7 support. Linux SDK, and L4-7 applications.
10GE LSM XMR4 10GE LSM XMR4 10GBASE-T	LSM10GXMR4-01 LSM10GXMR4GBT-01	NGY 4-port 10GE, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version.
10GE LSM XM4XP 10GE LSM XM4 10GBASE-T	LSM10GXM4XP-01 LSM10GXM4GBT-01	NGY 4-port 10GE, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version.
10GE LSM XM4S	LSM10GXM4S-01	NGY 4-port 10GE, LAN/WAN, SFP+ interface with 1GB RAM per port; for OPTIXIA XM12-02 and OPTIXIA XM2-02 chassis; full L2/7 support. Requires one or more SFP+ transceiver options: 10GBASE-SR, 10GBASE-LR, 10GBASE-LRM, or 10GSFP+Cu.
10GE LSM XMR4S	LSM10GXMR4S-01	Same as 10GE LSM XM4S but reduced L2/3 support with limited L3 routing.
NGY-NP4-01	NGY-NP4-01	10 Gigabit Application Network Processor Load Module, 4-Port LAN/WAN, SFP+ interface.
10GE LSM XM2XP 10GE LSM XM2 10GBASE-T	LSM10GXM2XP-01 LSM10GXM2GBT-01	NGY 2-port 10GE, 1GHz, 1GB, Extra Performance. Includes 10GBASE-T version.
10GE LSM XMR2 10GE LSM XMR2 10GBASE-T	LSM10GXMR2-01 LSM10GXMR2GBT-01	NGY 2-port 10GE, 400MHz, 128MB, single slot, reduced L2/3 support with limited L3 routing, Linux SDK, and L4-7 applications. Includes 10GBASE-T version.
10GE LSM XM2S	LSM10GXM2S-01	NGY 2-port 10GE, LAN/WAN, SFP+ interface with 1GB RAM per port; for OPTIXIA XM12-02 and OPTIXIA XM2-02 chassis; full L2/7 support. Requires one or more SFP+ transceivers: 10GBASE-SR, 10GBASE-LR, 10GBASE-LRM, or 10GSFP+Cu.
10GE LSM XMR2S	LSM10GXMR2S-01	Same as 10GE LSM XM2S but reduced L2/3 support with limited L3 routing.

Table 20-1. 10GE LSM modules

Load Module	Part Number	Description
NGY-NP2-01	NGY-NP2-01	10 Gigabit Application Network Processor Load Module, 2-Port LAN/WAN, SFP+ interface.
XENPAK-ADAP-01	948-0007	XENPAK LAN Adapter for LSM10Gx1-xx.
XFP-ADAP-02	948-0002	LAN/WAN Adapter for LSM10Gx1-xx
X2-ADAP-01	948-0008	X2 Carrier
10GBASET-ADAP-01	948-0009	10GBase-T Adapter for LSM10Gx1-xx
SFP-ADAP-01	948-0012	SFP+ Adapter for LSM10G1 and LSMGL1, must be used with an SFP+ transceiver.
SFP+ transceiver 10GBASE-SR	948-0013	10GBASE-SR Accessory, SFP+ Transceiver for 10GE LAN/WAN load modules with pluggable SFP interface, 850nm.
SFP+ transceiver 10GBASE-LR	948-0014	10GBASE-LR Accessory, SFP+ Transceiver for 10GE LAN/WAN load modules with pluggable SFP interface, 1310nm.
SFP+ transceiver 10GBASE-LRM	948-0015	10GBASE-LRM Accessory, SFP+ Transceiver for 10GE LAN load modules with pluggable SFP+ interface, 1300nm, MMF. **Note**: LAN mode is not supported.
SFP+ transceiver 10GSFP+Cu	948-0016	10GSFP+Cu Accessory, Direct Attach Cable Transceiver for 10GE LAN/WAN load modules with pluggable SFP+ interface, Copper Wire, 3 meter length.
10GE LSM XM8NGY	944-1070-01	LSM10GXM8NG-01 10 Gigabit Ethernet Load Module, 8-Port LAN/WAN, XFP interface
10GE LSM XM4NGY	944-1071-01	LSM10GXM4NG-01 10 Gigabit Ethernet Load Module, 4-Port LAN/WAN, XFP
10GE LSM XM2NGY	944-1096-01	LSM10GXM2NG 10 GIGABIT ETHERNET LOAD MODULE, 2-Port LAN/WAN, XFP

Table 20-2. 10GE LSM Load Module Specifications (except NGY)

	LSM10G1-01 LSM10GL1-01[1]	**LSM10GMS-01**	**LSM10GXL6-01, -02**	**LSM10GXM3-01 LSM10GXMR3-01[2]**
# ports	1	1	6	3
Data Rate	10GB	10GB	10GB	10GB

Table 20-2. 10GE LSM Load Module Specifications (except NGY)

	LSM10G1-01 LSM10GL1-01[1]	LSM10GMS-01	LSM10GXL6-01, -02	LSM10GXM3-01 LSM10GXMR3-01[2]
Port CPU Speed	1GHz (G1) 500MHz (GL1)	1GHz	1GHz	
Port CPU Memory	512MB (G1) 128MB (GL1)	512MB	512MB	512 MB (GXM) 128 MB (GXMR)
Connector/ Frequency-Mode	XFP or XENPAK/ X2. See *XENPAK Connectors* on page 20-33 10GBase-T Adapter, see *Removable Carrier Cards* on page 20-15 Also XFP-CX4 and SFP-CX4	Integrated XFP LAN/WAN carrier card Also XFP-CX4	XFP	XFP XFP-CX4
Ambient Operating Temp. Range	41°F to 95°F (5°C to 35°C)	41°F to 95°F (5°C to 35°C)	41°F to 95°F (5°C to 35°C)	41°F to 95°F (5°C to 35°C)
Capture buffer size	Up to 384 MB	Up to 384 MB	Up to 384 MB	GXM3: 350 MB GXMR3: 32 MB
Captured packet size	17-65,535 bytes	17-65,535 bytes	17-65,535 bytes	17-65,535 bytes
Streams per port	256	256	256	256
Advanced streams	256	256	256	256
Preamble size: min-max	8	8	8	8
p: min-max (bytes)	17-65,535	17-65,535	17-65,535	17-65,535
Inter-frame gap: min-max[3]	4.0ns - 42sec in 3.2ns steps	4.0ns - 42sec in 3.2ns steps	4.0ns - 42sec in 3.2ns steps	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min-max	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps
Inter-stream gap: min-max	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate	0.023fps - full line rate	0.023fps - full line rate	0.023fps - full line rate
Advanced stream min frame rate[4]	Slow: 0.023fps Fast: 1525fps	Slow: 0.023fps Fast: 1525fps	Slow: 0.023fps Fast: 1525fps	Slow: 0.023fps Fast: 1525fps

Table 20-2. 10GE LSM Load Module Specifications (except NGY)

	LSM10G1-01 LSM10GL1-01[1]	LSM10GMS-01	LSM10GXL6-01, -02	LSM10GXM3-01 LSM10GXMR3-01[2]
Latency[5]	20ns resolution	20ns resolution The 'No CRC' option is not supported.	20ns resolution	20ns resolution
Table UDF Entries	1M (full) 32K (reduced)	1M	1M	1M (GXM3) 32K (GXMR3)
Max Value List UDF entries	G1: 512K entries GL1: 8K entries	512K entries	512K entries	GXM3-01: 512K entries GXMR3-01: 8K entries
Max Range List UDF entries	G1: 256 entries GL1: 16 entries			GXM3-01: 256 entries GXMR3-01: 16 entries

1. Applications are not supported on LSM10GL1-01 (no Layer 4-5 support).
2. The LSM10GMXR3-01 only supports IxNetwork, IxAutomate, and IxExplorer.
3. Packet gap size also depends on the stream mode selected—Fixed or Average.
4. Streams are divided up into two categories: 224 slow speed streams and 32 fast streams.
5. Cancel Intrinsic Latency feature measures and/or removes the latency induced by the test equipment (not the DUT). See *Intrinsic Latency Adjustment* on page 20-20.

.

Table 20-3. NGY Load Module Specifications

Feature	Extra Performance	Full Performance	Reduced Performance
Load Modules	LSM10GXM8XP	LSM10GXM8	LSM10GXMR8
	LSM10GXM4XP	LSM10GXM4	LSM10GXMR4
	LSM10GXM2XP		LSM10GXMR2
	LSM10GXM8S		LSM10GXMR8S
	LSM10GXM4S		LSM10GXMR4S
	LSM10GXM2S		LSM10GXMR2S
	LSM10GXM8GBT		LSM10GXMR8GBT
	LSM10GXM4GBT		LSM10GXMR4GBT
	LSM10GXM2GBT		LSM10GXMR2GBT
Number of ports per module	8/4/2	8/4	8/4/2
Line rate	10 Gb/s	10 Gb/s	10 Gb/s
Number of chassis slots per module	1	1	1
Maximum ports per chassis			

Table 20-3. NGY Load Module Specifications

Feature	Extra Performance	Full Performance	Reduced Performance
XM12 High Performance	96/48/24[1]	96/48[1]	96/48/24[1]
XM2 Desktop	16/12[1]/8/4	16/8	16/8/4
Supported transceivers (optical and copper) **Note**: The NGY family of load modules can support transceivers that use up to 2.5W of power. Do not use transceivers beyond 2.5W.	XFP, SFP+, RJ-45 10GBASE-T	XFP	XFP, SFP+, RJ-45 10GBASE-T
Per-port CPU speed and memory	1 GHz, 1 GB[2]	800 MHz/512 MB	400 MHz/128 MB
Per-port capture buffer	512 MB	512 MB	64 MB
Captured packet size	17 bytes—absolute minimum frame size 64 bytes—minimum frame size at line rate		
Interface protocols	10 GE LAN/WAN	10 GE LAN/WAN	10 GE LAN/WAN
Layer 2/3 routing protocol emulation	Yes	Yes	Yes
Layer 4-7 application traffic testing	Yes	Yes	No
Number of transmit flows per port (sequential values)	Billions	Billions	Billions
Number of transmit flow per port (arbitrary values)	1 million	1 million	32 K
Number of trackable receive flows	1 million	1 million	64K
Number of stream definitions per port	512	512	512
	In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows.		
Preamble size: min-max	8	8	8
p: min-max (bytes)	48-16,000	48-16,000	48-16,000
Inter-frame gap: min-max	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps
Inter-burst gap: min-max	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps

Table 20-3. NGY Load Module Specifications

Feature	Extra Performance	Full Performance	Reduced Performance
Inter-stream gap: min-max	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps	3.2ns - 27.48sec in 3.2ns steps
Normal stream frame rate	0.023fps - full line rate	0.023fps - full line rate	0.023fps - full line rate
Advanced stream min. frame rate	Slow: 0.023fps Fast: 1525fps	Slow: 0.023fps Fast: 1525fps	Slow: 0.023fps Fast: 1525fps
Number of streams in Packet Stream Mode (Non Data Center Mode)	512	512	512
Number of streams in Advanced Scheduler Mode (Non Data Center Mode)	Fast: 32 Slow: 480	Fast: 32 Slow: 480	Fast: 32 Slow: 480
Number of streams in Advanced Scheduler Mode (Data Center Mode)	Fast: 32 Slow: 224	Fast: 32 Slow: 224	Fast: 32 Slow: 224
Table UDF	1 million entries	1 million entries	32 K
	Comprehensive packet editing function for emulating large numbers of sophisticated flows. Entries of up to 256 bytes, using lists of values can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size and a list of values in a table format.		
Max Value List UDF entries	512K entries for 32-bit and 24-bit, 1M entries for 8 and 16-bit.	512K entries for 32-bit and 24-bit, 1M entries for 8 and 16-bit.	256K entries for 32-bit and 24-bit, 512K entries for 8 and 16-bit.
Max Range List UDF entries	512 entries	512 entries	256 entries
Packet flow statistics	Track 1 million flows	Track 1 million flows	Track 64 K flows
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures		
Receive engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, data integrity, and sequence checking		
User defined field features	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained		
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)		
Data field per stream	Fixed, increment (byte/word), decrement (byte/word), random, repeating, user-specified		

Table 20-3. NGY Load Module Specifications

Feature	Extra Performance	Full Performance	Reduced Performance
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/ received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), user-defined stat 5, user-defined stat 6, 8 QoS counters, data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies		
Error generation	CRC (good/bad/none), undersize, oversize		
Latency measurements	20 ns resolution in packet timestamp		
Latency self-calibration	Ability to calibrate and remove inherent latency from any MSA-compliant 10GbE XFP transceivers, including unsupported transceivers		
Transmit line clock adjustment	Ability to adjust the parts per million (ppm) line frequency over a range of: • LAN mode: -105 to +105 ppm[3] • WAN mode: -30 to +30 ppm		
IPv4, IPv6, UDP, TCP	Hardware checksum generation and verification		
Frame length controls	Fixed, random, weighted random, or increment by user-defined step, random, weighted random		
Operating temp. range	41°F to 95°F (5°C to 35°C), ambient air[4]		

1. XM12 High Performance chassis (941-0009) is required for 80 or more ports of 10 GbE NGY XFP or SFP+ 8-port, load modules to be installed in a single chassis. A field replaceable power supply upgrade kit (943-0005) is available for the XM12 chassis (941-0002) to convert it to the high-performance version. Up to ten 8-port NGY 10GBASE-T full performance load modules are supported in an XM12 High Performance chassis, and up to eight 8-port NGY 10GBASE-T full performance load modules are supported in a standard XM12 chassis). The XM2 chassis (941-0003) supports up to twelve ports of 10GBASE-T full performance load modules.
2. The LSM10GXM8XP, LSM10GXM8S, and LSM10GXM8GBT use a high performance 800MHz processor with additional layer 2 cache.
3. For 10GBASE-T interfaces on NGY the ppm does change the data rate, but does not change the bit period due to phy chip limitations.
4. When an NGY load module is installed in an XM12 or XM2 chassis, the maximum operating temperature of the chassis is 35°C (ambient air).

Port LEDs

Note: The NGY 10GBASE-T load module has only 2 port LEDs:

- Rx/Error: Same as Rx/Error in the following table
- Tx/Link: Combines the Link and Tx/Pause functions. Solid green = link; blinking green = transmit; red = flow control.

Each 10GB port incorporates a set of LEDs, as described in the following figure.

Table 20-4. 10GE LSM Port LEDs

LED Label	Usage
Link	Green if Ethernet link is up (established) or the port is in a forced Link Up state, red if link is down. Link may be down due to no signal or no PCS lock.
Tx/Pause	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction. **Note**: For NGY load modules LSM10GXM(R)8 and LSM10GXM(R)4: green indicates that Tx is active and frames being sent; red indicates Tx is paused; off indicates Tx is not active.
Rx/Error	Green while data is received. Red on any Ethernet error. Off if no frames are received. **Note**: For NGY load modules LSM10GXM(R)8 and LSM10GXM(R)4: green indicates valid Rx frames are being received; red indicates error frames being received; off indicates no frames being received..
LASER ON	Green when the port's laser is turned on. Off otherwise.
Detect	Green when valid plug in module is detected, red otherwise.
Power	Green when power is on, red if power fault occurs.
Option1/2	N/A
Trigger	See *Trigger Out Values* on page 20-15.

Clock In/Out

The load module provides coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in the following figure to ensure proper performance of the load module.

The clock in/out electrical interface parameters are also defined in the following figure.

Table 20-5. Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
Clock Input	Frequency	156.25 MHz ±100ppm
	Duty cycle	50%
	Jitter	±150ps max. cycle to cycle, >1kHz
	Amplitude	Vpp = 4.0
	Impedance	50 ohm ± 5%, DC coupled

Table 20-5. Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
	Connector	Female SMA
Clock Output	Frequency	156.25MHz +/-105PPM (Programmable PPM in Internal Clock Mode) **LSM10GXM8-01** and variations: 156.25MHz (LAN) or 155.52MHz (WAN) +/-30PPM (Programmable PPM in Internal Clock Mode)
	Duty cycle	40 to 60%
	Jitter	20ps max cycle to cycle, >1kHz
	Amplitude	0.7Vpp min into 50 ohms, AC coupled output
	Edge rates	200ps to 340ps (20% to 80%) into 50 Ohms
	Impedance	50 ohms +/-5%, AC coupled
	Connector	Female SMA

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1 kHz.

Trigger Out Values

The signals and LEDs available on the trigger out pins for these cards are described in the following table.

Table 20-6. 10GE LAN Trigger Out Signals

Pin/LED	Value
Trigger Out	Single ended output that pulses high for approximately 1.18s shortly after the Central FPGA is loaded, and following an event defined by UDS1. Voltage output = 3.3V for high, 0V for low.
Trigger LED	Pulses following an event defined by UDS1.

Removable Carrier Cards

The 10GE10G1-01 and the LSM10GL1-01 load modules have removable carrier cards available for use:

- The XENPAK-ADAP-01 carrier card for XENPAK transceivers, shown in Figure 20-8 on page 20-16.
- The XFP-ADAP-01 LAN only carrier card for XFP transceivers (not shown).
- The XFP-ADAP-02 LAN/WAN carrier card for XFP transceivers (shown being inserted into the LSM load module in Figure 20-10 on page 20-17.
- X2 carrier card for X2 Transceiver (shown with transceiver installed in Figure 20-9 on page 20-16).

- 10GBase-T-ADAP-01 10 Gigabit Ethernet adapter module (shown in Figure 20-11 on page 20-18).

Figure 20-8. XENPAK-ADAP-01 Carrier Card

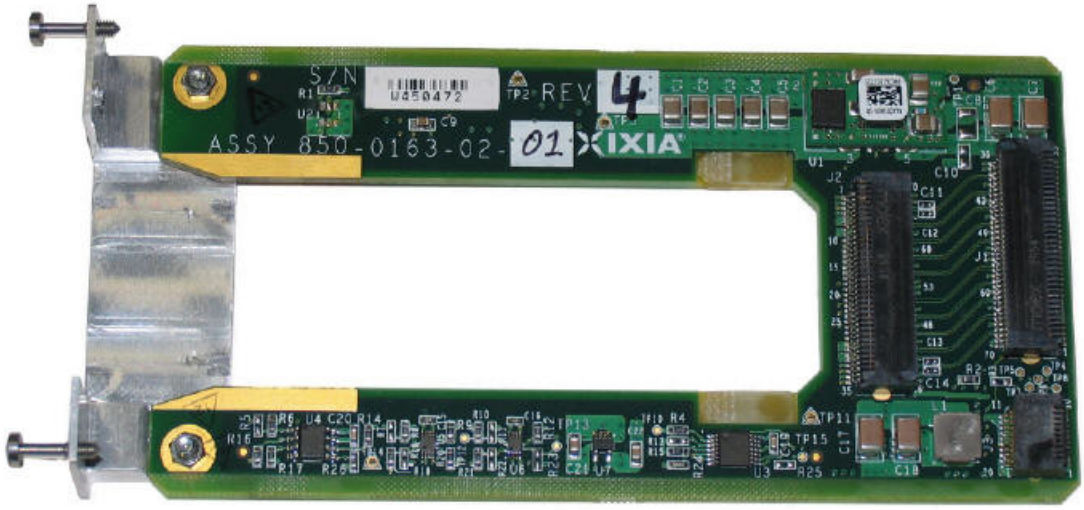


Figure 20-9. X2 Carrier Card with X2 Transceiver

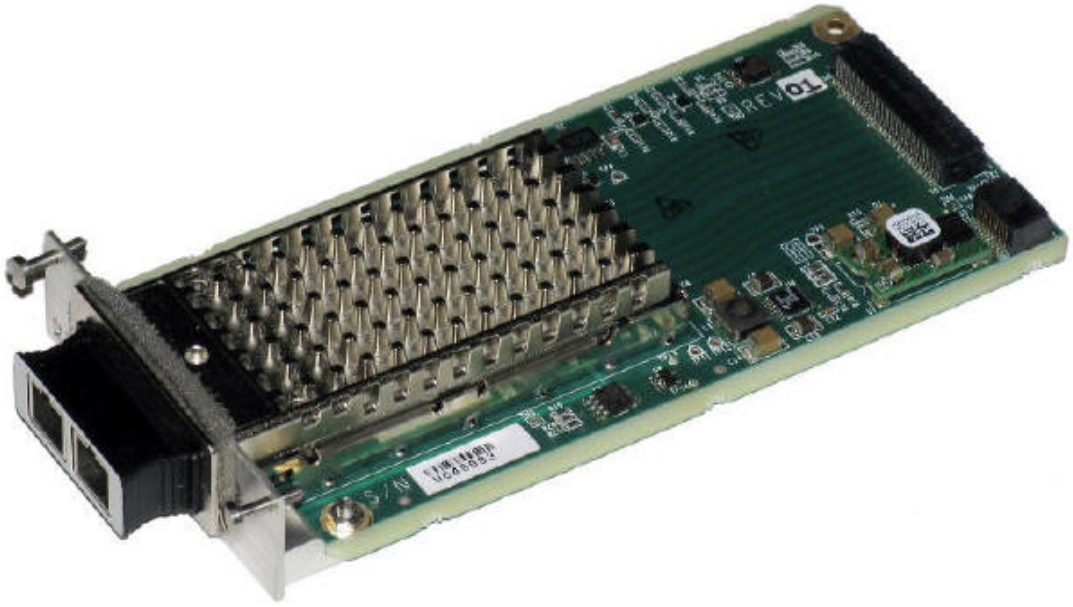


Figure 20-10.XFP-ADAP-02 Carrier Card

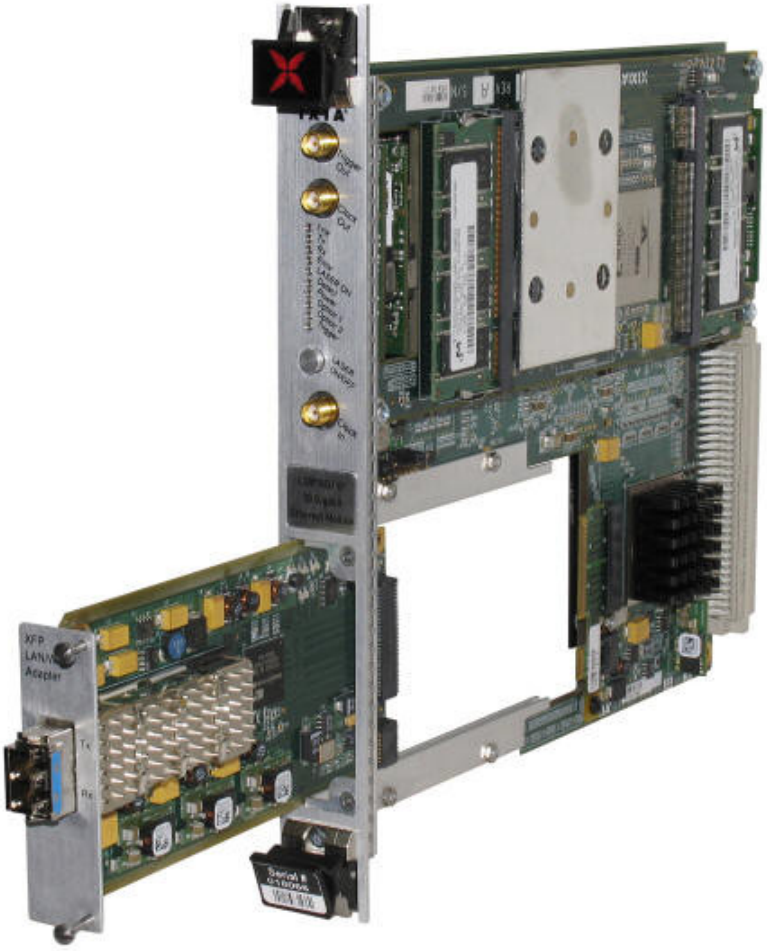
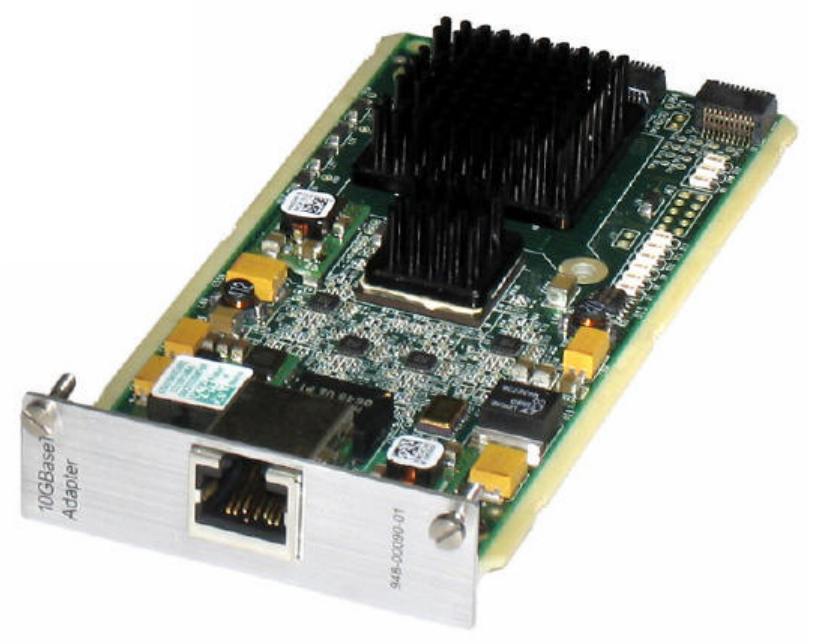


Figure 20-11. 10GBase-T Adapter Module



Carrier Card Installation

To install the carrier card, do the following:

1. Insert the card into the opening in the 10GE LSM module.
2. Slide the card along the guide rails until it connects to the load module.
3. Tighten the screws so that the carrier card is firmly in place. Do not over tighten the screws (no more than a quarter turn once flush with the card front).

The carrier card can be installed either before or after the load module is connected to the chassis. It is best not to attach the transceiver to the carrier card until the card is installed in the load module. Load modules should be screwed down in the chassis before removing or installing a carrier card, to prevent from accidentally dislodging a load module from the chassis backplane.

Note: The carrier cards do not come with the required transceivers. They must be purchased separately.

XENPAK/XAUI Connectors

The LSM10G1-01 and LSM10GL1-01 load modules have XAUI and XENPAK connectors available. See *XAUI Connectors* on page 20-27 and *XENPAK Connectors* on page 20-33 above for more information on XENPAK connectors.

These connectors are only applicable when the XENPAK carrier is being used.

Statistics

Statistics for 10GE LSM cards (except NGY), under various modes of operation may be found in *Table B-23* on page B-118. Statistics for NGY load modules may be found in *Table B-24* on page B-126.

NGY Fault Handling

IEEE Requirements

IEEE 802.3ae, section 46.3.4 defines how a Reconciliation Sublayer (RS) shall respond to Local and Remote Faults. Response to a Local Fault is to immediately cease sending traffic on the transmit data path (even if doing so truncates a frame) and to send continual Remote Faults. Response to a Remote Fault is to stop sending MAC data (completing any frame that is being transmitted) and to send continual idles.

NGY Operation

NGY load modules have a single statistic for Faults called Link Fault State. This statistic is real-time and indicates the current state of the port's Reconciliation Sublayer (RS) state machine. The possible statistics values are:

- No Fault
- Local Fault
- Remote Fault

Features that force deviation from IEEE spec

Note: In general, if a NGY port appears to be transmitting according to the Frames Sent statistic, be aware that Link Fault State may override this.

Tx Ignores Rx Link Faults

This feature is enabled through the **Link Fault Signaling** tab of Port Properties. When the feature is enabled, the Fault statistic continues to indicate the RS state of the port; however, the transmit-side response behaves as if no fault was received. That is to say, Remote Faults are not sent as a response to Local Fault and Idles are not forced as a response to Remote Fault, even though Link Fault State indicates the board is in a Fault state.

Transmit Ignores Link Status

This feature is enabled through the Transmit Modes tab of Port Properties. When the feature is enabled, a port is permitted to transmit under conditions that would normally inhibit transmit. For instance, a port that has no link and is not in diagnostic loopback appears in IxExplorer as red color, and is normally not permitted to transmit. Enabling this feature allows transmit. When the feature is enabled, the statistic called Link State indicates 'Ignore Link'.

Note that if the port is in Fault, enabling this feature and forcing transmit may result in misleading results. The port shown in the following stat view (Figure 20-12) is ignoring link (see Link State statistic), is in Remote Fault (see Link

Fault State statistic), yet appears to be transmitting (see Frames Sent Rate statistic). The reality is that no frames are actually leaving the port because the port is in Remote Fault. This is because the block that maintains the transmit statistics is located before the block that forces idles as a response to Remote Fault.

Figure 20-12. Statistic View for NGY, Ignore Link Status

	A	B
1	Name	loopback:02.01
2	Link State	Ignore Link
3	Line Speed	10GE LAN
4	Frames Sent	164,624,279
5	Frames Sent Rate	14,880,954
6	Valid Frames Received	0
7	Valid Frames Received Rate	0
8	Bytes Sent	10,535,953,80
9	Bytes Sent Rate	952,380,945
10	Bytes Received	0
11	Bytes Received Rate	0
12	Fragments	0
13	Undersize	0
14	Oversize	0
15	CRC Errors	0
16	Link Fault State	Remote Fault
17	Scheduled Transmit Duration	0 : 0: 0.0
18	Bytes Sent / Transmit Duration	21,740,528
19	Bits Sent	84,287,630,43
20	Bits Sent Rate	7,619,047,560
21	Bits Received	0
22	Bits Received Rate	0
23	Central Chip Temperature(C)	45
24	Port Chip Temperature(C)	45
25	Port CPU Status	Ready
26	Port CPU DoD Status	Ready

Intrinsic Latency Adjustment

This option, when present and enabled, reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). For a specific transceiver, the system retrieves its pre-determined latency value and subtracts this from the measured overall latency. For an ‘unknown’ transceiver (not previously measured), it calculates and stores the intrinsic latency value.

On the **General** tab in **Port Properties**, the **Latency Calibration** option is only enabled for cards with transceivers that have not been pre-measured for intrinisic latency by Ixia. The **Latency Calibration** option is grayed-out if any one of the following conditions are present:

- There is no carrier.
- There is no transceiver.
- The transceiver is XFP or XAUI (which do not need to be calibrated).

- The transceiver is XENPAK or X2 and a value is found for it in the list of pre-calibrated values.

The **Latency Calibration** option is enabled if the transceiver is XENPAK or X2 but no pre-calibrated value is found in the stored list. The **Latency Calibration** option is also enabled for transceivers that you have previously calibrated, so that the calibration measurement may be repeated (if desired).

Clicking the **Latency Calibration** option runs a Tcl script that measures intrinsic latency and stores the value in an .xml file. The .xml file contains the values that you have produced and saved. Each value is identified for a specific transceiver (per manufacturer, model, and serial number). You can run the calibrate process repeatedly with the same transceiver (if desired). Each new measurement overwrites the previous one for that transceiver.

Running the calibration measurement puts the port into a special loopback mode to measure intrinsic latency. When done, the port is put back into default normal mode. Any port configuration you have set before calibrating intrinsic latency, is lost as the port reverts to a default configuration.

The **Enable** check box is grayed out when no value exists in the system for the specific transceiver. If a value exists (in the .xml file) then the **Enable** check box is available. Select the check box to enable the intrinsic latency adjustment.

After the intrinsic latency adjustment has been done, you may want to refresh the chassis or close and reopen the Port Properties dialog.

Note: The LSM10GMS-01 load module always compensates for intrinsic latency—it is not optional. Also, this load module does not support the'No CRC' option. Any imported stream with No CRC enabled is Forced Valid to 'Bad CRC'.

10GE LAN Family

Part Numbers

The currently available LAN family part numbers are shown in the following table. Items without a *Price List Names* entry are no longer available.

Table 20-7. 10GE LAN Load Modules

Load Module	Part Number	Description
LM10GELAN	LM10GE223F	10GBASE-LR (LAN), 1-port, 1310nm, singlemode
	LM10GE224F	10GBASE-ER, (LAN) 1-port, 1550nm, singlemode
LM10GELAN-M	LM10GE223M	10GBASE-LR (LAN), 1-port, 1310nm, singlemode, manufacturing mode
	LM10GE224M	10GBASE-ER (LAN), 1-port, 1550nm, singlemode, manufacturing mode

Specifications

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 20-8. 10GB LAN Load Module Specifications

	10GBASE-R (LAN)
# ports	1
-M Card Available	Y
Layer2/Layer3 Card Available?	N
Layer 7 Card Available	N
Data Rate	10GB
Connector/Wavelength-Mode	SC/850 multimode, 1310nm /1550nm singlemode
Capture buffer size	32MB
Captured packet size	24-65,000 bytes
Streams per port	255, 32 (-M version)
Advanced streams	160, 16 (-M version)
Preamble size: min-max	8
Frame size: min-max	24-65,000
Inter-frame gap: min-max	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min-max	4.0ns - 42sec in 10.0ns steps
Inter-stream gap: min-max	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate
Advanced stream min frame rate[1]	Slow: 0.023fps Med: 95fps Fast: 1525fps
Latency	20ns resolution

1. Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

The LAN-M boards includes all of the features of the LAN board with the following exceptions:

- No support for routing protocols
- No real-time latency, but timestamps are included
- 32 streams in packet stream mode
- 16 streams in advanced scheduler mode
- No configurable preamble

When performing sequence checking, no more than 8192 packet group IDs should be used.

Port LEDs

Each 10GB LAN port incorporates a set of LEDs, as described in the Table 20-9.

Table 20-9. 10GE LAN Port LEDs

LED Label	Usage
Link	Green if Ethernet link has been established, red otherwise. Link may be down due to no signal or no PCS lock.
Tx/Pause	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction.
Rx/Error	Green while data is received. Red on any Ethernet error. Off if no frames are received.
Trigger	See below.
Option	Reserved for future use.
LASER ON	Green when the port's laser is turned on. Off otherwise.

Trigger Out Values

The signals and LEDs available on the trigger out pins for these cards are described in the following table.

Table 20-10. 10GE LAN Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on Rx Pause Request, high (+5V) otherwise.
Trigger Out B	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.

Optical Specifications

The optical characteristics for the 10GE LAN cards is described in *Table 20-11*.

Table 20-11. 10GE Optical Specifications

Specification	10GBASE-SR (LAN) 850nm	10GBASE-LR (LAN) 1310nm	10GBASE-ER (LAN) 1550nm
Tx Power (dBm)	-5 to -1	-6 to 2	-4 to 0
Rx Sensitivity (dBm)	-7 to -1	-11 to -1	-5 to 2
Safety	Class 1 Laser	Class 1 Laser	Class 1 Laser

Statistics

Statistics for 10GB cards, under various modes of operation may be found in *Table B-21* on page B-103 and *Table B-22* on page B-110.

XAUI Family

Part Numbers

The XAUI family part numbers are shown in the following table.

Table 20-12. 10GE XAUI Load Modules

Load Module	Part Number	Description
LM10GEXAUI	LM10GE500F1	10GBASE (XAUI), 1 port
LM10GEXAUI+ BERT	LM10GE500F1B	10GBASE (XAUI), Ethernet/BERT, 1 port
LM10GEXAUI BERT only	LM10GE500M1B	10GBASE (XAUI), BERT, 1 port
Cables	CAB10GE500S1	XAUI cable, 20 inch, standard pinout
	CAB10GE500S2	XAUI cable, 40 inch, standard pinout
	BOB10GE500	XAUI SMA break-out box
	CON10GE500	XAUI Fujitsu MicroGiGa connector
	LPG10GE500	XAUI front panel loopback connector

Specifications

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 20-13. 10GB XAUI Load Module Specifications

	10GBASE (XAUI)	10GBASE (XAUI/ BERT)
# ports	1	1
-M Card Available	N	N
Layer2/Layer3 Card Available?	N	N
Layer 7 Card Available	N	N
Data Rate	10GB	N/A
Connector/Frequency-Mode	See *XAUI Connectors* on page 20-27	See *XAUI Connectors* on page 20-27
Capture buffer size	32MB	N/A
Captured packet size	24-65,000 bytes	N/A
Streams per port	255	N/A
Advanced streams	160	N/A
Preamble size: min-max	8	N/A
Frame size: min-max	24-65,000	N/A

Table 20-13. 10GB XAUI Load Module Specifications

	10GBASE (XAUI)	10GBASE (XAUI/ BERT)
Inter-frame gap: min-max	4.0ns - 42sec in 3.2ns steps	N/A
Inter-burst gap: min-max	4.0ns - 42sec in 10.0ns steps	N/A
Inter-stream gap: min-max	4.0ns - 42sec in 10.0ns steps	N/A
Normal stream frame rate	0.023fps - full line rate	
Advanced stream min frame rate[1]	Slow: 0.023fps Med: 95fps Fast: 1525fps	
Latency	20ns resolution	N/A

1. Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

XAUI accessories are discussed in *Appendix A, XAUI Connector Specifications*.

Port LEDs

Each 10GB XAUI port incorporates a set of LEDs, as described in the following table.

Table 20-14. 10GE XAUI Port LEDs

LED Label	Usage
Link	Green if Ethernet link has been established, red otherwise. Link may be down due to no signal or no PCS lock.
Tx/Pause	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction.
Rx/Error	Green while data is received. Red on any Ethernet error. Off if no frames are received.
Trigger	See below.
Option	Reserved for future use.
LASER ON	Green when the port's laser is turned on. Off otherwise.

Trigger Out Values

The signals and LEDs available on the trigger out pins for these cards are described in the following figure.

Table 20-15. 10GE XAUI Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on Rx Pause Request, high (+5V) otherwise.
Trigger Out B	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.

Clock In/Out

The XAUI load module provides SMA coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the XAUI interface. When running off an external clock, the clock input signal must meet the requirements listed in Table 20-16 to ensure proper performance of the load module.

Table 20-16. XAUI Reference Clock Input Requirements

Parameter	Characteristic
Frequency	156.25 MHz ±100ppm
Jitter	±150ps max. cycle to cycle, >1kHz
Amplitude	0.9 Vpp minimum, into 50 Ω
Duty cycle	40 to 60%
Edge rates (20% to 80%)	600ps maximum, into 50 Ω

The clock in/out electrical interface parameters are defined in Table 20-17.

Table 20-17. XAUI Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
Clock Input	Connector	Female SMA
	Impedance	50 ohm ± 5%, DC coupled
	Absolute max input	6V (DC plus half AC peak-to-peak
Clock Output	Connector	Female SMA
	Impedance	50 ohm ± 5%, AC coupled
	Amplitude	0.9 Vpp minimum, into 50 Ω. (1.5 Vpp typical)
	Edge rates	200ps to 340ps (20% to 80%) into 50Ω
	Duty cycle	45% to 55%
	Jitter	20ps max cycle to cycle, >1kHz
	Frequency	156.25 MHz ±20ppm (internal clock mode)

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

XAUI Connectors

The following connectors and adapters are available for the XAUI Load Modules and are discussed in *Appendix A, XAUI Connector Specifications*.

- *Standard Connector Specifications*: the signals carried on the Load Module's XAUI connector.
- *Front Panel Loopback Connector*: a connector used to loopback XAUI signals at the external connector.
- *Standard Cable Specification*: the CAB10GE500S1 (20 inch) and CAB10GE500S2 (40 inch) cables.
- *SMA Break-Out Box*: the BOB10GE500 SMA break-out box.

MDIO

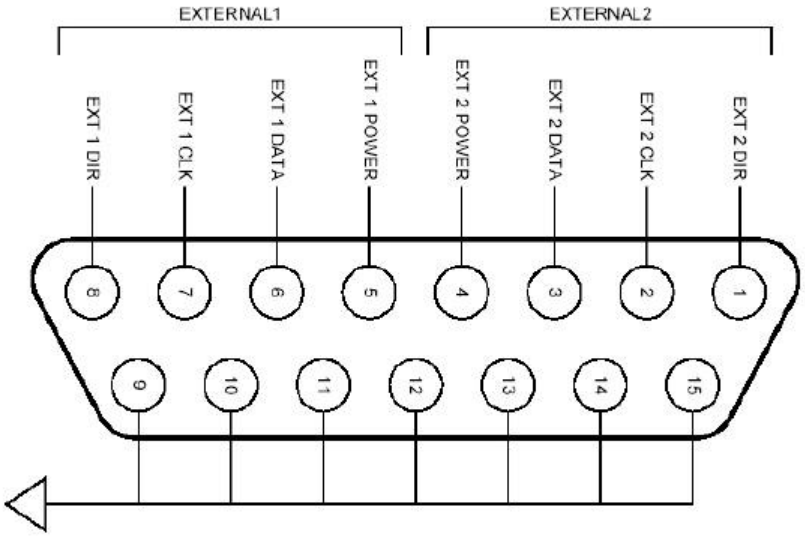
A Management Data Input/Output (MDIO) interface is provided to you. The Ixia Load Module acts as the Station Management entity (STA), and can control one or more MDIO Manageable Devices (MMD) in the users system. Multiple MMDs can be attached to the interface. You can set/read the MDIO control/status registers inside a MMD through a graphical user interface.

The connector used for the MDIO interface is a 15-pin female D-sub and provides with the ability to add up to two external Mii interfaces compliant to either 802.3 clause 22 or 802.3ae clause 45. The connector pin assignments, Mii Interface, signal names, and functional descriptions are listed in *Table 20-18*.

Table 20-18. MDC/MDIO Connector Pin Assignments

Pin No.	Mii Interface	Signal Name	Functional Description
1	External 2	DIR	Data direction control.
2	External 2	MDC	Clock.
3	External 2	MDIO	Bi-directional data.
4	External 2	+5V	+5Vdc supply.
5	External 1	+5V	+5Vdc supply.
6	External 1	MDIO	Bi-directional data.
7	External 1	MDC	Clock.
8	External 1	DIR	Data direction control.
9-15	GND	GND	Ground

Figure 20-13.MDC/MDIO D-sub Connector Pin Assignments



WARNING: The MDIO on the Ixia XAUI Load Module is 3.3V while the Ixia XENPAK Load Module, when used with the adapter for XAUI, is 1.2V. The reason for the difference is that the XENPAK MSA requires 1.2V for MDIO whereas most XAUI SerDes chips require 3.3V (LVTTL). Therefore, when using the XAUI Load Module to test a XENPAK transceiver or SerDes, which require 1.2V, a level shifter is needed to convert 3.3V to 1.2V.

The MDIO/MDC interface has a clock line (MDC) and bi-directional data line (MDIO) as defined in IEEE 802.3ae. In addition to these, a +5Vdc supply, and data direction control line (DIR) are provided to make interfacing easier for you. The +5Vdc output is intended to power buffers and/or optocouplers at the user-end of the cable. This supply can be turned ON or OFF under software control through the GUI.

The +5Vdc supply is OFF when the chassis is initially powered-up, or following a reset.

For more information on XAUI connectors, see *Appendix A, XAUI Connector Specifications*.

Statistics

Statistics for 10GB cards, under various modes of operation may be found in *Table B-21* on page B-103 and *Table B-22* on page B-110.

XENPAK Family

The LM10GE700P3 family is referred to as the XENPAK load modules. Each card accepts a XENPAK transceiver, or with an appropriate carrier card accepts an XPAK or X2 transceiver. Five variants are available, which feature Ethernet and/or BERT modes and full or manufacturing mode.

Part Numbers

The XENPAK family part numbers are shown in *Table 20-19*.

Table 20-19. 10GE XENPAK Modules

Load Module	Part Number	Description
LM10GEXENPAK	LM10GE700F1	10GE (XENPAK), Ethernet, 1-port
	LM10GE700F1-P	10GE (XENPAK), Ethernet, 1-port, PowerPC with 256MB of processor memory.
LM10GEXENPAK-M	LM10GE700M1	10GE (XENPAK), Ethernet, 1-port, manufacturing mode
LM10GEXENPAK+ BERT	LM10GE700F1B	10GE (XENBAK), Ethernet/ Bert, 1-port
LM10GEXENPAK BERT only	LM10GE700M1B	10GE (XENPAK), BERT only, 1-port, manufacturing mode
LM10GEXENPAK-MA+BERT	LM10GE700M2B	10GE (XENPAK), Ethernet+BERT, 1-port, manufacturing mode
Transceivers	XENPAK-LR	XENPAK Transceiver - 1310nm LAN, 10GBASE-LR
	XENPAK-SR	XENPAK Transceiver - 850nm LAN, 10GBASE-SR
	XENPAK-ER	XENPAK Transceiver - 1550nm LAN, 10GBASE-ER
	XENPAK-CX4	XENPAK Transceiver - CX4 Interface (10GBASE-CX4)
Cables	CAB10GE-CX4	CX4-to-CX4 cable, 1 meter
	CX410GE500	CX4 to XENPAK adapter
	FXN10GE500	XAUI Fujitsu to XENPAK Adapter

Specifications

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 20-20. 10GB Load Module Specifications—Part 3

	10GBASE (XENPAK)
# ports	1
-M Card Available	Y
Layer2/Layer3 Card Available?	N
Layer 7 Card Available	N
Data Rate	10GB
Connector/ Frequency-Mode	See *XENPAK Connectors* on page 20-33
Capture buffer size	32MB
Captured packet size	24-65,000 bytes
Streams per port	255, 32 (-M version)
Advanced streams	160
Preamble size: min-max	8
Frame size: min-max	24-65,000
Inter-frame gap: min-max	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min-max	4.0ns - 42sec in 10.0ns steps
Inter-stream gap: min-max	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate
Advanced stream min frame rate[1]	Slow: 0.023fps Med: 95fps Fast: 1525fps
Latency	20ns resolution

1. Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

The -M load modules includes all of the features of the non-M board with the following exceptions:

- No support for routing protocols
- No real-time latency, but timestamps are included
- 32 streams in packet stream mode
- 16 streams in advanced scheduler mode

- No configurable preamble

When performing sequence checking, no more than 8192 packet group IDs should be used.

Port LEDs

Each 10GB port incorporates a set of LEDs, as described in the following tables.

Table 20-21. 10GE XENPAK Port LEDs

LED Label	Usage
Link	Green if Ethernet link has been established, red otherwise. Link may be down due to no signal or no PCS lock.
Tx/Pause	Green while data is transmitted. Red while flow control frames are received. Off if no traffic is passing in either direction.
Rx/Error	Green while data is received. Red on any Ethernet error. Off if no frames are received.
Trigger	See below.
LASER ON	Green when the port's laser is turned on. Off otherwise.

Trigger Out Values

Trigger out values depend on the particular board type.

XENPAK Load Modules

The signals and LEDs available on the trigger out pins for these cards are described in *Table 20-22*.

Table 20-22. 10GE XENPAK 1-Slot Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on Rx Pause Request, high (+5V) otherwise.
Trigger Out B	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.

Clock In/Out

The load module provides SMA coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in Table 20-23 to ensure proper performance of the load module.

Table 20-23. Reference Clock Input Requirements

Parameter	Characteristic
Frequency	156.25 MHz ±100ppm
Jitter	±150ps max. cycle to cycle, >1kHz
Amplitude	0.9 Vpp minimum, into 50 Ω
Duty cycle	40 to 60%
Edge rates (20% to 80%)	600ps maximum, into 50 Ω

The clock in/out electrical interface parameters are defined in Table 20-24.

Table 20-24. Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
Clock Input	Connector	Female SMA
	Impedance	50 ohm ± 5%, DC coupled
	Absolute max input	6V (DC plus half AC peak-to-peak
Clock Output	Connector	Female SMA
	Impedance	50 ohm ± 5%, AC coupled
	Amplitude	0.9 Vpp minimum, into 50 Ω. (1.5 Vpp typical)
	Edge rates	200ps to 340ps (20% to 80%) into 50Ω
	Duty cycle	45% to 55%
	Jitter	20ps max cycle to cycle, >1kHz
	Frequency	156.25 MHz ±20ppm (internal clock mode)

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

XENPAK Connectors

Power Sequencing Specification

The Xenpak 2.1 MSA does not specify any particular power sequencing for the various Xenpak power supply rails (3.3V, 5V, and APS).

When Xenpak Power is enabled, power sequencing is as follows:

- The 5V rail comes up first, with a ramp-up time of approximately 2.25 ms.
- The 3.3V and APS rails both start to come up about 500 us after 5V rail is up.
  - The 3.3V supply has a ramp-up time of approximately two milliseconds.
  - The APS supply ramp-up time varies, according to level required by APS Set resistor, but will be no more than two milliseconds. When no Xenpak module is inserted into the Load Module, APS voltage is less than 150 mV.

Reset

Hardware asserts a Reset by bringing Xenpak connector pin 10 low whenever either of the following conditions is true:

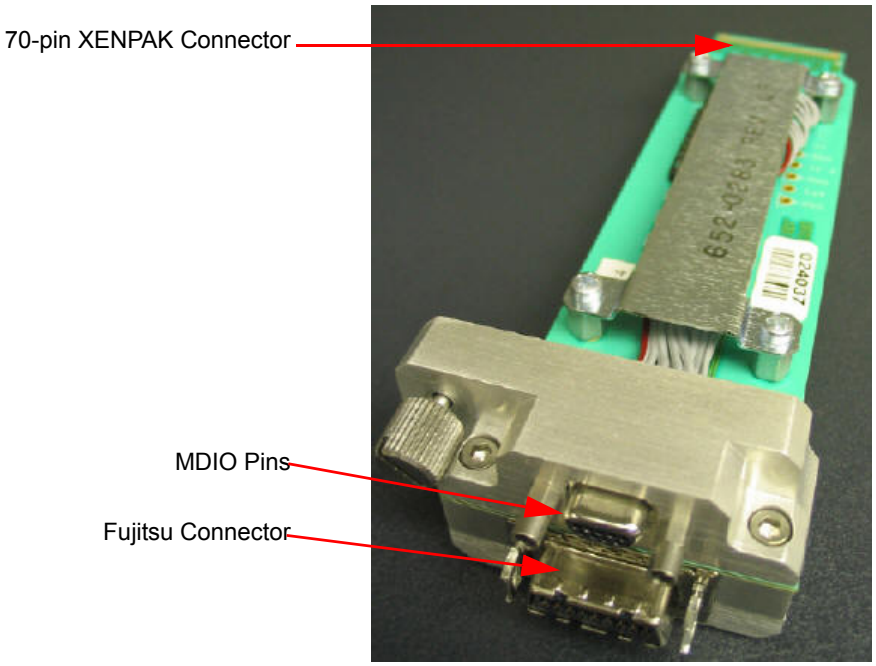
- The Xenpak module is not inserted into the load module; that is, Xenpak pin 14 is high.
- Xenpak power is turned off.

The hardware continues to assert Reset until both of these items are false. Once Xenpak Power is asserted, or if a Xenpak is hot-plugged, the system waits 5 seconds for Xenpak initialization (per MSA 2.1). Reset is then de-asserted, and the system waits an additional 500 ms for any vendor-based reset management to complete initialization. After this final 500 ms delay, the load module assumes the Xenpak module is ready for MII access or to transmit and receive.

XAUI Fujitsu to XENPAK Adapter

The XAUI Fujitsu to XENPAK Adapter (P/N FXN10GE500) is shown in Figure 20-14.

Figure 20-14. XAUI Fujitsu to XENPAK Adapter



The MDIO pins are pictured and described in Figure 20-15 and Table 20-25.

Figure 20-15. MDIO Pins for XAUI Fujitsu to XENPAK Adapter

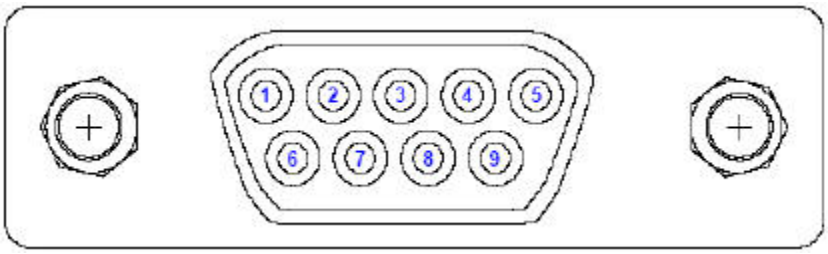


Table 20-25. MDIO Pin Assignments for XAUI Fujitsu to XENPAK Adapter

Pin	Signal
1	PU-5V
2	PU-3.3V
3	PU-APS
4	LASI (GND)
5	RESET
6	TX ON/OFF

Table 20-25. MDIO Pin Assignments for XAUI Fujitsu to XENPAK Adapter

Pin	Signal
7	MDIO
8	MDC
9	GND

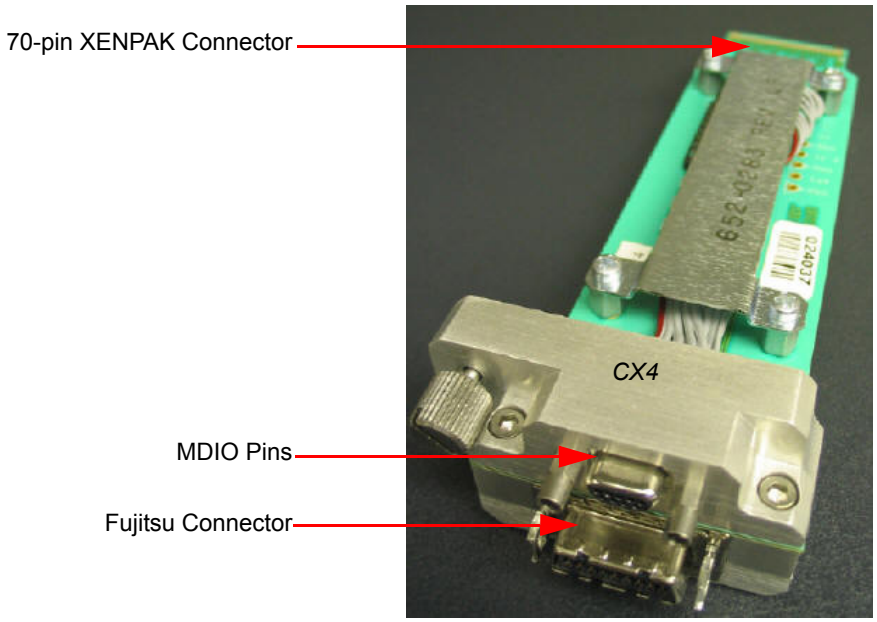
This MDIO pinout is the same for the CX4 to XENPAK adapter (P/N CX410GE500).

For more information on XAUI connectors, see *Appendix A, XAUI Connector Specifications*.

CX4 to XENPAK Adapter

The CX4 to XENPAK Adapter (P/N CX410GE500) is shown in Figure 20-16.

Figure 20-16. CX4 to XENPAK Adapter



The MDIO pins are pictured and described in Figure 20-15 and Table 20-25.

For more information on XAUI connectors, see *Appendix A, XAUI Connector Specifications*.

Statistics

Statistics for 10GB cards, under various modes of operation may be found in *Table B-21* on page B-103 and *Table B-22* on page B-110.

21 IXIA 10GE LAN/WAN and OC 192 POS Load Modules

Overview

Ixia offers two families of load modules that operate in multiple modes, as specified in Table 21-1.

Table 21-1.Operating Modes Available for Multimode Cards

Family	OC-192 POS	BERT	10GE WAN	10GE LAN	FEC	VCAT/ Channel ized
10G MSM	X		X	X		X
OC-192 Triple Mode	X	X	X			
UNIPHY	X	X	X	X	X	

Full specifications for each family may be found at:

- *10G MSM Family* on page 21-1
- *OC-192c Triple Mode Family* on page 21-6
- *UNIPHY Family* on page 21-12

10G MSM Family

The 10G MSM load module family consists of a UNIPHY LM Load module which supports SONET and Ethernet at 10G rates. Modes supported on this board include POS, WAN, and LAN. For POS there is additional feature support such as DCC, RPR, and SRP.

Figure 21-1 on page 21-2 displays the 10G MSM module.

Figure 21-1. MSM10G1-02 Load Module

Note: Due to power requirements, only one MSM module can be used in a 250 or 400T chassis. Other modules can be used with the MSM in the same chassis, but only one CPM1000T8 at a time (except the CMP1000T8 module, which has the same limitation).

Part Numbers

The MSM family part numbers are shown in *Table 21-2*.

Table 21-2. 10G MSM Modules

Load Module	Part Number	Description
MSM10G1-02	944-0012	10GE OC192 load module, 1-port Multi Services Module, supports 10GE LAN/WAN and optional OC-192c POS (order OPTOC192POS). Full features: supports routing and Linux-based applications. Requires an XFP transceiver. Purchase options include XFP-1310 and XFP-1550. **Note**: Maximum one (1) MSM10G1-02 load module permitted per IXIA 400T chassis .
	945-0005	SW-VCAT-SONET configuration option, SONET Virtual Concatenation (VCAT) Option license per port. Includes support for LCAS and GFP-F protocols. Requires purchase of a supported load module (see 945-0003 MSM2.5G1-01 or 944-0012 MSM10G1-02)
	945-0002	SW-RPRSRP-SONET, OC-48/ OC-192 configuration option, SONET RPR and SRP stream generation and protocol support, license per port. Requires purchase of a supported load module (see LMOC192xx, LM10GUxF, LMOC48xx, 945-0003 MSM2.5G1-01, or 944-0012 MSM10G1-02)
	OPTOC192POS	10 Gigabit Ethernet OC-102 POS configuration option for 944-0012 (MSM10G1-02) and LM10GUxx load modules.

Specifications

.

Table 21-3. 10G MSM Load Module Specifications

	MSM10G1-02
# ports	1
-M Card Available	No
Layer2/Layer3 Card Available?	Yes

Table 21-3. 10G MSM Load Module Specifications

	MSM10G1-02
Layer 7 Card Available	No
Data Rate	10GB
Connector/ Wavelength-Mode	XFP 1310nm or 1550nm Single or pluggable
Capture buffer size	Up to 384 MB
Captured packet size	17-65,535bytes
Streams per port	256
Advanced streams	256
Preamble size: min-max	8
Frame size: min-max	17-65,535
Inter-frame gap: min-max[1]	4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min-max	4.0ns - 42sec in 10.0ns steps
Inter-stream gap: min-max	4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate
Advanced stream min frame rate[2]	Slow: 0.023fps Fast: 1525fps
Latency[3]	20ns resolution

1. Packet gap size also depends on the stream mode selected, Fixed or Average.

2. Streams are divided up into two categories: 224 slow speed streams and 32 fast streams.

3. When performing latency measurements in POS mode, the following restrictions apply:

   The minimum frame size should be 80 bytes for latency measurements to be supported at line rate. On the MSM10G, there is only one packet group mode (wide packet groups) . Two different scenarios apply:

If sequence checking is enabled, then the number of packet group IDs is limited in this way:

When Wide Bin Mode (on the Wide Packet Groups page) is **not** enabled = 65536.

When Wide Bin Mode is enabled = 524288.

If sequence checking is **not** enabled, then the number of packet group IDs is limited in this way:

When Wide Bin Mode (on the Wide Packet Groups page) is **not** enabled = 65536.

When Wide Bin Mode is enabled = 2097152.

Port LEDs

Each 10G MSM port incorporates a set of LEDs, as described in the following table.

Table 21-4. 10G MSM Port LEDs

LED Label	Usage
LASER ON	Green when the port's laser is turned on. Blank otherwise.
Pause	Green when transmit is paused, blank when powered off.
PPP/Link	Green in link up condition, Red in link down condition, blank indicates loopback mode enabled.
Tx	Green if transmit is active and frames are being sent, blank otherwise.
LOS	Green when signal level is good, Red when loss of signal occurs, blank if no transceiver detected.
Option	N/A
Trigger	Green when Trigger A condition occurs, Red for Temperature Fault, blank otherwise.
Error	Red when module in error state (fault condition), blank otherwise.
Rx	Green indicates valid receive frames, Red indicates errored frames received, blank when no frames received.
LOF	Green when valid framing occurs, Red when Loss of Frame occurs.

Clock In/Out

The load module provides coaxial connectors for clock input and clock output to allow the DUT to phase-lock with the interface. When running off an external

clock, the clock input signal must meet the requirements listed in Table 21-5 to ensure proper performance of the load module.

Table 21-5. Clock Input Specifications

Parameter	Characteristic
Connector	SMA
Frequency	SONET: 155.52 MHz ±20ppm 10GE: 161.132 MHz ±-100ppm
Amplitude	1.1 Vpp minimum, into 50 Ω, AC coupled
Duty cycle	40 to 60%

The clock in/out electrical interface parameters are defined in Table 21-6.

Table 21-6. Clock Output Specifications

Parameter	Characteristic
Connector	SMA
Frequency	SONET: 155.52 MHz ±20ppm 10GE: 161.132 MHz ±-100ppm
Amplitude	500m Vpp minimum, 600 Vpp typical into 50 Ω
Duty cycle	40 to 60%

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

Trigger Out

The signals and LEDs available on the trigger out pins for these cards are described in *Table 21-7*.

Table 21-7. 10G MSM Trigger Out Signals

Pin/LED	Value
Trigger Out	10nS active high pulse on trigger
Trigger LED	Indicates Trigger, Pause Frame received in 10GE mode.

Statistics

Statistics for 10G MSM cards, under various modes of operation may be found in *Table B-25* on page B-134.

OC-192c Triple Mode Family

The OC-192c Triple Mode family of load modules implements Optical Carrier interfaces that run at OC192 speeds. The interface operates in concatenated

mode, as opposed to channelized mode. One of the modules in this family (the LMOC192cPOS) is shown in *Figure 21-2*.

Figure 21-2. LMOC192c Load Module

Part Numbering

The OC192 cards come with a number of options. All part numbers are of the form:

LMOC192*HTOS* or

LMFOC192*HTOS*

where ***H*** is the hundreds designator, ***T*** is the tens designator, ***O*** is the ones designator, and ***S*** is the suffix.

LMF boards have no fiber optic interface. It allows for quick validation of serializer and deserializer designs for WAN Packet over SONET/SDH products operating at the STS-192c/STM-64 level. The LMF interface is a 300 pin MegaArray BERG connector, which is an industry standard MSA interface and is compliant per OIF1999.102.8, SFI-4 specification. A reference clock can be supplied through this interface ranging in frequency from 25 MHz to 622 MHz.

The part numbers for these load modules are shown in *Table 21-8*. Items without a *Price List Names* entry are no longer available.

Table 21-8. OC-192c Load Modules

Load Module	Part Number	Description
LMOC192cPOS		POS, 1-port, intermediate reach (SR1), 1310nm, singlemode.
		POS, 1-port, intermediate reach, 1310nm, singlemode.
		POS, 1-port, intermediate reach, 1550nm, singlemode.
		POS, 1-port, no optics.
LMOC192cVSRPOS	LMOC192168	POS, 1-port, VSR optics, parallel interface.
LMOC192cBERT		BERT, 1-port, intermediate reach, 1310nm, singlemode.
		BERT, 1-port, intermediate reach, 1550nm, singlemode.
LMOC192cVSR-BERT		BERT, 1-port, VSR optics, parallel interface.

Table 21-8. OC-192c Load Modules

Load Module	Part Number	Description
LMOC192cPOS+ BERT		POS with BERT, 1-port, intermediate reach, 1310nm, singlemode.
		POS with BERT, 1-port, intermediate reach, 1550nm, singlemode.
LMOC192cVSR-POS+BERT	LMOC192468	POS with BERT, 1-port, VSR optics.
LMOC192cPOS+ WAN		POS+WAN, 1-port, intermediate reach, 1310nm, singlemode.
LMOC192cPOS+ BERT+WAN		POS+BERT+WAN, 1-port, intermediate reach, 1310nm, singlemode.
		POS+BERT+WAN, 1-port, intermediate reach, 1550nm, singlemode.
LM10GEWAN		10GBASE-LW (WAN), 1-port, 1310nm, singlemode.
		10GBASE-EW (WAN), 1-port, 1550nm, singlemode.
Options	SW-DCCSONET	DCC SONET support.
	945-0002	SW-RPRSONET SW-SRPSONET SRP SONET and RPR SONET support.

Specifications

The load module specifications are contained in *Table 21-9*. Note that the -M modules are not included in the table; their limitations versus the non-M version are discussed in *Ixia Load Modules* on page 1-4.

Table 21-9. OC192 Load Module Specifications

	LMOC192cPOS LMOC192cPOS+ WAN	LMOC192c BERT	LMOC192c POS+BERT[1]
# ports	1	1	1
-M Card Available	N	N	N
Layer2/Layer3 Card Available?	N	N	N
Layer 7 Card Available	N	N	N
Data Rate	1-100% of OC192 speeds	N/A	
Connector/ Wavelength-Mode	SC/1310nm or 1550nm Singlemode	SC/1310nm or 1550nm Singlemode	SC/1310nm or 1550nm Singlemode
Capture buffer size	32MB	N/A	
Captured packet size	33-64k	N/A	
Streams per port	255	N/A	
Flows per port	N/A	N/A	
Advanced streams	160	N/A	
Preamble size: min-max	N/A	N/A	
Frame size: min-max	54-65535	N/A	
Inter-frame gap: min-max	N/A[2]	N/A	
Inter-burst gap: min-max	1us - 42sec	N/A	
Inter-stream gap: min-max	1us - 42sec	N/A	
Normal stream frame rate	0.023fps - full line rate		
Advanced stream frame rate[3]	Slow: 0.023 - 2083333 fps Med: 95fps - full line rate Fast: 1525fps - full line rate		
Latency	20ns resolution	N/A	

1. Refer to the LMOC192cPOS and LMOC192cBERT columns for the characteristics of this card when its port is in POS or BERT mode, respectively.
2. The inter-frame gap is indirectly controlled by the frame rate.
3. Streams are divided up into three categories: 144 slow speed streams, 8 medium streams and 8 fast streams.

The Ixia VSR modules, which were developed in accordance with the OIF Implementation Agreement VSR-1, use twelve parallel multimode fiber optic lines operating at 1.25Gbps per channel, instead of existing 1310nm or 1550nm serial optics. VSR optics are designed to drive signals over distances less than 300 meters, which is sufficient for interconnecting devices within a service provider's Point-of-Presence (POP). Over these short distances, VSR optics offer a significant cost savings compared to intermediate and long-reach serial lasers.

When performing latency measurements, the following restrictions apply:

- If latency is measured with packets that are smaller than 80 bytes, then normal (not wide-packet group) mode should be used and the number of packet group IDs is limited to 1,024.
- If packets are 80 bytes or larger, then wide-packet group mode may be used. Two different scenarios apply when using wide-packet group mode:
  - If sequence checking is enabled, then the number of packet group IDs is limited to 8,192.
  - If sequence checking is not enabled, then the number of packet group IDs is limited to 128k.

Port LEDs

Each OC192c port incorporates a set of 10 LEDs, as described in *Table 21-10*.

Table 21-10. LMOC192cPOS Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal, Green otherwise.
LOF	Red during Loss of Frame, Green otherwise.
PPP	Green if a PPP link has been established. Red otherwise.
Tx	Green while data is transmitted.
Rx	Green while data is received.
Error	Red on any error.
Trigger	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.
Option 1	Reserved for future use.
Option 2	Reserved for future use.
LASER ON	Green when the port's laser is turned on.

Trigger Out Values

The signals available on the trigger out pins for all cards in this category are described in *Table 21-11*.

Table 21-11. OC192 Trigger Out Signals

Pin	Signal
A	Low (0V) on User Defined Statistic 1 true. High (+5V) otherwise.
B	Low (0V) on User Defined Statistic 2 true High (+5V) otherwise.

Optical Specifications

The optical characteristics for the OC192c cards are described in *Table 21-12*.

Table 21-12. LMOC192c Optical Specifications

Specification	OC192c 1310nm	OC192c 1550nm	OC192c VSR-1
Manufacturer	GTRAN	GTRAN	Gore
Average Output Power—Min/Max	+1 dBm/+5 dBm	-1 dBm/+2 dBm	-10 dBm/-5 dBm
Transmit Center Wavelength—Min/Max	1300 nm/1320 nm	1530 nm/1565 nm	830 nm/860 nm
Receive Center Wavelength—Min/Max	1280 nm/1580 nm	1280 nm/1580 nm	830 nm/860 nm
Receive Sensitive—Min/Max	-17 dBm/0 dBm	-17 dBm/0 dBm	-16 dBm/-3 dBm
Safety	Class 1 Laser	Class 1 Laser	Class 1 Laser

Note: An attenuating should be used when looping back to the same port or when using a short length of cable.

Statistics

Statistics for OC192 cards, under various modes of operation may be found in *Table B-18* on page B-83.

UNIPHY Family

The UNIPHY family of load modules is based on a universal PHY which allows each port to operate in a number of modes. *Figure 21-3* and Figure 21-4 are pictures of two of the load modules in this family.

Figure 21-3. UNIPHY LM10GUEF-FEC

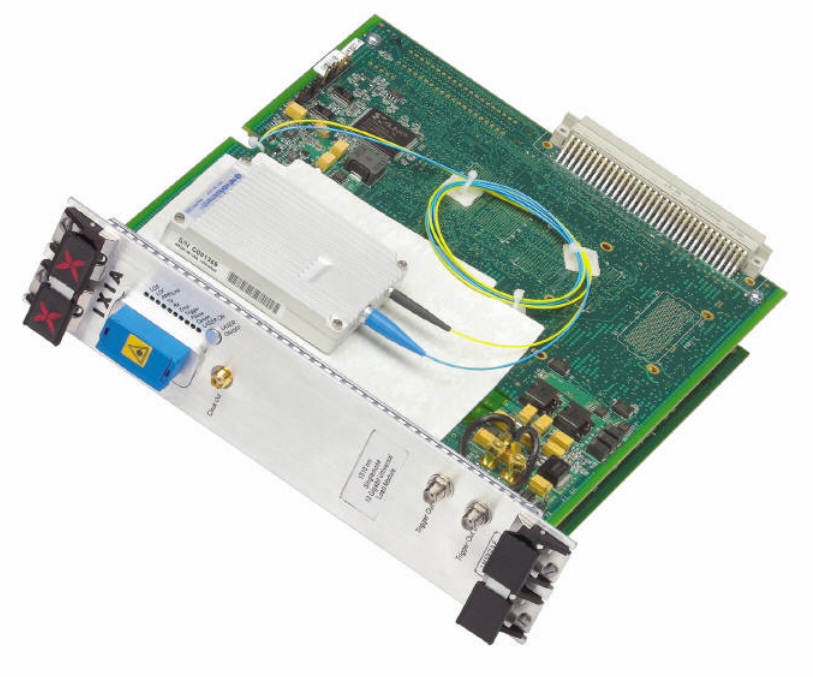
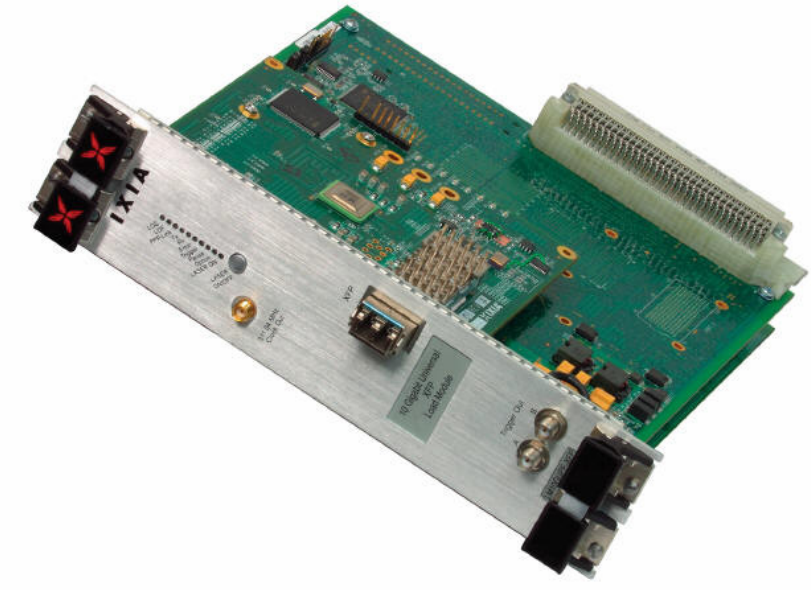


Figure 21-4. UNIPHY LM10GUPF-XFP



Part Numbers

The currently available part numbers are shown in *Table 21-13*.

Table 21-13. UNIPHY Load Modules

Load Module	Part Number	Description
LM10GUEF-FEC	LM10GUEF-FEC	10GE Universal Base Load Module with G.709 FEC capabilities, 1-port, 1550nm, singlemode. One or more of OPT10GELWAN, OPTOC192POS, or OPTOC192BERT must be purchased.
LM10GULF-P	LM10GULF-P	10GE Universal Base Load Module, 1-port, 1310nm, singlemode. -P version uses a PowerPC with 256MB processor memory. One or more of OPT10GELWAN, OPTOC192POS, or OPTOC192BERT must be purchased.
LM10GUPF-XFP	LM10GUPF-XFP	10GE Universal Base Load Module with pluggable XFP interface, 1-port. One or more of OPT10GELWAN, OPTOC192POS, or OPTOC192BERT must be purchased.
LM10GUVF	LM10GUVF	10GE Universal Base Load Module with VSR parallel optics, 1-port, 1310nm, singlemode. One or more of OPT10GELWAN, OPTOC192POS, or OPTOC192BERT must be purchased.
10G MSM	MSM10G1-02	10G Universal Base Load Module, 1-port, 1550nm, singlemode. -P version uses a PowerPC with 256MB processor memory. One or more of OPT10GELWAN or OPTOC192POS must be purchased in addition.
Transceivers	XFP-1550	XFP Transceiver, 1550nm
	XFP-1310	XFP Transceiver for LM10GUPF-XFP, 1310nm
Options	OPT10GELWAN	10GE LAN/WAN configuration option for the LM10GU*F.
	OPTOC192POS	OC-192 POS configuration option for the LM10GU*F.
	OPTOC192BERT	OC-192 BERT configuration option for the LM10GU*F.
	SW-DCCSONET	DCC SONET support for LM10GU*F.
	945-0002	SW-RPRSONET SW-SRPSONET DCC SONET support for LM10GU*F.

Specifications

The limitations of -M, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 21-14. UNIPHY Load Module Specifications

	10GUEF/ULF/ UPF/UVF (10GEWAN mode)	10GUEF/ULF/ UPF/UVF (10GE LAN mode	10GUEF/ULF/ UPF/UVF (OC192 mode)	10GUEF/ULF/ UPF/UVF (BERT mode)[1]	10GUEF-FEC[2]
# ports	1	1	1	1	1
-M Card Available	N	N	N	N	N
Layer2/Layer3 Card Available?	N	N	N	N	N
Layer 7 Card Available	N	N	N	N	N
Data Rate	1-100% of 10Gbps speeds	10GB	1-100% of OC192 speeds	N/A	1-100% of 10Gbps/ OC192 speeds
Connector/ Wavelength-Mode	SC/1310nm or 1550nm Single or pluggable	SC/1310nm or 1550nm Singlemode	SC/1310nm or 1550nm Singlemode	SC/1310nm or 1550nm Singlemode	SC/1550nm Singlemode
Capture buffer size	32MB	32MB	32MB	N/A	
Captured packet size	24-65,000 bytes	24-65,000 bytes	33-64k	N/A	
Streams per port	255	255, 32 (-M)	255	N/A	
Advanced streams	160	160 16 (-M version)	160	N/A	
Preamble size: min-max	8	8	N/A	N/A	
Frame size: min-max	24-65,000	24-65,000	54-1600	N/A	
Inter-frame gap: min-max	3/4ns - 43sec in 3.4ns steps	3.2ns - 42sec in 3.2ns steps	N/A	N/A	
Inter-burst gap: min-max	3/4ns - 43sec in 3.4ns steps	3.2ns - 42sec in 3.2ns steps	N/A	N/A	
Inter-stream gap: min-max	3/4ns - 43sec in 3.4ns steps	3.2ns - 42sec in 3.2ns steps	4ns - 42secs	N/A	
Normal stream frame rate	0.023fps - full line rate	0.023fps - full line rate	0.023fps - full line rate	N/A	
Advanced stream min frame rate[3]	Slow: 0.023fps Med: 95fps Fast: 1525fps	Slow: 0.023fps Med: 95fps Fast: 1525fps	Slow: 0.023fps Med: 95fps Fast: 1525fps	N/A	
Latency	20ns resolution	20ns resolution	20ns resolution	N/A	

1. Framed BERT only, channelized and unframed BERT are not available.

2. For values not shown, use values from the 10GEWAN/10GELan/OC192 columns according to mode.

3. Streams are divided up into three speed streams: 144 slow, 8 medium and 8 fast. MSM family streams are divided into two speed streams: 224 slow and 32 fast.

Port LEDs

Each UNIPHY port incorporates a set of LEDs, as described in the following table.

Table 21-15. UNIPHY Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal. Green when link has been established and no Loss of Signal.
LOF	Red during Loss of Frame. Green when link has been established and no Loss of Signal.
PPP/Link	Green if Ethernet/PPP link has been established. Red otherwise.
Tx	Green while data is transmitted.
Rx	Green while data is received.
Error	Red on any Ethernet error.
Trigger	Green when Trigger is applied.
Pause	Indicates flow control frames have been received.
Option	Reserved for future use.
LASER ON	Green when the port's laser is turned on. Off otherwise.

Trigger Out Values

The signals and LEDs available on the trigger out pins for UNIPHY family load modules are described in *Table 21-16*.

Table 21-16. 10 GE UNIPHY Trigger Out Signals

Pin/LED	Value
Trigger Out A	Low (0V) on User Defined Statistic 1 true, high (+5v) otherwise.
Trigger Out B	Low (0V) on (POS mode) User Defined Statistic 2 true or (Ethernet mode) pause frame detect, high (+5V) otherwise.
Trigger LED	Pulses each time a Pause Request is detected.
Pause/Option1 LED	Pulses each time a Pause Acknowledge is granted.

Clock Out Values

For -XFP suffix load modules, one coaxial connector is provided to allow phase-lock to the DUT. The frequency is either 311.0400 MHz or 322.2656 MHz +/- 100ppm.

Optical Specifications

The optical characteristics for the UNIPHY cards are described in Table 21-17.

Table 21-17. UNIPHY Optical Specifications

Type	Specification	Wavelength	Value
Transmit	Output power (dBm)	1310nm	-6 to -1
		1550nm	-1 to 2
	Distance (km)	1310nm	10
		1550nm	40
	Extinction ratio (dB)	1310nm	6
		1550nm	8.2
Receive	Rx Sensitivity (dBm)	1310nm	-12.6
		1550nm	-14
	Overload (dBm)	1310nm	-1
		1550nm	-1
	Dispersion (ps/nm)	1310nm	40
		1550nm	800

Statistics

Statistics for UNIPHY cards, under various modes of operation may be found in *Table B-21* on page B-103 and *Table B-22* on page B-110.

22 IXIA OC12 ATM/POS Load Modules

This chapter provides details about OC12 ATM/POS (LM622MR) load module —specifications and features.

The OC12 ATM/POS (LM622MR) load module enables high performance testing of routers and broadband aggregation devices such as DSLAMs and PPP termination systems. The board accommodates pluggable PHYs: The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/ Spreadsheets.

- 1310 nm multimode optics with dual-SC connectors
- Small Form-factor Pluggable (SFP) socket. Ixia offers 1310 nm singlemode and multimode transceivers with LC connectors; others may be purchased independently.

The LM622MR load module is shown in *Figure 22-1* on page 22-2.

Figure 22-1. LM622MR Load Module with Pluggable PHYs Installed

Part Numbers

The currently available part numbers are shown in *Table 22-1* on page 22-2. Items without a *Price List Names* entry are no longer available.

Table 22-1. Currently Available ATM/POS Modules

Load Module	Part Number	Description
LM622MR	LM622MR	2-port ATM/Packet over SONET Load Module. Supports 622 and 155 Mbps data rates. Requires the purchase of 2 PHY modules (OC3OC12PHY or OC3OC12PHY-SFP) and the OPTATMMR and/or OPTPOSMR operational mode option.
LM622MR-512	LM622MR-512	2-port ATM/Packet over SONET Load Module. Supports 622 and 155 Mbps data rates. Requires the purchase of 2 PHY modules (OC3OC12PHY or OC3OC12PHY-SFP) and the OPTATMMR and/or OPTPOSMR operational mode option.
	OPTATMMR	ATM operational mode option for LM622MR.

Table 22-1. Currently Available ATM/POS Modules

Load Module	Part Number	Description
	OPTPOSMR	OC12c/OC3c Packet over SONET (POS) operational mode option for LM622MR.
	OC3OC12PHY	Single-port OC-3/OC-12 PHY module for the ATM/Packet over SONET Load Module. 1310 nm multimode optics with dual SC connectors.
	OC3OC12PHY-SFP	Single-port OC-3/OC-12 PHY module for the ATM/Packet over SONET Load Module. Requires one SFP pluggable transceiver (not included).
	SFP-OC12MM1310D	Multirate (OC-3, OC-12) SFP transceiver. 1310 nm, multimode with dual LC connectors. Supports diagnostic features.
	SFP-OC12SM1310D	Multirate (OC-3, OC-12) SFP transceiver. 1310 nm, single mode with dual LC connectors. Supports diagnostic features.

OC12 POS 622 Specifications

The OC12c POS specifications for the LM622MR load module are contained in *Table 22-2* on page 22-3.

Table 22-2. OC12c POS Specifications for LM622MR Load Module

	LM622MR	LM622MR-512
# ports	2	2
Data Rate	1-100% of OC12/OC3 speeds	1-100% of OC12/OC3 speeds
Connector	Changeable physical interface (PHY) per port: • SC connectors for 1310 nm multimode • SFP socket for SFP-LC module PHY clock-in and clock-out: • SMA connectors.	Changeable physical interface (PHY) per port: • SC connectors for 1310 nm multimode • SFP socket for SFP-LC module PHY clock-in and clock-out: • SMA connectors.
CPCU RAM	256	512
Capture buffer size	8 MB	8 MB
Captured packet size	34 - 65535 bytes	34 - 65535 bytes
Streams per port	255 Packet Streams	255 Packet Streams
Advanced streams	160	160

Table 22-2. OC12c POS Specifications for LM622MR Load Module

	LM622MR	LM622MR-512
Frame size: min-max	35 - 65536 bytes (at full line rate) 12 - 65536 bytes (otherwise)	35 - 65536 bytes (at full line rate) 12 - 65536 bytes (otherwise)
Inter-frame gap: min-max	1 μs - 4.294967 secs	1 μs - 4.294967 secs
Inter-burst gap: min-max	1 μs - 4.294967 secs	1 μs - 4.294967 secs
Inter-stream gap: min-max	1 μs - 4.294967 secs	1 μs - 4.294967 secs
Latency	20 ns resolution Minimum frame size of 33 bytes is required.	20 ns resolution Minimum frame size of 33 bytes is required.

ATM Specifications

The ATM load module specifications for the LM622MR are contained in *Table 22-3* on page 22-5.

Table 22-3. ATM Load Module Specifications

	LM622MR/LM622MR-512
# ports	2
Data Rate	0-100% of OC-12/OC-3 speeds
Connector	Changeable physical interface (PHY) per port: • SC connectors for 1310 nm multimode • SFP socket for SFP-LC module PHY clock-in and clock-out: • SMA connectors.
Capture buffer size	8 MB
Captured packet size	49 - 64K bytes (Note 1)
Streams per port	4096 shared by 15 interleaved transmit engines
Frame size: min-max	40 - 65,536 bytes (Note 1)
Latency	20 ns resolution

(Note 1) ATM ports transmits a packet of 65568 bytes, including the header. The receive buffer, however, is restricted to 65536 bytes. The last 32 bytes of a maximum size packet is not visible in the capture buffer.

ATM related specifications are detailed in Table 22-4 on page 22-5.

Table 22-4. ATM Specifications

Parameter	Specification
Encapsulation	• LLC/SNAP Routed Protocol • LLC/NLPID Routed Protocol • LLC Bridged Ethernet/802.3 • LLC Bridged Ethernet/802.3 without FCS • LLC Encapsulated PPP • VC Mux Routed Protocol • VC Mux Bridged Ethernet/802.3 • VC Mux Bridged Ethernet/802.3 without FCS • VC Multiplexed PPP
Virtual Circuits	65,536 VC ids distributed among 4,096 unique streams
Cell Header Format	UNI or NNI per port
ATM Framing	AAL5, Constant Bit Rate (CBR) or Unspecified Bit Rate (UBR)

Physical Interfaces

Two pluggable physical interfaces are available for the ATM card:

- **OC3OC12PHY**: Single OC3/OC12 port module. 1310 nm multimode optics with dual-SC connectors. This module is shown in Figure 22-2 on page 22-6. The optical characteristics are expressed in Table 22-5 on page 22-7.

Figure 22-2. OC3OC12PHY Physical Interface

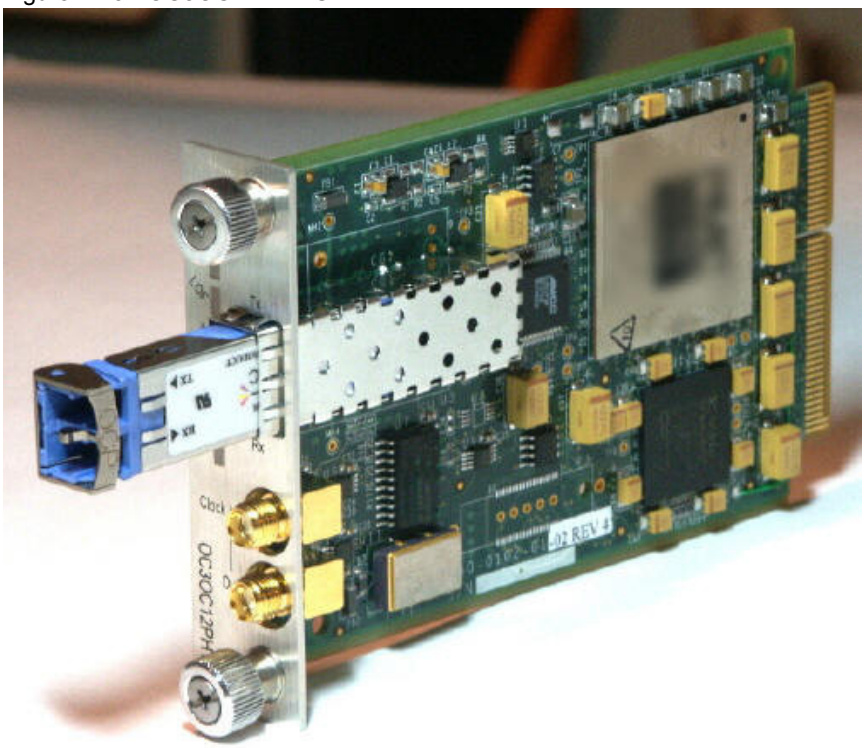
Table 22-5. OC3OC12PHY Optical Specifications

Transmitter/Receiver	Specification	OC12/OC3 Multimode
Transmitter	Fiber	62.5um fiber
	Wavelength	1270nm - 1380nm
	Mean Launched Power	-20dBm to -14dBm
	Minimum Extinction Ratio	10dB
	Safety	LED based
Receiver	Fiber	62.5um fiber
	Wavelength	1100nm - 1600 nm
	Minimum Sensitivity (OC12)	-26dBm
	Minimum Sensitivity (OC3)	-30dBm
	Minimum Overload	-14dBm

- **OC3OC12PHY-SFP**: Single OC3/OC12 port module. The PHY accommodates a SFP transceiver, which is not included with this part. Ixia offers two transceivers:
  - **SFP-OC12MM1310D**: 1310nm multimode transceiver.
  - **SFP-OC12SM1310D**: 1310nm singlemode transceiver.

  Figure 22-3 on page 22-8 shows an OC3OC12PHY-SFP with a transceiver partially inserted.

Figure 22-3. OC3OC12PHY-SFP



The optical characteristics for the two available transceivers are expressed in Table 22-6 on page 22-8.

Table 22-6. SFP-OC12xx1310 Optical Specifications

Specification	SFP-OC12MM1310D (62.5um fiber)	SFP-OC12SM1310D (short reach)
Transmit Center Wavelength—Min/Max	1270 nm/1380 nm	1260 nm/1360 nm
Mean Launched Power—Min/Max	-20 dBm/-14 dBm	-15 dBm/-8 dBm
Minimum Extinction Ratio	10dB	8.2dB
Safety	LED based	Laser based
Receive Wavelength	1100nm - 1600nm	1100nm - 1600nm
Minimum Sensitivity (OC12)	-26dBm	-23dBm
Minimum Sensitivity (OC3)	-30dBm	-8dBm
Minimum Overload	-14dBm	
Dispersion (OC12)		13ps/nm
Dispersion (OC3)		18ps/nm

The clock-in/clock-out signal characteristics on both PHYs are described in Table 22-7 on page 22-9 and Table 22-8 on page 22-9.

Table 22-7. Clock Input Electrical Interface Parameters

Parameter	Characteristic
Connector	Female SMA
Impedance	50 ohm ± 5%, AC coupled
Absolute max input	6V (DC plus half AC peak-to-peak)
Frequency (OC12)	77.76 MHz
Frequency tolerance	+/- 20ppm
Duty Cycle	40/60% of UI
Jitter limits	(12kHz to 5MHz) 12 ps rms

Table 22-8. Clock Output Electrical Interface Parameters

Parameter	Characteristic
Connector	Female SMA
Impedance	50 ohm ± 5%, AC coupled
Amplitude	1.3 Vpp minimum, into 50 Ω. (1.5 Vpp typical)
Edge rates	200ps to 340ps (20% to 80%) into 50Ω
Duty cycle	45% to 55%
Jitter	20ps max cycle to cycle, >1kHz
Frequency (OC12)	77.76 MHz (internal clock mode)
Frequency (OC3)	19.44 MHz (internal clock mode)

Port LEDs

Each OC12c/OC3c port incorporates a set of 6 LEDs, as described in *Table 22-9* on page 22-9.

Table 22-9. LMOC12c Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal and green otherwise.
LOF	Red during Loss of Frame and green otherwise.
Tx	Green while data is transmitted and blank otherwise.
Rx	Green while data is received and blank otherwise.
Err	Red on any receive error and blank otherwise.
Trig	Blank—reserved for future use.

Statistics

Statistics for ATM/POS cards, under various modes of operation, may be found in *Table B-26* on page B-145.

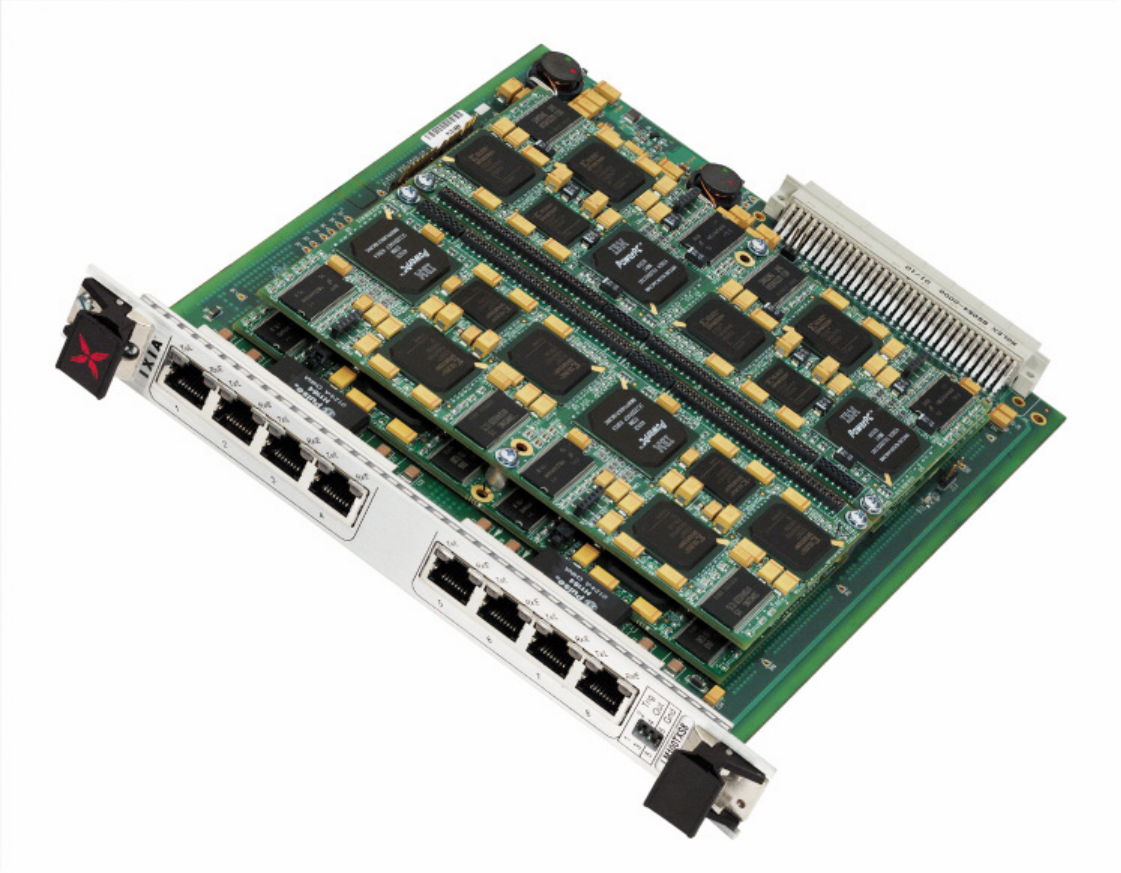
23 IXIA 10/100 Load Modules

This chapter provides details about 10/100 family of load modules—specifications and features.

The 10/100 family of load modules implements Ethernet interfaces that may run at 10Mbps or 100Mbps. Different numbers of ports and interfaces are available for the different board types. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the family's modules (the LM100TXS8) is shown in *Figure 23-1* on page 23-2.

Figure 23-1. LM100TXS8 Load Module



Part Numbers

The part numbers are shown in *Table 23-1* on page 23-2. Items without a *Price List Names* entry are no longer available.

Table 23-1. Part Numbers for 10/100 Modules

Load Module	Price List Names	Description
LM100TX	LM100TX	4-port multilayer 10/100Mbps Ethernet
LM100TX8	LM100TX8	8-port 10/100Mbps Ethernet, reduced features; no support for routing protocols, Linux SDK or L4-L7 applications.
LM100TXS8	LM100TXS8	8-port multilayer 10/100Mbps Ethernet
LM100MII		2-port multilayer 10/100Mbps MII Ethernet
LM100RMII		4-port multilayer 10/100Mbps Reduced MII Ethernet

Specifications

The load module specifications are contained in *Table 23-2* on page 23-3. The limitations of -3, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 23-2. 10/100 Load Module Specifications

	LM100TXS8 LM100TX8	LM100TX	LM100MII	LM100RMII
# ports	8	4 (LM100TX)	2	4
-3 Card Available?	N	N	N	N
L2/L3 Card Available?	Y (LM100TX8)	N	N	N
Layer 7 Card Available	N	N	N	N
Data Rate	10/100 Mbps	10/100 Mbps	10/100 Mbps	10/100 Mbps
Connector	RJ-45	RJ-45	MII[1]	RMII[2]
Interfaces	100Base-TX 10Base-T	100Base-TX 10Base-T		
Capture buffer size	6MB	2MB	2MB	2MB
Captured packet size	12-13k bytes	12-64k bytes	12-64k bytes	12-64k bytes
Streams per port	255	255	255	255
Flows per port	N/A	15872	15872	15872
Advanced Streams	128	N/A	N/A	N/A
Preamble size: min-max	2-63 bytes	2-254 bytes	2-254 bytes	2-254 bytes
Frame size: min-max	12-13k bytes	12-64k bytes	12-64k bytes	12-64k bytes
Inter-frame gap: min-max	**Basic scheduler:** 10Mbps: 8000ns-429s in 400ns steps 100Mbps: 800ns-42.9s in 40ns steps **Advanced scheduler:** 10Mbps: 8000ns-53s in 400ns steps 100Mbps: 800ns-5.3s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps
Inter-burst gap: min-max	10Mbps: 8000ns-429s in 400ns steps 100Mbps: 800ns-42.9s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps

Table 23-2. 10/100 Load Module Specifications

	LM100TXS8 LM100TX8	LM100TX	LM100MII	LM100RMII
Inter-stream gap: min-max	10Mbps: 8000ns-429s in 400ns steps 100Mbps: 800ns-42.9s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps	10Mbps: 800ns-1717s in 400ns steps 100Mbps: 160ns-171s in 40ns steps
Normal stream min frame rate	10: 0.00238fps 100: 0.0238fps			
Advanced stream min frame rate[3]	10 slow: 0.0186fps 10 fast: 9.53 fps 100 slow: 0.186fps 100 fast: 95.3fps			
Latency	20ns resolution	20ns resolution	20ns resolution	20ns resolution

1. AMPLIMITE Subminiature D connector 787170-4.
2. AMPLIMITE Subminiature D connector 787170-7.
3. Streams are divided up into tree categories: 112 slow speed streams and 16 fast streams.

Port LEDs

Each LM100TXS8 port incorporates a set of 2 LEDs, as described in *Table 23-4* on page 23-5.

Table 23-3. LM100TXS8 Port LEDs

LED	Color	Usage
Tx/L	Orange	10Mbps link. Pulses on activity.
	Green	100Mbps link. Pulses on activity.
RX/E	Orange	Pulses on error.
	Green	Full duplex. Pulse on activity.

All other 10/100 card types incorporate a set of 6 LEDs, as described in *Table 23-4* on page 23-5.

Table 23-4. 10/100 Port LEDs

LED Label	Usage
Link	Green if link established. For Mii and RMii boards, Red if no transceiver is detected.
100	Green for 100Mbps.
Half	Green for half duplex operation.
Tx/Coll	Green during data transmission. Red during collisions.
Rx/Err	Green during error free reception. Red if errors received.
Trig	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Trigger Out Values

The signals available on the trigger out pins for all cards in this category are described in *Table 23-5* on page 23-5. The LM100TXS8 and LM100TX8 cards output 60ns pulses and all other cards output 40ns pulses.

Table 23-5. 10/100 Trigger Out Signals

Pin	Signal
1	Port 1: High pulse for each packet matching User Defined Statistic 1
2	Port 2: High pulse for each packet matching User Defined Statistic 1
3	Port 3: High pulse for each packet matching User Defined Statistic 1
4	Port 4: High pulse for each packet matching User Defined Statistic 1

The signals available on the trigger out pins for the LM1000SFPS4 cards is described in *Table 23-6*.

Table 23-6. LM1000SFPS4 Trigger Out Signals

Pin	Signal
1	660ns negative pulse when User Defined Statistic 1 is true.
2	660ns negative pulse when User Defined Statistic 1 is true.
3	660ns negative pulse when User Defined Statistic 1 is true.
4	660ns negative pulse when User Defined Statistic 1 is true.
5	Ground
6	Ground

Statistics

Statistics for 10/100 cards, for various modes of operation may be found in *Table B-8* on page B-35 and *Table B-9* on page B-37.

24 IXIA 100 Load Modules

This chapter provides details about 100 family of load modules—specifications and features.

The 100 family of load modules implements Ethernet interfaces that may run at 100Mbps. Different numbers of ports and interfaces are available for the different board types. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the modules in this family (the LM100FX) is shown in *Figure 24-1* on page 24-2. The face plate for the same module is shown in *Figure 24-2* on page 24-2.

Figure 24-1. LM100FX Load Module

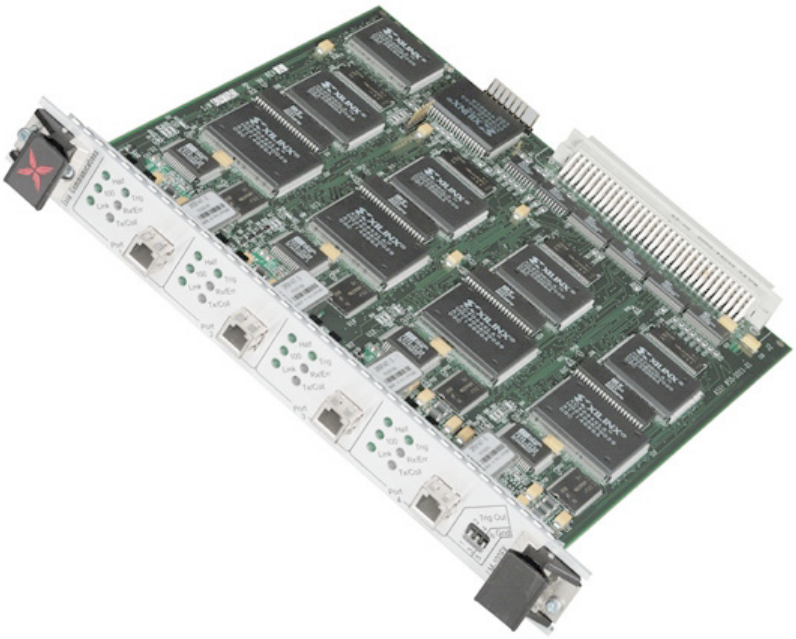


Figure 24-2. LM100FX Face Plate

Part Numbers

The part numbers are shown in *Table 24-1* on page 24-3. Items without a *Price List Names* entry are no longer available.

Table 24-1. Part Numbers for 100Mbps Modules

Load Module	Price List Names	Description
LM100FX		4-port multilayer multimode FX Ethernet.
LM100FXSM		4-port multilayer singlemode FX Ethernet.

Specifications

The load module specifications are contained in *Table 24-3* on page 24-5. The limitations of -3, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 24-2. 100 Load Module Specifications

	LM100FX	LM100FXSM
# ports	4	4
-3 Card Available	N	N
Layer2/Layer3 Card Available?	N	N
Layer 7 Card Available	N	N
Data Rate	100 Mbps	100 Mbps
Connector	MT-RJ (Multimode)	MT-RJ (Singlemode)
Interfaces	100Base-X (multimode)	100Base-X (single mode)
Capture buffer size	2MB	2MB
Captured packet size	12-64k bytes	12-64k bytes
Streams per port	255	255
Flows per port	15872	15872
Preamble size: min-max	2-254 bytes	2-254 bytes
Frame size: min-max	12-64k bytes	12-64k bytes
Inter-frame gap: min-max	100Mbps: 160ns-171s in 40ns steps	100Mbps: 160ns-171s in 40ns steps
Inter-burst gap: min-max	100Mbps: 160ns-171s in 40ns steps	100Mbps: 160ns-171s in 40ns steps

Table 24-2. 100 Load Module Specifications

	LM100FX	LM100FXSM
Inter-stream gap: min-max	100Mbps: 160ns-171s in 40ns steps	100Mbps: 160ns-171s in 40ns steps
Latency	20ns resolution	20ns resolution

Port LEDs

Each 100 port incorporates a set of 6 LEDs, as described in Table 24-3 on page 24-5.

Table 24-3. 100 Port LEDs

LED Label	Usage
Link	Green if link established. For Mii and RMii boards, Red if no transceiver is detected.
100 Mbps	Green for 100Mbps.
Half	Green for half duplex operation.
Tx/Col	Green during data transmission. Red during collisions.
Rx/Err	Green during error free reception. Red if errors received.
Trig	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Trigger Out Values

The signals available on the trigger out pins for all cards in this category are described in *Table 24-4* on page 24-5.

Table 24-4. 100 Trigger Out Signals

Pin	Signal
1	Port 1: 40 ns high pulse for each packet matching User Defined Statistic 1
2	Port 2: 40 ns high pulse for each packet matching User Defined Statistic 1
3	Port 3: 40 ns high pulse for each packet matching User Defined Statistic 1
4	Port 4: 40 ns high pulse for each packet matching User Defined Statistic 1

Statistics

Statistics for 100Mbps cards, under various modes of operation may be found in *Table B-8* on page B-35.

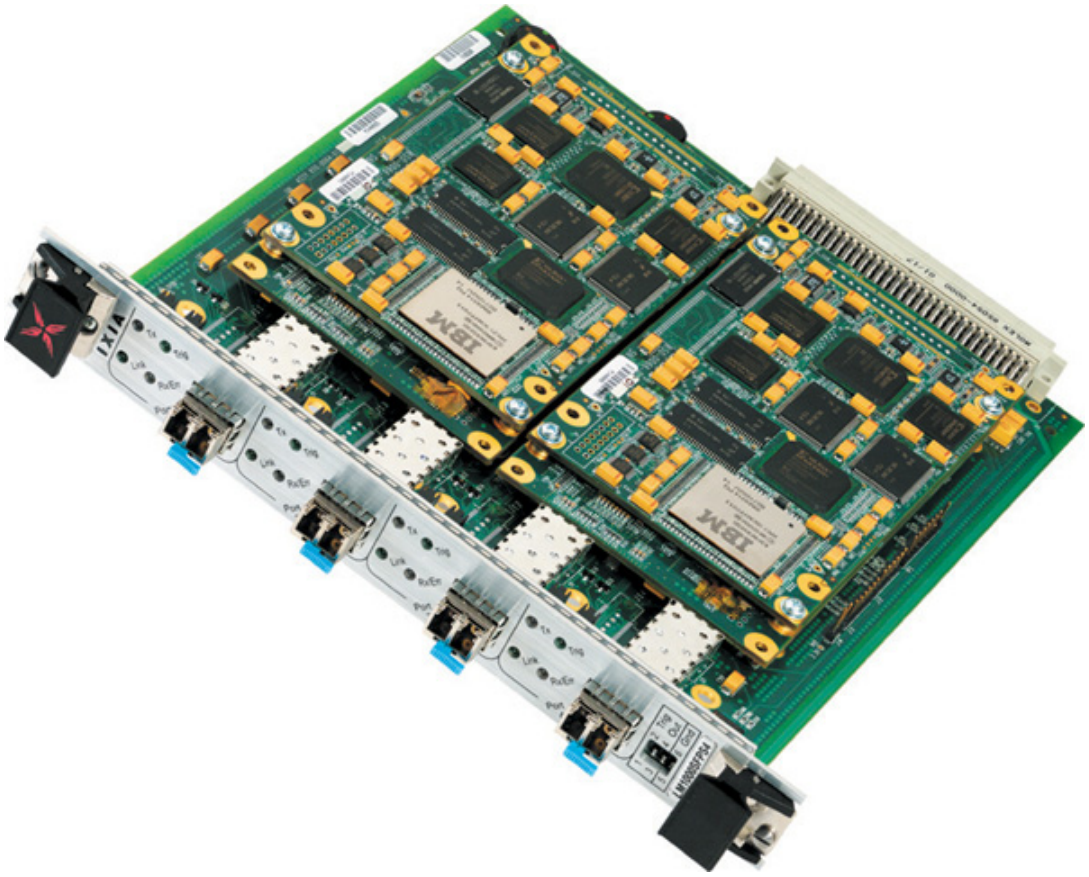
25 IXIA Gigabit Load Modules

This chapter provides details about Gigabit family of load modules—specifications and features.

The Gigabit family of load modules implements copper and fiber Ethernet interfaces that may run at 1000Mbps. Different numbers of ports and interfaces are available for the different board types. The features available for these modules are included in the *Port Features by Port Type* matrix, which is located on the
ixiacom.com website under Support/User Guides/Spreadsheets.

One of the modules in this family, the LM1000SFPS4, is shown in *Figure 25-1*.

Figure 25-1. LM1000SFPS4 Load Module



Part Numbers

The currently available part numbers are shown in *Table 25-1*. Items without a *Price List Names* entry are no longer available.

Table 25-1. Part Numbers for Gigabit Modules

Load Module	Price List Names	Description
LM1000GBIC		2-port multilayer Gigabit GBIC Ethernet; transceivers not included.
		2-port multilayer Gigabit GBIC Ethernet; with 2 multimode GBIC transceivers.
		2-port multilayer Gigabit GBIC Ethernet; with 2 singlemode GBIC transceivers.
		2-port multilayer Gigabit GBIC Ethernet; with 2 multimode and 2 singlemode GBIC transceivers.

Table 25-1. Part Numbers for Gigabit Modules

Load Module	Price List Names	Description
LM1000SFPS4	LM1000SFPS4	4-port Gigabit Ethernet fiber; SFP transceiver not included.
	SFP-LX	1310nm LX SFP transceiver used with LM1000SFPS4 .
	SFP-SX	850nm SX SFP transceiver used with LM1000SFPS4

Specifications

The load module specifications are contained in *Table 25-3* on page 25-5. The limitations of -3, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 25-2. Gigabit Load Module Specifications

	LM1000GBIC	LM1000SFPS4
# ports	2	4
-3 Card Available	N	N
Layer2/Layer3 Card Available?	N	N
Data Rate	1000 Mbps[1]	1000 Mbps
Connector	SX, SX3: SC Multimode LX: SC Singlemode GBIC: GBIC single and/or multimode	SFP or MT-45.[2]
Interfaces	1000Base-X	1000Base-X
Capture buffer size	4MB	8MB
Captured packet size	12-64k bytes	12-13k
Streams per port	255	255
Advanced streams per port	N/A	256
Flows per port	15872	N/A
Preamble size: min-max	6-254 bytes	8-61 bytes
Frame size: min-max	48-64k bytes	12-13k bytes
Inter-frame gap: min-max	64ns-68sec in 16ns steps	**Basic scheduler:** 64ns-4.29s in 16ns steps **Advanced scheduler:** 64ns-0.53s in 16ns steps
Inter-burst gap: min-max	96ns-68sec in 16ns steps	64ns-16.7ms in 16ns steps
Inter-stream gap: min-max	96ns-68sec in 16ns steps	64ns-4.29ms in 16ns steps
Normal stream min frame rate		0.238fps
Advanced stream min frame rate[3]		slow: 1.86fps fast 953fps
Latency	20ns resolution	20ns resolution

Table 25-2. Gigabit Load Module Specifications

	LM1000GBIC	LM1000SFPS4
Max Value List Entries	N/A	48K
Max Range List Entries[4]	N/A	6K

1. Odd frame sizes can cause diminishment in actual data rates on gigabit modules.
2. LC connector is built-in, SFP connection requires either SFP-SX (850nm SX) or SFP-LX (1310nm LX) module purchased from Ixia, or separately supplied.
3. Streams are divided up into tree categories: 112 slow speed streams and 16 fast streams.
4. 192k memory is shared between value list entries (at 4 bytes per entry) and range list entries (at 32 bytes per entry).

Note: A special capability of Gigabit modules is the ability to echo all received packets back out to the network. This feature should never be used in a live network, as it is likely crash the network.

Port LEDs

Each Gigabit port incorporates a set of LEDs, as described in *Table 25-3* on page 25-5.

Table 25-3. Gigabit Port LEDs

LED Label	Usage
Link	Green if link established.
Line	Green if an alignment, disparity, or symbol error has been detected. (Not available on the LM1000SFPS4.)
Half	Green for half duplex operation. (Not available on the LM1000SFPS4.)
Tx/Coll	Green during data transmission. Red during collisions.
Rx/Err	Green during error free reception. Red if errors received.
Trig	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Each LM1000SFPS4 port incorporates a set of 6 LEDs, as described in Table 25-4 on page 25-5.

Table 25-4. 10/100/1000 Port LEDs for LM1000TXS4

LED Label	Usage
Link	Green for 1000 Mbps link, orange for 100 Mbps link, yellow for 10 Mbps link and off for no link.
Tx/Col	Green during data transmission and red during collisions.

Table 25-4. 10/100/1000 Port LEDs for LM1000TXS4

LED Label	Usage
Rx/Err	Green during error free reception and red if errors are received.
Trigger	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Trigger Out Values

The signals on the trigger out pins for cards in this category are described in *Table 25-5* on page 25-7.

Table 25-5. Gigabit Trigger Out Signals

Pin	Signal
1	Port 1-10 ns high pulse for each packet matching User Defined Statistic 1
2	Port 2-10 ns high pulse for each packet matching User Defined Statistic 1
3	Port Z-low during transmit of frame, otherwise high
4	Port 2-low during transmit of frame, otherwise high

The LM1000SFPS4 sends a 660ns negative pulse when user defined statistic 1 is true.

Statistics

Statistics for Gigabit cards, under various modes of operation may be found in *Table B-8* on page B-35 and *Table B-12* on page B-48.

26 IXIA OC12c/OC3c Load Modules

This chapter provides details about OC12c/OC3c family of load modules—specifications and features.

The OC12c/OC3c family of load modules implements Optical Carrier interfaces that may run at OC12 or OC3 speeds. Both interfaces operate in concatenated mode, as opposed to channelized mode. Different numbers of ports and interfaces are available for the different board types. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the modules in this family, the LMOC12c, is shown in the following figure.

Figure 26-1. LMOC12c Load Module

Part Numbers

The part numbers are shown in the following figure. Items without a *Price List Names* entry are no longer available.

Table 26-1. Part Numbers for OC12c/OC3c Modules

Load Module	Price List Names	Description
LMOC12c/ LMOC3c	LMOC12c	2-port multilayer OC12c/OC3c SR-1 POS/SDH, 1310nm multimode
	LMOC12cSM	2-port multilayer OC12c/OC3c SR-1 POS/SDH, 1310nm singlemode

Specifications

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3 and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 26-2. OC12c/OC3c Load Module Specifications

	LMOC12c LMOC12cSM
# ports	2
-3 Card Available	N
Layer2/Layer3 Card Available?	N
Layer 7 Card Available	N
Data Rate	1-100% of OC12/OC3 speeds (See note 3)
Connector	SC-Singlemode or Multimode
Capture buffer size	16MB
Captured packet size	OC3: 49 - 5,120 bytes OC12: 49 - 15,500 bytes (See note 1)
Streams per port	255
Flows per port	N/A
Preamble Size: min-max	N/A
Frame size (transmit): min-max	34-65,536 bytes (See note 4)
Frame size (receive): min-max	12-65,536 bytes (See note 5)
Inter-frame gap: min-max	N/A
Inter-burst gap: min-max	1μs - 85secs
Inter-stream gap: min-max	1μs - 85secs
Latency	20ns resolution (See note 2)

1. Captured Packet Size Note: At 100% line rate. Smaller values are possible at lower line rates.
2. Requires that packets be larger than 70 bytes when operating at full line rate.

3. Correct data rates can only be maintained with a minimum number of packets, depending on packet size. For OC12 operation, the numbers of packets are required for the indicated ranges of packet sizes:

Table 26-3. OC12 Minimum Number of Packets

Packet Size	Minimum Number of Packets per Stream
45 or less	30
46 - 47	8
48 - 54	7
55 - 63	6
64 - 84	5
85 - 129	4
130 - 199	3
200 - 499	2
500+	0

For OC3 operation, the numbers of packets are required for the indicated ranges of packet sizes:

Table 26-4. OC3 Minimum Number of Packets

Packet Size	Minimum Number of Packets per Stream
34 or less	4
35 - 64	3
65 - 274	2
275+	0

4. The maximum frame size depends on the type of header and PPP negotiation. The maximum frame size is 64k bytes although beyond 8192 bytes, the data is repeated.

5. 12 byte frames cannot be received back-to-back. A 34 byte frame is required to receive back-to-back frames.

Port LEDs

Each OC12c/OC3c port incorporates a set of 4 or 6 LEDs, as described in the following table.

Table 26-5. LMOC12c Port LEDs

LED Label	Usage
LOS	Red during Loss of Signal.
LOF	Red during Loss of Frame.

Table 26-5. LMOC12c Port LEDs

LED Label	Usage
Error	Red on any POS error.
Tx	Green while data is transmitted.
Rx	Green while data is received.
Trig	Follows the state of the *Trigger Out* pin.

Trigger Out Values

The signals available on the trigger out pins for all cards in this category are described in the following table.

Table 26-6. OC12c/OC3c Trigger Out Signals

Pin	Signal
1	Port 1: 10 ns high pulse for each packet matching User Defined Statistic 1
2	Port 2: 10 ns high pulse for each packet matching User Defined Statistic 1
3	Port 1: Low during transmit of frame, otherwise high
4	Port 2: Low during transmit of frame, otherwise high

Optical Specifications

The optical characteristics for the OC12c/OC3c cards are described in the following table.

Table 26-7. LMOC12c Optical Specifications

Specification	OC12c/OC3c Multimode	OC12c/OC3c Singlemode
Average Output Power–Minimum/ Maximum	-19 dBM/-14 dBM	-15 dBM/-8 dBM
Transmit Center Wavelength–Minimum/Maximum	1270 nm/1380 nm	1293 nm/1310 nm
Receive Center Wavelength–Minimum/Maximum	1270 nm/1380 nm	1200 nm/1550 nm
Receive Sensitive–Minimum/ Maximum	-26 dBM/-14 dBM	-28 dBM/-5 dBM
Safety	Led based	Class 1 Laser

Statistics

Statistics for OC12c cards, under various modes of operation may be found in *Table B-13* on page B-51.

27 IXIA OC48c Load Modules

This chapter provides details about OC48c family of load modules—specifications and features.

The OC48c family of load modules implements Optical Carrier interfaces that runs at OC48 speeds. The interface operates in concatenated mode, as opposed to channelized mode. Cards are available that perform Packet Over SONET testing, Bit Error Rate Testing or both. The features available for these load modules are included in the *Port Features by Port Type* matrix, which is located on the ixiacom.com website under Support/User Guides/Spreadsheets.

One of the modules in this family, the LMOC48c, is shown in the following figure.

Figure 27-1. LMOC48c Load Module

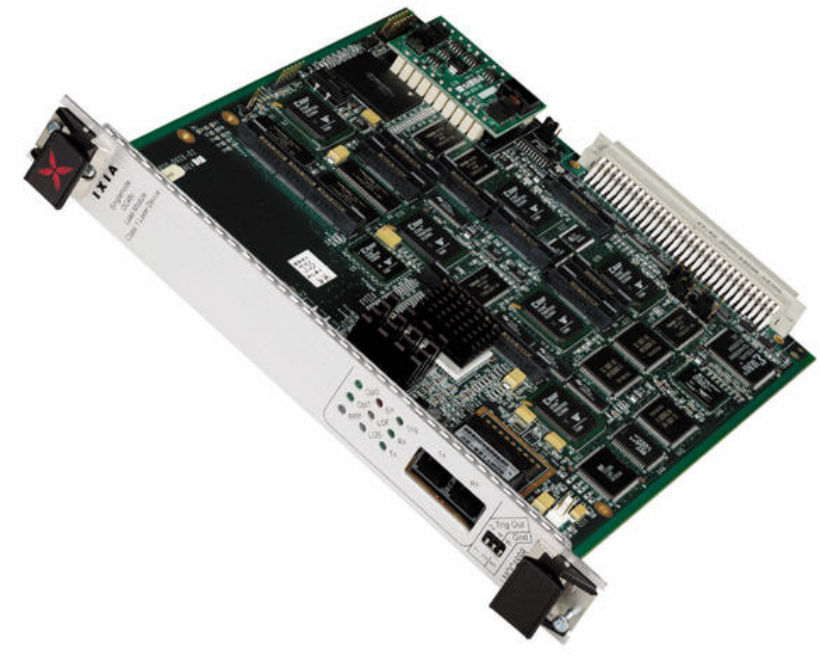


Figure 27-2. MSM2.5G1-01 Load Module

Part Numbers

The part numbers are shown in the following figure. Items without a *Price List Names* entry are no longer available.

Table 27-1. Part Numbers for OC48 Modules

Load Module	Part Numbers	Description
LMOC48cPOS	LMOC48C	1-port multilayer OC48cSR-1 POS/SDH, 1310nm, singlemode
LMOC48cPOS-M	LMOC48C3	1-port multilayer OC48cSR-1 POS/SDH, 1310nm, singlemode, manufacturing version
LMOC48cBERT	LMOC48311	1-port multilayer OC48cSR-1 SONET/ BERT, 1310nm, singlemode
	LMOC48312	1-port multilayer OC48cIR-2 SONET/ BERT, 1550nm, singlemode

Table 27-1. Part Numbers for OC48 Modules

Load Module	Part Numbers	Description
LMOC48cPOS/ BERT	LMOC48411	1-port multilayer OC48cSR-1 POS/BERT, 1310nm, singlemode
	LMOC48412	1-port multilayer OC48cIR-2 POS/BERT, 1550nm, singlemode
2.5G MSM POS	MSM2.5G1-01	1-port multilayer OC48cSR-1 POS/SDH, 1310nm, singlemode
SW-DCCSONET		DCC SONET support for all modules.
		SRP SONET support for all modules.
SW-SRPSONET SW-RPRSONET	945-0002	SRP SONET and RPR SONET support for all modules
SW-VCAT-SONET	945-0005	SONET Virtual Concatenation (VCAT) option

Specifications

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 27-2. OC48 Load Module Specifications

	LMOC48c	LMOC48cBERT LMOC48cBERTRx	LMOC48c POS+ BERT[1]	2.5G MSM POS[2]
# ports	1	1	1	1
-3/-M Card Available	Y	N	N	N
Layer2/Layer3 Card Available?	N	N/A	N	Y
Layer 7 Card Available	N	N/A	N	N
Data Rate	1-100% of OC48 speeds	2.488 Gbps		1-100% of OC48 speeds
Connector/ Wavelength-Mode	SC/1310nm or 1550nm Singlemode	SC/1310nm Singlemode		SFP/1310nm or 1550nm Singlemode
Capture buffer size	32MB	N/A		Up to 384 MB
Captured packet size	26-65,535 bytes	N/A		17-65,535 bytes

Table 27-2. OC48 Load Module Specifications

	LMOC48c	LMOC48cBERT LMOC48cBERTRx	LMOC48c POS+ BERT[1]	2.5G MSM POS[2]
Streams per port	255	N/A		256
Flows per port	N/A	N/A		N/A
Advanced Streams	160			256
Preamble size: min-max	N/A	N/A		N/A
Frame size: min-max	26-65,535	N/A		25-65,535
Inter-frame gap: min-max	N/A	N/A		4.0ns - 42sec in 3.2ns steps
Inter-burst gap: min-max	1µs - 42secs	N/A		4.0ns - 42sec in 10.0ns steps
Inter-stream gap: min-max	1µs - 42secs	N/A		4.0ns - 42sec in 10.0ns steps
Normal stream frame rate	0.023fps - full line rate			0.023fps - full line rate
Advanced streams frame rate[3]	Slow: 0.023 - 2083333 fps Med: 95fps - full line rate Fast: 1525fps - full line rate			Slow: 0.023fps Fast: 1525fps
Latency	20ns resolution	N/A		20ns resolution

1. Refer to the LMOC48cPOS and LMOC48cBERT columns for the characteristics of this card when its port is in POS or BERT mode, respectively.
2. Due to power requirements, only one 2.5G MSM POS module can be used in a 250 or 400T chassis. Other modules can be used with the 2.5G MSM POS in the same chassis, but only one 2.5G MSM POS at a time (excepting MSM family of modules and the CPM1000T8, which have the same limitation).
3. Streams are divided up into three categories: 144 slow speed streams, 8 medium streams, and 8 fast streams (excluding the 2.5G MSM POS load module).

OC48c VAR Calibration

This procedure allows the OC48 VAR module's transmission frequency to be varied to test compliance of devices to the limits of the specification.

Frequency Adjustment

The OC48 VAR allows a variation of +/- 100 parts per million (ppm) from the clock source's nominal frequency, through a DC voltage input into the BNC jack marked 'DC IN' on the front panel. The variation is from the lowest frequency when DC IN is 0 V, to highest frequency when DC IN is 3.3 V. The input voltage should be used only within this range, although the DC IN circuitry is designed to withstand +/- 30 V in the case of accidental overdrive from a function generator. The input has a single-pole low pass at 16 Hz to keep injected noise from causing a violation of OC48 jitter specifications. As a result, the system should be given 50 to 100 milliseconds to settle after a voltage step at DC IN.

Frequency Monitoring

The frequency may be monitored through the BNC marked 'Freq Monitor.' This output provides the OC48 line clock divided by 16. The center frequency is 155.52 MHz. The voltage is 70 mV peak-to-peak into 50 ohms, suitable for direct connection into a frequency counter (such as an HP53181A) through 50 ohm coaxial cable. The frequency counter should be set for 50 ohm termination in a suitably sensitive mode.

Port LEDs

There are two sets of LEDs, one for LMOC-48c load modules and one for MSM OC-48c load modules.

Each OC48c port incorporates a set of LEDs, as described in the following figure.

Table 27-3. LMOC48c Port LEDs

LED Label	Usage
PPP	Green if a PPP link has been established. Red otherwise.
Option 1	Reserved for future use.
Option 2	Reserved for future use.
LOS	Red during Loss of Signal, Green otherwise.
LOF	Red during Loss of Frame, Green otherwise.
Error	Red on any POS error.
Tx	Green while data is transmitted.
Rx	Green while data is received.
Trig	Follows the state of the *Trigger Out* pin, which is programmed through User Defined Statistic 1.

Each 2.5G MSM POS port incorporates a set of LEDs, as described in the following table.

Table 27-4. MSM2.5G1-01 Port LEDs

LED Label	Usage
Trigger	Green if a Trigger A condition occurred, Red if a temperature condition occurred.
Tx	Green if transmit is active and frames are being sent, blank otherwise.
LOS	Green if signal level is good, Red if loss of signal condition is detected, blank if no transceiver is detected.
Error	Red if module is in an error state, blank otherwise.
Rx	Green if valid frames being received, Red if errored frames being received, blank otherwise.
LOF	Green if valid framing exists, Red if loss of frame condition exists.

Trigger Out Values

The signals available on the trigger out pins for legacy OC-48c load modules in this category are described in the following table.

Table 27-5. LMOC48c Trigger Out Signals

Pin	Signal
1	Always high (no trigger available)
2	Always high (no trigger available)
3	Always high (no trigger available)
4	Always high (no trigger available)

The signals available on the trigger out pins for MSM load modules in this category are described in the following table.

Table 27-6. 2.5G MSM POS Trigger Out Signals

Pin/LED	Value
Trigger Out	10nS active high pulse on trigger.
Trigger LED	Indicates Trigger. This triggers on User Defined Statistic 1.

Optical Specifications

The optical characteristics for the OC48c cards are described in the following table.

Table 27-7. LMOC48c Optical Specifications

Specification	OC48c Singlemode
Average Output Power–Minimum/ Maximum	-10 dBM/-3 dBM
Transmit Center Wavelength–Minimum/Maximum	1266 nm/1360 nm
Receive Center Wavelength–Minimum/ Maximum	1260 nm/1580 nm
Receive Sensitive–Minimum/Maximum	-18 dBM/-3 dBM
Safety	Class 1 Laser

Statistics

Statistics for OC48 cards, under various modes of operation may be found in *Table B-14* on page B-57.

28 IXIA FCMGXM Load Modules

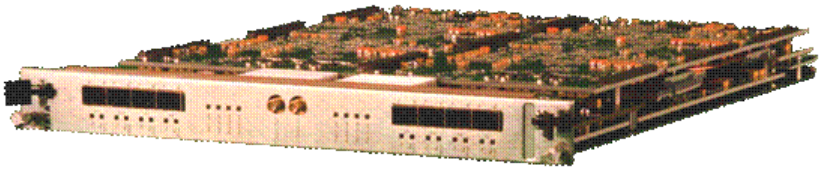
This chapter provides details about FCMGXM family of load modules—specifications and features.

The FCMGXM family of high speed load modules delivers high-density, 2/4/8G fibre channel test solution. These load modules deliver high-density converged data center infrastructure for testing end-to-end Fibre Channel and Fibre Channel over Ethernet (FCoE) testing. The fibre channel load module comes with four or eight ports and each port can be configured to run at 2, 4, or 8 G speeds.

The 4-port and 8-port FCMGXM load modules deliver complete FC-2 and FCP data plane capabilities and performance.

One of the modules in this family, the FCMGXM8, is shown in the following figure.

Figure 28-1. FCMGXM Load Module



Part Numbers

The part numbers are shown in *Table 28-1*.

Table 28-1. Part Numbers for FCMGXM Modules

Load Module	Part Numbers	Description
FCMGXM4	950-0001 FCMGXM4S-01	4-Port Fibre Channel Load Module, with 2 Gbps, 4 Gbps and 8 Gbps support and SFP+ interface. It requires one or more SFP+ transceiver options.
FCMGXM8	950-0002 FCMGXM8S-01	8-Port Fibre Channel Load Module, with 2 Gbps, 4 Gbps and 8 Gbps support and SFP+ interface. It requires one or more SFP+ transceiver options.

Specifications

The load module specifications are contained in *Table 28-2* on page 28-2.

Table 28-2. FCMGXM Load Module Specifications

Feature	Specification
Load Modules	FCMGXM8/FCMGXM4
Number of ports per module	8/4
Number of chassis slots per module	1
Maximum ports per chassis	**Note**: XM12 High Performance chassis is required for 88 ports to be installed in a single chassis. Up to eleven 8-port load modules are supported in an XM12 High Performance chassis, and up to 8 8-port load modules are supported in a standard XM12 chassis. The XM2 chassis supports up to 16 ports.
Supported transceivers	SFP+ Tri-rate 2/4/8G duplex LC connector 850nm multimode 1310 single mode.
Per-port CPU speed and memory	800 MHz, 1 GB/1 GHz, 1 GB.
Per-port capture buffer	512 MB
Interface speeds	2/4/8G FC
FC-1 Primitives	Yes
FC-2 Protocols	Yes

Table 28-2. FCMGXM Load Module Specifications

Feature	Specification
FCP Support	Yes
Number of transmit flows per port (sequential values)	Billions
Number of transmit flows per port (arbitrary values)	1 million
Number of trackable receive flows per port	1 million
Number of stream definitions per port	256 In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows.
Table UDF	1 million entries. Comprehensive packet editing function for emulating large numbers of flows. Entries of up to 256 bytes, using lists of values can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size, and a list of values in a table format.
Packet flow statistics	Tracks 1 million flows.
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
Receive engine	Wire-speed packet filtering, capturing, real-time latency, and inter-arrival time for each packet group, data integrity, and sequence checking.
User defined field features	Fixed, increment, or decrement by user-defined step, value lists, range lists, cascade, random, and chained fields.
Filters	2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, and sequence checking error (small, big, reverse).
Data field per stream	Fixed, increment (byte/word), decrement (byte/word), random, repeating, user-specified, CJPAT, and CRPAT fields.
Error generation	CRC (good/bad), oversize frame, parity error, and R_RDY errors.
Latency measurements	20 nanoseconds resolution in packet timestamp.

Table 28-2. FCMGXM Load Module Specifications

Feature	Specification
Statistics	The new statistics are as follows: • Link State and speed • (Tx) Bytes, Frames, (count and rate) • (Rx) Bytes, Frames, (count and rate) • (Rx) CRC errors, Oversize (2112), Undersize (24) (count and rate) • Packet group Latency • Data Integrity • Capture Trigger/Filter (count and rate) • User Defined Stats: 6 (count and rate) • Protocol Server Tx/Rx (count and rate) • Remote B-B Credit Value • Remote B-B Credit Count • R_RDY Tx/Rx (count and rate) • Disparity errors (count and rate) • Stats: Port CPU status • Transmit Duration • Invalid EOF Count/Rate • Code Error Count/Rate • FLOGI Sent • FLOGI LS_ACC received • FLOGO Sent • PLOGI Sent • PLOGI LS_ACC received • PLOGI Request received • PLOGO Sent • PLOGO Received • FDISC Sent • FDISC LS_ACC Received • NS Registration Sent • NS Registration Successful • NxPort Enabled • NxPort-IDs Acquired • NS Query Sent • NS Query Successful • PRLI Sent • PRLI Successful • PRLI Received • RSCN Received • RSCN Acc Transmitted • SCR Transmitted • SCR Acc Received
Operating temperature range	41°F to 95°F (5°C to 35°C), ambient air.

29 IXIA Xcellon-Flex Load Modules

This chapter provides details about Xcellon-Flex family of load modules—specifications and features.

The Xcellon-Flex family of high speed load modules delivers high-density, high-performance test solutions. Xcellon, the architecture behind these load modules, features aggregation of multi-core CPUs and high memory to meet testing needs for high-scale performance.

The Xcellon-Flex family consists of the following load modules:

- 10GbE Accelerated Performance
- 10GbE Full Emulation
- A 10/40 Gigabit Ethernet Accelerated Performance
- A 40 Gigabit Ethernet Full Emulation

The card names are FlexAP10G16S, FlexFE10G16S, FlexAP1040SQ, and FlexFE40QP.

The Accelerated Performance load module provides architecture for layer 2-7 performance testing, providing ultra-high-scale session and protocol emulation per port. The Full Emulation load module is for layer 2-3 mid-range protocol emulation and scale capacity testing for switches and routers. The Xcellon-Flex Combo 10/40GE Accelerated Performance load module provides both 10GE SFP+ and/or 40GE QSFP+ ports in a single chassis slot. It uses aggregation technology to combine CPU power and memory, and provides ultra-high networking protocol scalability. The 4x40GE Full Emulation load module has a rich layer 2-7 feature set and is well suited for mid-range protocol emulation and scale testing. The load module is ideal for manufacturers of large-port-count, converged data center switches.

The Xcellon-Flex family load module is shown in the following figure:

Figure 29-1. Xcellon-Flex Module-FlexAP10G16S

The Xcellon-Flex family load module is shown in the following figure:

Figure 29-2. Xcellon-Flex Module-FlexFE10G16S

Figure 29-3. Xcellon-Flex Module-FlexAP1040SQ

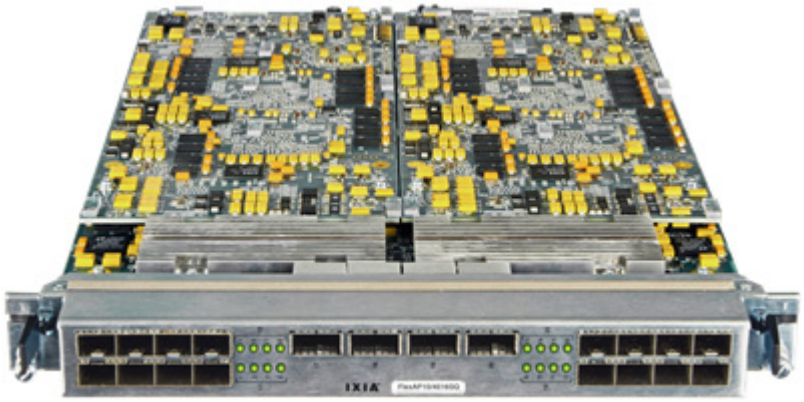
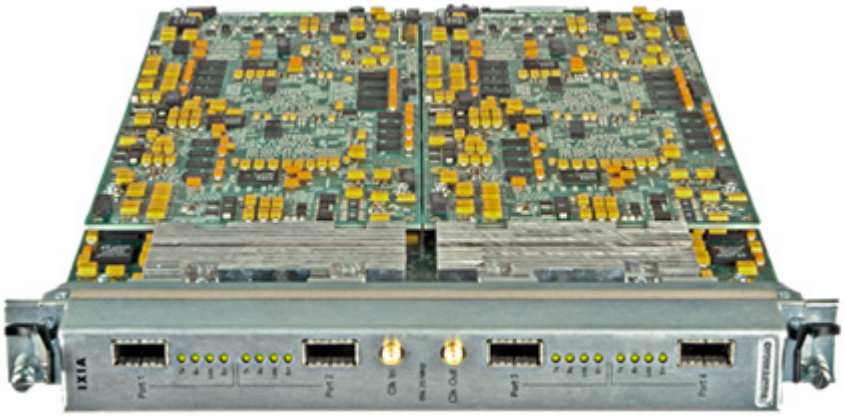


Figure 29-4. Xcellon-Flex Module-FlexFE40QP



Part Numbers

The part numbers are shown in *Table 29-1*.

Table 29-1. Part Numbers for Xcellon-Flex Modules

Model Number	Part Number	Description
FlexAP10G16S	944-1060	10 Gigabit Ethernet Accelerated Performance Load Module, 16-Port LAN, SFP+ interface with full performance L2-L7 support.
FlexFE10G16S	944-1061	10 Gigabit Ethernet Full Emulation Load Module, 16-port LAN, SFP+ interface with L2-3 support.
FlexAP1040SQ	944-1062	10/40 Gigabit Ethernet Accelerated Performance Load Module, 16-Ports of SFP+ interfaces and 4-ports of QSFP+ 40GE interfaces with full performance L2-7 support, for XM12-02 (941-0009) High Performance rackmount chassis and XM2-02 (941-0003) portable chassis, requires one or more SFP+ transceiver options: 10GBASE-SR/SW (948-0013), or 10GBASE-LR/LW (948-0014).
FlexFE40QP	944-1065	40 Gigabit Ethernet Full Emulation Load Module, 4-ports of QSFP+ 40GE with L2-3 support.

Specifications

The load module specifications are contained in *Table 29-2*.

Table 29-2. Xcellon-Flex Load Module Specifications

Feature	Specification
Load Modules	FlexAP10G16S/FlexFE10G16S/ FlexAP1040SQ/FlexFE40QP
Number of ports per module	FlexAP10G16S/FlexFE10G16S: 16 Flex AP1040SQ: 16 ports of SFP+ 10GE and/or 4-ports of QSFP+ 40GE FlexFE40QP: 4-ports of 40GE QSFP+
Number of chassis slots per module	1
Maximum ports per chassis	FlexAP10G16S/FlexFE10G16S: XM12 High Performance: 128 XM2Desktop: 16 **Note**: XM12 High Performance chassis is required for the simultaneous operation of 128 ports in a single chassis. If a standard XM12 chassis (941-0002) is used with these load modules, conversion to the High Performance model is required. A field-replaceable power supply upgrade kit (943-0005) is available for this purpose. When one or more FlexAP10G16S or FlexFE10G16S load modules is installed in an HM12 High Performance chassis, the maximum total number of load modules that may be installed at one time in a single chassis is 8. The XM2 portable chassis (941-0003) supports up to 16 ports (1 load module) of the FlexAP10G16S FlexFE10G16S modules. No other load module is installed in the XM2 chassis when a FlexAP10G16S or FlexFE10G16S load module is installed. FlexAP1040SQ: XM12 High Performance: 96-ports 10GE SFP+ and 24-ports 40GE QSFP XM2Desktop: 16-ports 10GE SFP+ or 4-ports 40GE QSFP FlexFE40QP: XM12 High Performance: 24-ports 40GE QSFP+ XM2Desktop: 4-ports 40GE QSFP+

Table 29-2. Xcellon-Flex Load Module Specifications

Feature	Specification
10GbE Interface protocols	FlexAP10G16S/FlexFE10G16S: 10GbE LAN FlexAP1040SQ/FlexFE40QP: IEEE802.3ae 10GE LAN, IEEE802.3ba 40GBASE-R LAN
Data Center Protocol Upgrades (optional feature)	FCoE, Priority-based Flow Control (IEEE 802.1Qbb) and LLDP/DCBX support FlexFE40QP: Priority-based Flow Control (IEEE 802.1Qbb)
Multi-core processors	Yes
Aggregation capability	FlexAP10G16S/FlexFE10G16S/ FlexAP1040SQ: Yes FlexFE40QP: No
Per-port capture buffer	FlexAP10G16S/FlexFE40QP: 256 MB FlexFE10G16S: 64 MB FlexAP1040SQ: 256MB (10GE), 1GB (40GE)
Layer 2-3 routing protocol emulation	Yes
Layer 4-7 application traffic testing	FlexAP10G16S/FlexAP1040SQ/ FlexFE40QP: Yes FlexFE10G16S: No
Number of transmit flows per port (sequential values)	Billions
Number of transmit flows per port (arbitrary values)	FlexAP10G16S: 1 million FlexFE10G16S: 32 K
Number of transmit flows per port (PGID)	FlexAP1040SQ/FlexFE40QP: 1 million
Trackable receive flows	FlexAP10G16S/FlexAP1040SQ: 1 million FlexFE10G16S/FlexFE40QP: 64 K
Number of stream definitions per port	FlexAP10G16S/FlexAP1040SQ: 512 FlexFE10G16S/FlexFE40QP: 256 In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows. **Note**: In the Data Center mode, the number of transmit streams is 256.

Table 29-2. Xcellon-Flex Load Module Specifications

Feature	Specification
Table UDF	FlexAP10G16S/FlexAP1040SQ/ FlexFE40QP: 1 million entries FlexFE10G16S: 256 K entries Comprehensive packet editing function for emulating large numbers of sophisticated flows. Entries of up to 256 bytes, using lists of values, can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size, and a list of values in a table format.
Packet flow statistics	FlexAP10G16S: 1 million flows FlexFE10G16S: 64 K flows
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures
Receive engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, data integrity, and sequence checking
User defined field features	Fixed, increment or decrement by user defined step, value lists, range lists (supported in all 10 GE mode), cascade, random, and chained
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, and sequence checking error (small, big, reverse)
Data field per stream	Fixed, increment (byte/word), decrement (byte/word), random, repeating, and user-specified
Error generation	FlexAP10G16S/FlexFE10G16S/ FlexAP1040SQ (10GE): CRC (good/bad/none), undersize, oversize FlexAP1040SQ (40GE)/FlexFE40QP: CRC (good/bad), undersize, oversize

Table 29-2. Xcellon-Flex Load Module Specifications

Feature	Specification
Link Fault Signaling	FlexAP10G16S/FlexFE10G16S/ FlexAP1040SQ (10GE): Link state indicator for No Fault, Local Fault, and Remote Fault. FlexAP1040SQ (40GE)/FlexFE40QP: Generate local and remote faults with controls for the number of faults and order of faults, and the ability to select the option to have the transmit port ignore link faults from a remote link partner.
Latency measurements	FlexAP10G16S/FlexFE10G16S/ FlexAP1040SQ (10GE):20 ns resolution in packet timestamp FlexAP1040SQ (40GE)/FlexFE40QP: 2.5 ns resolution in packet timestamp
Latency self-calibration	Ability to calibrate and remove inherent latency
Transmit line clock adjustment	Ability to adjust the parts per million (ppm) line frequency over a range of the following: • LAN mode: +/-100 ppm
IPv4, IPv6, UDP, TCP	Hardware checksum generation and verification
Frame length controls	Fixed, random, weighted random, or increment by user-defined step
Operating temperature range	41°F to 86°F (5°C to 30°C), ambient air **Note**: When an Xcellon-Flex load module is installed in an XM12 chassis, the maximum operating temperature of the chassis is 30°C (86°F) ambient air temperature.
40 GE Physical Coding Sublayer (PCS) test features (for FlexFE40QP)	IEEE 802.3ba compliant PCS transmit and receive side test capabilities
Per PCS lane, transmit lane mapping (for FlexFE40QP)	Supports all combinations of PCS lane mapping: Default, Increment, Decrement, Random, and Custom
Per PCS lane, lane marker, or lane marker and payload error injections (for FlexFE40QP)	Ability to inject errors into the PCS Lane Marker and simultaneously into PCS Lane Marker and Payload fields by the user. This includes the ability to inject sync bit errors into the Lane Marker and Payload. User can control the PCS lane, number or errors, period count and manage the repetition of the injected errors.

Table 29-2. Xcellon-Flex Load Module Specifications

Feature	Specification
Per PCS lane, receive lanes statistics (for FlexFE40QP)	PCS Sync Header and Lane Marker Lock, Lane Marker mapping, Relative lane skew measurement (up to 104 microseconds), Sync Header and PCS Lane Marker Error counters, indicators for Loss of Synch Header and Lane Marker, BIP8 errors.

Table 29-2. Xcellon-Flex Load Module Specifications

Feature	Specification
Statistics	The new statistics are as follows: • Link State • Link Speed • Frames Sent • Valid Frames Received • Bytes Sent • Bytes Received • Fragments • Undersize • Oversize and Good CRCs • CRC Errors • Vlan Tagged Frames • Flow Control Frames Received • Oversize and CRC Errors • User Defined Stat 1 • User Defined Stat 2 • Capture Trigger (UDS 3) • Capture Filter (UDS 4) • User Defined Stat 5 • User Defined Stat 6 • ProtocolServer Receive • Transmit Arp Reply • Transmit Arp Request • Transmit Ping Reply • Transmit Ping Request • Receive Arp Reply • Receive Arp Request • Receive Ping Reply • Receive Ping Request • IPv4 Packets Received • UDP Packets Received • TCP Packets Received • IPv4 Checksum Errors • UDP Checksum Errors • TCP Checksum Errors • Transmit Duration • Protocol Server Vlan Dropped Frames • Scheduled Frames Sent • Asynchronous Frames Sent • Port CPU Frames Sent • Link Fault State • Scheduled Transmit Duration • Bytes Sent/Transmit Duration

Table 29-2. Xcellon-Flex Load Module Specifications

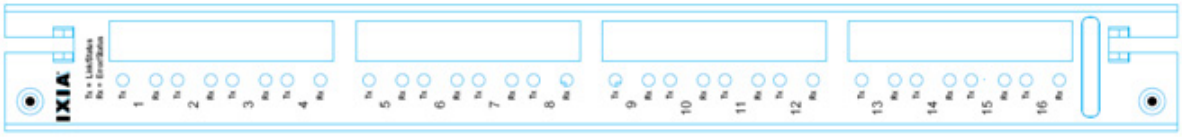
Feature	Specification
	Additional specifications for FlexAP1040SQ and FlexFE40QP are as follows: • Bits Sent • Bits Received • Central Chip Temperature(C) • Port CPU Status • Port CPU DoD Status • TxFmx Fpga Temperature(C) • RxFmx Fpga Temperature(C) • Pcpu Fpga Temperature(C) • PHY Chip Temperature(C) • Transmit Neighbor Solicitations • Transmit Neighbor Advertisements • Receive Neighbor Solicitations • Receive Neighbor Advertisements • Local Faults • Remote Faults • Frames Received with Coding Errors • Frames Received with /E/error Character • PCS Sync Errors • PCS Illegal Codes • PCS Remote Faults • PCS Local Faults • PCS Illegal Ordered Set • PCS Illegal Idle • PCS Illegal SOF • PCS Out of Order SOF • PCS Out of Order EOF • PCS Out of Order Data • PCS Out of Order Ordered Set

Mechanical Specification of FlexAP10G16S/FlexFE10G16S Load Modules

Front Panel

The Front panel of FlexAP10G16S/FlexFE10G16S load module is shown in the following figure:

Figure 29-5. Front panel of FlexAP10G16S/FlexFE10G16S



Led Panel

Table 29-3. Led panel of FlexAP10G16S/FlexFE10G16S Load Module Specifications

Feature	Specification
LED1	TX
	10GE Link up = Solid Green
	10GE TX Active = Blinking Green
	10GE TX Error = Blinking Red
	Inactive = Off
LED2	RX
	Loopback = Solid Green
	10GE RX Active = Blinking Green
	10GE RX Error = Blinking Red
	Link Down = Solid Red
	Port Inactive = Off

When port is in aggregation mode (the PCPU resource is used by other port), TX/RX LEDs are inactive (i.e. off). The aggregation egress port will have normal TX/RX LED operation.

Mechanical Specification of FlexAP1040SQ Load Modules

Front Panel Production – 944-1062-02

The Front panel of FlexAP1040SQ load module is shown in the following figure:

Figure 29-6. Front panel of FlexAP1040SQ

Led Panel Production – 944-1062-02

The Led panel of FlexAP1040SQ load module is shown in the following figure:

Figure 29-7. Led panel of FlexAP1040SQ

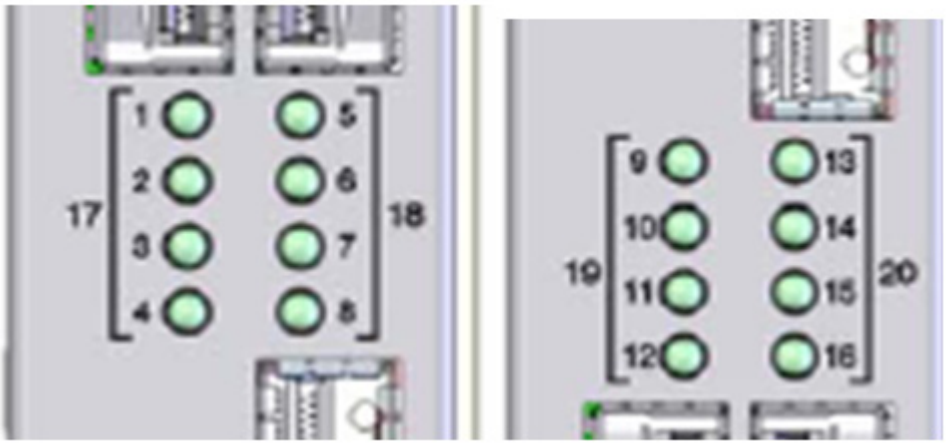


Table 29-4. Led panel of FlexAP1040SQ Load Module Specifications

Feature	Specification
10GE Mode	1 LED/Port where LED number matches port number
Blinking Green	Tx/Rx Activity
Blinking Red	Rx Error
Solid Red	Link down
Solid Green	Link up
Solid Yellow	Loopback
Off	Port is inactive

When port is in aggregation mode (the PCPU resource is used by other port), TX/RX LEDs are inactive (i.e. off). The aggregation egress port will have normal TX/RX LED operation.

Feature	Specification
40GE Mode	LED/Port aligned from top/down defined as follows: • Tx • Rx • Link • Error

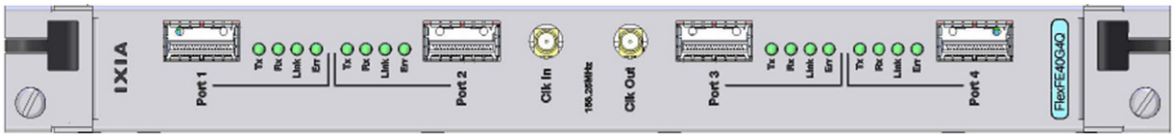
Definition matches the 40G Only definition.

Mechanical Specification of FlexAP40QP4 Load Modules

Front Panel

The Front panel of FlexAP40QP4 load module is shown in the following figure:

Figure 29-8. Front panel of FlexAP40QP4



Led Panel

Table 29-5. Led panel of FlexAP40QP4 Load Module Specifications

Feature	Specification
	LED/Port aligned from top/down defined as follows: • Tx • Rx • Link • Error
LED1	TX
	10GE TX Active = Blinking Green
	10GE TX Error = Blinking Red
	Inactive = Off
LED2	RX
	10GE RX Active = Blinking Green
	10GE RX Error = Blinking Red
	Port Inactive = Off
LED3	Link
	Link up = Solid Green
	Link Down = Solid Red
	Internal Loopback = Solid Yellow
	Line Loopback = Solid Blue
	Port Inactive = Off
LED4	Error
	Remote Faults = Blinking Yellow
	Local Faults = Solid Red
	Port Inactive = Off

30 IXIA Xdensity XDM10G32S Load Modules

This chapter provides details about Xdensity family of load modules—specifications and features. The IxExplorer name of this load module is XDM10G32S.

Xdensity is a 32 port load module with 10GE density per port. Each slot in this load module consists of 32 ports that can scale up to 384 ports in a single XM12 chassis. The high scalability feature of Xdensity load module provides test solutions for high density 10GE converged data center switches and routers.

The key features of Xdensity load module are mentioned as follows:

- An optimum solution for testing high density network switches
- Energy-efficient solution for large 10GE test environments
- 32-ports of 10GE in a single-slot load module
- 384-ports of 10GE SFP+ interfaces in a single 10U rackmount chassis
- Compatible with Ixia's XM2 and XM12 chassis
- Support for host protocol emulation to test layer 3 devices such as ARP, NDP, IPv4, IPv6, IGMP, MLD and DHCPv4/v6 (client and server)
- Built with multicore processor technology
- Supports the IxNetwork test application

The XDM10G32S load module is shown in the following figure:

Figure 30-1. Xdensity Load Module(XDM10G32S)

Part Numbers

The part numbers are shown in *Table 30-1*.

Table 30-1. Part Numbers for Xdensity Load Module

Model Number	Part Number	Description
XDM10G32S	944-1080	10-Gigabit Ethernet load module with 32 ports of SFP+ interfaces and L2-L3 data plane support; suitable for XM12-02 (941-0009) High Performance and XM2-02 (941-0003) portable chassis

Specifications

The load module specifications are contained in *Table 30-2*.

Table 30-2. Xdensity Load Module Specifications

Feature	Specification
Load Modules	XDM10G32S
Number of ports per module	32-ports of 10GBE SFP+ interface
Number of chassis slots per module	1
Maximum ports per chassis	• XM12 High Performance(4000W): 384-ports 10GESFP+ • XM2 Desktop: 64-ports 10GESFP+
SFP+ transceiver support	• 10GBASE-SR/SW • 10GBASE-LR/LW
Multi-core processor technology	Yes
Interface protocols	IEEE8002.3ae10GE LAN
Host protocol emulationsupport	ARP, NDP, IPv4, IPv6, IGMP, MLD and DHCPv4/v6 (Client+Server)
Performance benchmark tests	RFC 2544, RFC 2889
Stream definitions per port	16
Number of transmit flows per port (sequential values)	Billions
Number of transmit flows per port (non-sequential values)	Millions
User-Defined Fields (UDF)	Counter, Value List, and Nested Counter UDFs

Table 30-2. Xdensity Load Module Specifications

Feature	Specification
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures
User defined field features	Fixed, increment or decrement by user-defined step, value list, and nested UDF
Data field pattern per stream	Random, increment (word/byte), decrement (word/byte)
Frame length controls	Fixed, uniform random, auto, increment byuser-defined step, dynamic frame rate change, and frame size change on the fly
Error generation	CRC good, bad
IPv4, UDP, TCP, ICMP, ICMPv6, IGMP checksum	Hardware checksum generation and verification
Receive engine	Wire-speed packet filtering, data integrity, real-time latency, and sequence checking for each packet group
Trackable receive flows	8K per port
Filters	48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error, IP/TCP/UDP checksum error
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats (UDS), data integrity frames, data integrity errors, sequence checking frames, and sequence checking errors
Intrinsic latency adjustment	Ability to remove inherent latency from any MSA-compliant 10GE SFP+ transceivers without factory support
Transmit line clock adjustment	Ability to adjust the parts per million (ppm) line frequency over a range of +/-100 ppm
Operating temperature range	41°F to 104°F (5°C to 40°C), ambient air temperature
Load module dimensions	15.95" (L) x 12.00" (W) x 1.28" (H) 405mm (L) x 305mm (W) x 33mm (H)
Load module weights	Module only: 7.1 lbs. (3.2 kg) Shipping weight: 9.4 lbs. (4.3 kg)

31 IXIA Impairment Load Modules

This chapter provides specification and details of Ethernet Impairment Modules (EIM). This family of load modules consist of the following cards:

- EIM1G4S—1G Ethernet LAN Impairment Module
- EIM10G4S—10G Ethernet LAN Impairment Module
- EIM40G2Q—40G Ethernet LAN Impairment Module

The Impairment load modules have a single-slot form factor and are inserted into a high-density XM2 or XM12 chassis to provide 2 to 12 modules per chassis configuration. The load modules offer 4x1GE, 4x10GE, or 2x40GE Ethernet interfaces that can emulate 64, 32, or 8 unidirectional network clouds respectively.

The high density 1GE, 10GE, and 40GE Impairment test modules are ideal for emulating real-life network impairments. The modules can emulate a WAN environment and simulate network characteristics, such as delay, delay variation, and impairments, such as packet loss, duplication, and re-ordering.

EIMs support the Impairment feature in IxNetwork and IxLoad applications that provides a quick and easy way to set up impairments, across multiple emulated WAN links. Using EIM ports, IxNetwork and IxLoad is capable of generating a number of impairments, for example packet drops, latency, or packet re-ordering, which replicates real-life WAN traversal conditions, whereby packet flows are impaired in different modes when traversing a network.

The EIM40G2Q load module is not supported in IxLoad.

For more information on the Impairment feature, refer to chapter on ‘Network Impairment’ in the *IxNetwork Help* and *IxLoad Help*.

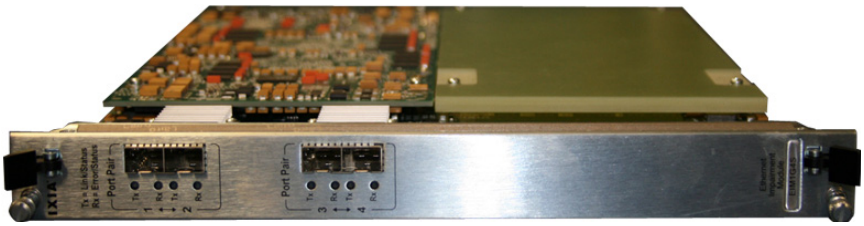
The key features of EIM are as follows:

- High density 1GE, 10GE, and 40GE load modules
- Realistic, high-scale WAN emulation
- Hardware-based impairment generation

- Integration with traffic generation, protocol emulation and analysis
- Scale port counts with high port density
- Simulate ultra-high latency: 500ms on each 40GE link, 600ms on each 10GE link and 6 sec. on each 1GE link at line rate traffic
- Leverage a single hardware chassis for traffic load modules
- Use IxNetwork for integrated traffic generation and impairment
- Quickly configure traffic flows and apply impairment
- Automate tests
- Analyze measurements with StatViewer interface
- Achieve 1GE, 10GE and 40GE line-rate impairment on all frame sizes (64 to 9180 byte frames) with no packet loss

The 1/10GE EIM load module is shown in the following figure:

Figure 31-1. ImpairNet™ 1/10GE Load Module



The 40GE EIM load module is shown in the following figure:

Figure 31-2. ImpairNet™ 40GE Load Module

Part Numbers

The part numbers are shown in *Table 31-1*.

Table 31-1. Part Numbers for Ethernet Impairment Load Module

Model Number	Part Number	Description
EIM1G4S	944-1081	ImpairNet EIM1G4S Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP interfaces. For XM12-02 (P/N 941-0009) High Performance and XM2-02 (P/N 941-0003) portable chassis, SFP transceivers are required. Options for transceivers include SFP-LX, SFP-SX, and SFP-CU (for RJ45 copper support).
EIM10G4S	944-1082	ImpairNet EIM10G4S 10 Gigabit Ethernet LAN Impairment module, 1-slot with 4-ports of SFP+ interfaces. For XM12-02 (P/N 941-0009) High Performance and XM2-02 (P/N 941-0003) portable chassis, SFP+ transceivers are required. Options for transceivers include 10GBASE-SR/SW (948-0013), or 10GBASE-LR/LW (948-0014).
EIM40G2Q	944-1083	ImpairNet EIM40G2Q 40 Gigabit Ethernet LAN Impairment module, 1-slot with 2-ports of QSFP+ interfaces. For XM12-02 (P/N 941-0009) High Performance and XM2-02 (P/N 941-0003) portable chassis QSFP+ 40GBASE-SR4 transceivers (P/N 948-0028) is required.

Specifications

The load module specifications are described in the following table:

Table 31-2. Ethernet Impairment Load Module 1/10GE Specifications

Feature	Specification
Number of ports per module	4-ports
Number of chassis slots per module	1
Chassis support	The EIM load modules are supported on the following XM2 chassis: • 941-0003-01 Rev. G and later version • 941-0003-02 Rev. C and later version • 941-0003-03 Rev. F and later version • 941-0003-04 Rev. G and later version • 941-0003-05 Rev. G or later version • 941-0003-06 Rev. A or later version **Note**: Earlier models of XM2 chassis require factory upgrade for compatibility with EIM load modules.
Module support	Up to 12 modules per XM12 Chassis Up to 2 modules per XM2 Chassis
SFP+ transceiver support	Available with 1GE SFP, Electrical SFP RJ45 1GE Transceiver, and 10GE SFP+ Ethernet interface options

Table 31-2. Ethernet Impairment Load Module 1/10GE Specifications

Feature	Specification
Traffic Selection and Impairment Configuration	• 16 traffic classifiers per link, total of 64 unidirectional classifiers per module for granular traffic classification • 16 impairment profiles per link, total of 64 profiles per module for granular service class emulation • Emulate 32 unidirectional or 16 bidirectional network clouds per port pair • Emulate 64 unidirectional or 32 bidirectional network clouds per module • Easy-to-use, packet-analyzer-based selection interface • Traffic classifier support for numerous protocols and applications like bridging, routing, carrier Ethernet, broadband, MPLS, IPv6, and miscellaneous application-layer protocols • Multiple service/traffic class emulation through independent and unique impairments per profile • Emulate network cloud aggregation using mask and match support for packet classifiers • Support for 8x16 bit frame matchers for each traffic classifier

Table 31-2. Ethernet Impairment Load Module 1/10GE Specifications

Feature	Specification
Supported Impairments	• Delay up to 600ms at 10GE, and up to 1.2s per module by cascading ports • Delay up to 6s at 1GE, and up to 12s per module by cascading ports • Packet Delay Variation using a selection of probability distributions • Delay resolution of 1µs • Emulate SLA validation by using normal/ Gaussian, exponential, uniform, and custom probability distribution for delay variations • Packet drop at rates of up to 100% in clusters up to 65535 packets • Reorder packets at rates of up to 50% in clusters up to 255 packets • Packet duplication at a rate up to 100% in clusters up to 65535 packets by creating up to 31 copies of each packet • Emulation of network/transmission/processing error conditions through bit error insertion for L2-L7 protocols • WAN forwarding error emulation • Ethernet FCS correction • Emulation of DS3, OC3, DS1, DS0, E1, E3, and cable modem link speeds using rate limiting
Multi-core processor technology	Yes
Operating temperature range	41°F to 86°F (5°C to 30°C), ambient air
Minimum Delay	• 1G: 300us • 10G: 30us

Table 31-3. EIM Load Module 40GE Specification

Feature	Specification
Interface Options	QSFP+
Ports/Module	1 port pair per module
Module/Chassis	• 1 module per XM2 chassis • Up to 6 modules per XM12 chassis

Table 31-3. EIM Load Module 40GE Specification

Feature	Specification
Traffic Selection and Impairment Configuration	• 16 traffic classifiers per up/down link, total of 32 unidirectional classifiers per module for granular traffic classification • 4 impairment profiles per link, total of 8 profiles per module for granular service class emulation • Emulates 32 unidirectional or 16 bidirectional network clouds per port pair • Emulate 64 unidirectional or 32 bidirectional network clouds per module • Easy to use packet analyzer based selection interface • Traffic classifier support for numerous protocols and applications like bridging, Routing, Carrier Ethernet, Broadband, MPLS, IPv6, and miscellaneous application-layer protocols • Multiple service/traffic class emulation through independent and unique impairments per profile • Emulate network cloud aggregation using mask and match support for packet classifiers • Real-time preview of classifier match on live traffic • Support for 8x16 bit frame matchers for each traffic classifier
Supported Impairments	• Delay up to 500ms at 40GE, and up to 1s per module by cascading ports • Delay resolution of 1µs • Emulate SLA validation by using normal/Gaussian, exponential, uniform, and custom probability distribution for delay variations • Packet drop at rates of up to 100% in clusters up to 65535 packets • Reorder packets at rates of up to 50% in clusters up to 255 packets • Packet duplication at a rate up to 100% in clusters up to 65535 packets by creating up to 31 copies of each packet • WAN forwarding error emulation • Ethernet FCS correction • Emulation of DS3, OC3, DS1, DS0, E1, E3, and cable modem link speeds using rate limiting.

32 IXIA Xcellon-Lava Load Modules

This chapter provides specification and feature details of the Xcellon-Lava 40/100 Gigabit Ethernet load modules. This family of load modules consist of the following 2-port cards:

- LavaAP40/100GE 2P
- LavaAP40/100GE 2RP

The Xcellon-Lava 40/100-Gigabit Ethernet load modules belong to the family of Ixia's High Speed Ethernet (HSE) products. These load modules combine the advantages of the Xcellon architecture and provide the highest 40GE and 100GE port densities. Lava load modules can be used for testing layer 1 to layer 7 applications. They are supported by Ixia's test applications, including IxNetwork and IxLoad.

Xcellon-Lava load modules are used for testing high-density data center 40 Gigabit Ethernet (40GbE) and 100 Gigabit Ethernet (100GbE) network equipments. 40GbE and 100GbE are high-speed computer network standards developed by the IEEE 802.3ba. Lava load modules extends the 802.3 protocol to operating speeds of 40 Gbps and 100 Gbps in order to provide greater bandwidth while maintaining maximum compatibility with the installed base of 802.3 interfaces.

Xcellon-Lava load modules are compatible with Ixia's XG12™, XM12, and XM2 chassis, and a broad range of Ethernet interfaces, allowing real-world, layer 1 to layer 7 test and measurement in a single chassis.

The Xcellon-Lava load module is shown in the following figure:

Figure 32-1. Xcellon-Lava Load Module

Part Numbers

The part numbers are shown in *Table 32-1*.

Table 32-1. Part Numbers for Xcellon-Lava Load Module and Supported Adapters

Model Number	Part Number	Description
Lava AP40/ 100GE 2P	944-1067	This is the dual speed 40GE/ 100GE Ethernet Lava load module with Accelerated Performance. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces. This load module supports full feature for layer 1 to layer 7 testing. **Note**: If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.
Lava AP40/ 100GE 2RP	944-1068	This is the dual speed 40GE/ 100GE Ethernet Lava load module with data plane support only. It is an economic alternative to the Accelerated Performance load module, perfectly suitable for testing layer 1 to layer 3 applications that does not require routing protocol emulation. Each load module consists of 2-ports and 1-slot with CFP MSA interfaces. **Note**: If XM12-01 (941-0002) chassis is used with this load module, the FRU-OPTIXIAXM12-01 (943-0005) power supply upgrade kit must be installed.

Table 32-1. Part Numbers for Xcellon-Lava Load Module and Supported Adapters

Model Number	Part Number	Description
CFP-to-QSFP+ Dual-Port Interface Adapter Module	948-0023	A pluggable, 2-port unit that converts an Ixia Xcellon-Lava CFP MSA port interface to 2-ports of pluggable 40 GE QSFP+ for fiber or copper cable assemblies or standalone transceivers. The adapter is compatible with the Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance, load module (944-1068). Both load modules accept up to two of the Dual Interface Adapter Modules.

Table 32-1. Part Numbers for Xcellon-Lava Load Module and Supported Adapters

Model Number	Part Number	Description
CFP-to-QSFP Interface Adapter Module	948-0022	A pluggable unit that converts an Ixia CFP MSA port interface to 1-port of the pluggable 40 GE QSFP+ for multimode fiber or copper cable assemblies or standalone transceivers. The adapter is compatible with the HSE40GETSP1-01, 40-Gigabit Ethernet load module (944-0069), HSE40/100GETSP1-01, 40/100-Gigabit Ethernet, dual-speed, load module (944-0091), HSE40/100GETSPR1-01, 40/100-Gigabit Ethernet, dual-speed, Data Plane Ethernet load module (944-0099), Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance load module (944-1068).

Table 32-1. Part Numbers for Xcellon-Lava Load Module and Supported Adapters

Model Number	Part Number	Description
CFP-to-CXP Interface Adapter Module	948-0027	A pluggable unit that converts an Ixia CFP MSA port interface to 1-port of the pluggable 100 GE CXP for multimode fiber or copper cable assemblies or standalone transceivers. The adapter is compatible with the HSE100GETSP1-01 100- Gigabit Ethernet load module (944-0070), HSE40/100GETSP1-01, 40/100-Gigabit Ethernet, dual-speed, load module (944-0091), HSE40/100GETSPR1-01, 40/100-Gigabit Ethernet, dual-speed, Data Plane load module (944-0099), Xcellon-Lava 40/100-Gigabit Ethernet, Accelerated Performance, load module (944-1067) and the Xcellon-Lava 40/100-Gigabit Ethernet, Reduced Performance load module (944-1068).

Specifications

The load module specifications are described in the following table:

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
Number of ports per module	• 2-100GE CFP MSA • 2-40GE CFP MSA or (4) 40GE QSFP [with interface adapter]
Number of chassis slots per module	1
Chassis support	The Lava load modules are supported on the following chassis: • XG12™ • XM12 • XM2

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
Maximum ports per chassis	• XG12™: (24) 100GE CFP MSA and (48) 40GE QSFP • XM12: (20) 100GE CFP MSA and (40) 40GE QSFP • XM2: (2) 100GE CFP MSA and (4) 40GE QSFP
Transceiver support	• CFP MSA 1.4, pluggable • SFF-8436 QSFP, pluggable fiber/copper cables (passive/active) with adapter
CFP interface adapters	• 1-port, CFP-to-QSFP for 40GE • 2-port, CFP-to-QSFP for 40GE **Note**: The 2-port, CFP-to-QSFP interface adapter module supports 1-port of the 2-ports of QSFP in the current release of the product. A future software upgrade will enable the second port • 1-port CFP-to-CXP for 100GE operation
Hardware capture buffer per port	1.4 GB
Interface protocols	40-Gigabit Ethernet 40GBASE-R and 100-Gigabit Ethernet 100GBASE-R as per IEEE802.3ba-2010 standard

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
Layer 2/3 routing protocol emulation	The following protocols are supported in LavaAP40/100GE 2P Full Performance load module: • **MPLS**: RSVP-TE, RSVP-TE P2MP, LDP, PWE, L3 MPLS VPN, 6VP, MPLS-TP • **Routing**: RIP, RIPng, OSPFv2/v3, ISISv4/v6, EIGRP, EIGRPv6, BGP-4,BGP+ • **VPLS**: 6PE, BGP Auto-Discovery with LDP FEC 129 Support, VPLS-LDP, VPLS-BGP • **IP Multicast**: IGMPv1/v2/v3, MLDv1/v2, PIM-SM/SSM, PIM-BSR, Multicast VPN, VPNv6 • **Switching**: STP/RSTP, MSTP, PVST+/ RPVST+, LACP • **Carrier Ethernet**: Link OAM, CFM, Service OAM, PBT/PBB-TE, SyncE, IEEE 1588v2 PTP • **High-Availability**: BFD The following **Host/Client** protocols are supported in LavaAP40/100GE2 RP Full Performance load module: • ARP • NDP • ICMP (PING) • IPv4 • IPv6
Layer 4-7 application traffic testing	This is suppoted only in LavaAP40/100GE 2P Accelerated Performance load module.
Transmit flows per port (sequential values)	Billions
Transmit flows per port	1 million
Trackable receive flows per port	1 million
Stream definitions per port	256 **Note**: In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows. In the Data Center mode, the number of transmit streams is 256.

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
Table UDF entries	512K **Note**: Comprehensive packet editing function for emulating large numbers of sophisticated flows is supported by Xcellon-Lava load module. Entries of up to 256 bytes, using lists of values can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size and a list of values in a table format.
Packet flow statistics	Xcellon-Lava load module tracks over 1 million flows.
Transmit engine	The Xcellon-Lava load module supports wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures.
Receive engine	The Xcellon-Lava load module supports wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, data integrity, and sequence checking.
User Defined Field (UDF) features	The Xcellon-Lava load module supports the UDF features of fixed, increment or decrement by user-defined step, value list, cascade, random, and chained.
Filters	The Xcellon-Lava load module uses 48-bit source/destination address, 2x128-bit user-definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)
Error Generation	CRC (good/bad/none), undersize, oversize
Transmit Line Clock Adjustment	Xcellon-Lava load module has the ability to adjust the parts per million (ppm) line frequency over a range of -100 ppm to +100 ppm.

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
Layer 1 BERT capability	The Xcellon-Lava load module supports the following BERT features on both 40 GE and 100 GE speeds: • User selected PRBS pattern for each PCS Lane • User can select from a wide range of PRBS data patterns to be transmitted with the ability to invert the patterns • Send single, continuous, and exponentially controlled amounts of error injection • Wide range of statistics, including Pattern Lock, Pattern Transmitted, Pattern Received, Total Number of Bits Sent and Received, Total Number of Errors Sent and Received, Bit Error Ratio (BER), and Number of Mismatched 1's and 0's. • Lane Stats Grouping per lambda for SMF and MMF 40GE and 100GE based on IEEE 802.3ba defined physical medium dependent (PMD).

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
40/100 GE Physical Coding Sublayer (PCS) test features	The Xcellon-Lava load module supports IEEE 802.3ba compliant PCS transmit and receive side test capabilities. The supported PCS features are as follows: • **Per PCS lane, transmit lane mapping**: Supports all combination of PCS lane mapping: Default, Increment, Decrement, Random, and Custom. • **Per PCS lane, skew insertion capability**: User selectable from zero up to 3 microseconds of PCS Lane skew insertion on the transmit side. • **Per PCS lane, lane marker, or lane marker and payload error injections**: User selectable ability to inject errors into the PCS Lane Marker and simultaneously into PCS Lane Marker and Payload fields. This includes the ability to inject sync bit errors into the Lane Marker and Payload. User can control the PCS lane, number or errors, period count and manage the repetition of the injected errors. • **Per PCS lane, receive lanes statistics**: PCS Sync Header and Lane Marker Lock, Lane Marker mapping, Relative lane deskew up to 52 microseconds for 40GE and 104 microseconds for 100GE, Sync Header and PCS Lane Marker Error counters, indicators for Loss of Synch Header and Lane Marker, and BIP8 errors.
IPv4, IPv6, UDP, TCP checksum	Xcellon-Lava load module supports hardware checksum generation and verification.
Frame length controls	Xcellon-Lava load module supports fixed, random, weighted random, or increment by user-defined step, random, and weighted random.
Preamble view	Xcellon-Lava load module allows to select to view and edit the preamble contents.
Link Fault Signaling	Xcellon-Lava load module generates local and remote faults with controls for the number of faults and order of faults, plus the ability to select the option to have the transmit port ignore link faults from a remote link partner.

Table 32-2. Xcellon-Lava Ethernet Load Module Specifications

Feature	Specification
Operating temperature range	41°F to 95°F (5°C to 35°C), ambient air **Note**: When an Xcellon-Lava load module is installed in an XM12, XM2, or XG12 chassis, the maximum operating temperature of the chassis is 35°C (ambient air).
Load module dimensions	16.0" (L) x 12.0" (W) x 1.3" (H) 406mm (L) x 305mm (W) x 33mm (H)
Weight	• Module only: 9.8 lbs (4.45 kg) • Shipping: 12.0 lbs (5.45 kg)

The Ixia application support for Lava AP40/100GE 2P and Lava AP40/100GE 2RP is provided in the following table:

Table 32-3. Xcellon-Lava Application Support

Lava AP40/100GE 2P	Lava AP40/100GE 2RP
IxExplorer	IxExplorer
IxNetwork	IxNetwork
IxAutomate	IxAutomate
IxLoad	IxLoad
TCL API	TCL API

33 IXIA Power over Ethernet Load Modules

This chapter provides details about Power over Ethernet (PoE) Load Modules—specifications and features.

Ixia's Power over Ethernet (PoE) Load Modules are used to test Power Sourcing Equipment (PSE) in accordance with IEEE Std 802.3af. The PoE Load Modules emulate Powered Devices (PDs) with programmable characteristics, and include data acquisition circuits for measuring voltage, current, and time.

The PoE Load Modules are intended to be used in conjunction with Ixia's line of Ethernet traffic generator/analyzer load modules. The PoE Load Modules handle the detection, classification, and power loading aspects of 802.3af, while passively conveying Ethernet data between the PSE and the traffic generator/analyzer load modules.

Ixia offers two models of PoE Load Modules. The basic model (PLM1000T4-PD) is rated for 20 Watts continuous power dissipation per port. The advanced module (LSM1000POE4-02) is rated for 30 Watts per port, and has several additional advanced features, including configurable ZAC2 settings. Both models include 4 independent and isolated PD emulators on a single-slot load module.

Figure 33-1. PLM1000T4-PD Load Module

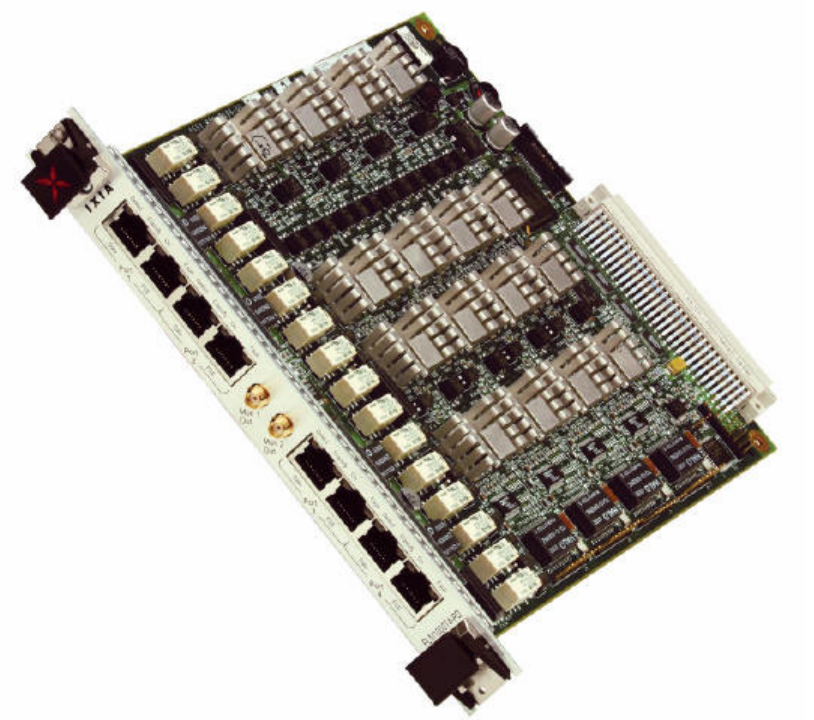


Figure 33-2. PLM1000T4-PD Load Module Face Plate

Part Numbers

The part numbers are shown in *Table 33-1*. Items without a *Price List Name* entry are no longer available.

Table 33-1. Part Numbers for Gigabit Modules

Load Module	Price List Name	Description
PLM1000T4-PD	PLM1000T4-PD	4-port PoE Load Module, 20W/Port, emulating Powered Devices.
LSM1000POE4-02	LSM1000POE4-02	4-port PoE Load Module, 30W/Port, emulating Powered Devices.

Specifications

The load module specifications are contained in the following table. The limitations of -3, Layer 2/3, and Layer 7 cards are discussed in *Ixia Load Modules* on page 1-4.

Table 33-2. PoE Load Module Specifications

	PLM1000T4-PD	LSM1000POE4-02
# ports	4	4
Data Rate	10/100/1000 Base-T	10/100/1000 Base-T
Connector	RJ-45	RJ-45
R_SIG Range/ Resolution	2–45k/200 Ohms	2–45k/200 Ohms
C_SIG Range/ Resolution	0–220nF/10nf	0–220nF/10nf
I_CLASS Range	–60mA	0–60mA
I_CLASS Resolution/ Accuracy	0.25mA	0.25mA
DC MPS Range/ Resolution	0–60mA/0.25mA	0–60mA/0.25mA
AC MPS R_PD Range/Resolution	Zac1: 10–45k/200 Ohms Zac2: Fixed/ > 4 Ohms	Zac1: 10–45k/200 Ohms Zac2: 200–1200k/ 8k
AC MPS C_PD Range/Resolution	0–220nF/10nF	0–220nF/10nF
Data Acquisition Sample Rate	5MSPS	5MSPS
Data Acquisition Voltage Range/ Resolution/ Accuracy	0–64V/10 bits/0.5%	0–64V/10 bits/0.5%
Data Acquisition Current Range/ Resolution/ Accuracy	0–1024mA/10 bits/0.5%	0–1024mA/10 bits/ 0.5%
Data Acquisition Power Readback Accuracy	100mW	100mW
Maximum Continuous Power	20W per port	30W per port
Load Modes	Constant Current (CC) Power (CP)	Constant Current (CC) Power (CP)

Table 33-2. PoE Load Module Specifications

	PLM1000T4-PD	LSM1000POE4-02
Pulse Modes (CC only)	Single, Continuous, Inrush	Single, Continuous, Inrush
Programmable Pulse Parameters	Amplitude, Width, Duty, Slew Rate	Amplitude, Width, Duty, Slew Rate

Port LEDs

Each port incorporates a set of LEDs, as described in *Table 33-3* on page 33-4.

Table 33-3. PoE Load Module Port LEDs

LED Label	Usage
Detect	When green, indicates the PSE is in the detection process.
Classify	When green, indicates the PSE is in the classification process.
Powered	When green, indicates the PSE is powering the emulated PD.
Fault	When red, indicates the PSE has performed an illegal operation. PoE disconnects under a fault condition until the PSE resets.

Test Monitor Output Ports

There are two test monitor output ports on each PoE module, used to measure the power/current into a selected port. These ports can be used in conjunction with an oscilloscope to view input characteristics. The ports have the following scale:

Table 33-4. Test Monitor Ports

Factor	Measurement
DC Measurements	62.5mV out/Volts input
DC Current	4mV out/ mA Input
AC Measurement	.05V out/Volts Input (Planned Feature)

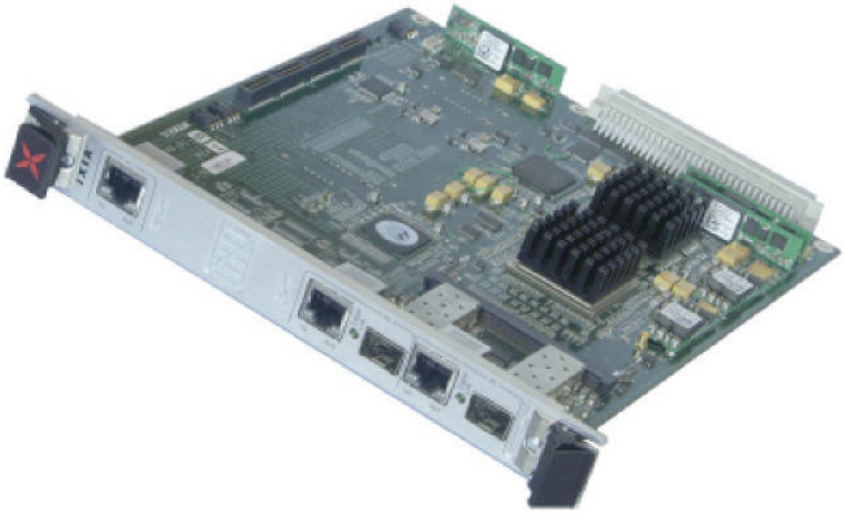
Statistics

Statistics counters for PoE cards may be found in *Table B-6* on page B-9.

34 IXIA Stream Extraction Modules

The Stream Extraction module has three ports: two test ports and one monitor port. The monitor port has up to eight pattern matchers that you can configure. In addition, there are AND/OR operations to the pattern matching that do not exist in other module.

Figure 34-1. AFM1000SP-01 Load Module



You can configure the pattern matching based on the MAC address, IP Address, or TCP/UDP address.

Part Numbers

The part numbers are shown in *Table 34-1*. Items without a *Price List Names* entry are no longer available.

Table 34-1. Part Numbers for Gigabit Modules

Load Module	Price List Name	Description
AFM1000SP-01	AFM1000SP-01	3 port Stream Extraction module, port 1 RJ-45 copper, port 2/3 RJ-45 Dual PHY copper/fiber.

Specifications

The load module specifications are contained in the following table.

Table 34-2. AFM1000SP-01 Load Module Specifications

	AFM1000SP-01
# ports	3 (to capture, one analyzer)
Data Rate	10/100/1000 Mbps
Connector	RJ-45 (Copper) port 1 RJ-45 Dual PHY (Copper and Fiber) port 2/3
Capture buffer size	N/A
Captured packet size	N/A
Streams per port	N/A
Advanced scheduler streams per port	N/A
Flows per port	N/A
Preamble size: min-max	N/A
Frame size: min-max	N/A
Inter-frame gap: min-max	N/A
Inter-burst gap: min-max	N/A
Inter-stream gap: min-max	N/A
Latency	N/A

Port LEDs

Each port incorporates a set of LEDs, as described in *Table 34-2* on page 34-2.

Table 34-3. AFM1000SP-01 Load Module Port LEDs

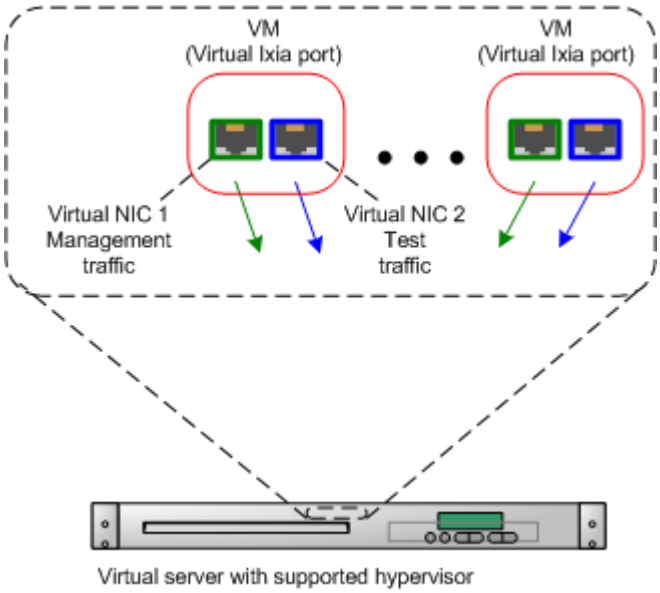
LED Label	Usage
Link/Tx (Upper LED)	Color is used to indicate the link speed: • 1000Mbps–Green • 100Mbps–Orange • 10Mbps–Yellow Flashing indicates transmit activity. Off if link is down.

Statistics

Statistics counters for AFM1000SP-01 cards may be found in *Table B-28* on page B-156.

35 IxVM

IxVM is a software-based test platform that enables you to turn standard Linux Ethernet ports into virtual Ixia ports. IxVM can create virtual Ixia ports from the virtual Ethernet ports on a Linux virtual machine (VM), or from the physical Ethernet ports on a physical Linux server.



To configure the traffic generated by the virtual Ixia ports, you use compatible versions of Ixia applications such as IxExplorer, IxNetwork, and IxLoad. When you use these applications, working with a virtual Ixia port is the same as working with a real chassis, with only a few minor differences.

IxVM offers the following benefits:

- Low hardware cost - you can use low-cost Linux servers or dedicated virtualization servers to generate traffic.
- More efficient use of hardware - the same Linux servers used to generate Ixia traffic can also be used for other non-Ixia applications, or the virtual Ixia ports can be hosted on a virtualization server used to host other applications.
- Choice of deployment models - IxVM components are supplied as pre-configured .ova templates or as standalone RPM packages for quick deployment.
- Rapid deployment - Virtual Ixia ports can be instantiated as necessary, used to generate traffic, and then destroyed when no longer needed, releasing system resources for other uses.
- Ease of Use - IxVM-aware Ixia applications are nearly identical to the standard versions, reducing learning time.
- Reduced System Administration - because the IxVM chassis is virtual, it does not have to be housed in a lab or monitored.

In this section:

Features

IxVM main features include:

- Support for VMware vSphere or KVM hypervisors.
- Ixia-enhanced kernel OVA template for full functional routing and switching testing.
- Reduced-footprint rpm-based installers for KVM and bare-metal Linux deployments.
- 32 bit Ixia Kernel self-extracting images for KVM hypervisors.
- Discovery service that finds virtual Ixia ports and adds them to list of available ports in the test application.
- Deployment of IxVM software upgrades using IxAdmin.
- Jumbo frame generation for high-throughput testing.
- Support for many IxNetwork and IxLoad protocols.

Requirements

IxVM requires the following:

Hardware

IxVM Server: IxVM server requires Windows XP Pro SP3 32-bit.

ESX(i) deployments: IxVM runs on any virtualization server that ESX(i) supports.

KVM / other deployments: For KVM and bare-metal deployments, Ixia recommends a high-performance server with CPUs that include virtualization extensions such as Intel-VT or AMD-V. A high-end application server is available from Ixia - contact your Ixia sales representative for more information.

Hypervisor / Host OS

IxVM supports the following hypervisors or host OSes:

- VMware ESX/ESXi 4.0 or ESXi 4.1 for vSphere 4 deployments (OVA deployments)
- KVM (QEMU) over CentOS 5.6 64-bit (KVM self-extracting deployments)
- CentOS 5.6 64-bit (RPM bare metal deployments)

VM Operating Systems (Guest OS)

IxVM virtual ports can be created on any VM running one of the following operating systems:

- Ixia-enhanced kernel
- RedHat Enterprise Linux 5.6, 32- or 64-bit
- CentOS 5.5 or 5.6, 32- or 64-bit
- SUSE Linux Enterprise Server 11, 32 bit

Distribution Methods

IxVM is distributed using a variety of methods. The table below lists how IxVM is distributed for supported combinations of hypervisor and guest OS.

	Guest OS Distribution Method	
Hypervisor or Host OS	**Ixia Kernel**	**RedHat/CentOS/SUSE**
VMware ESX/ESXi 4.0	OVA	RPM
VMware ESXi 4.1	OVA	RPM
KVM (QEMU) over CentOS 5.6 64-bit	Self-extracting image	RPM
CentOS 5.6 64-bit on bare metal		RPM

VM Discovery

Discovery Server discovers virtual Ixia ports, and adds them to the list of available ports in Ixia testing applications. You can download Discovery Server from the IxVM page of Ixia's website.

Update Utility

IxAdmin updates the IxVM platform with new versions of the IxVM software. You can download IxAdmin from the IxVM page of Ixia's website.

Ixia Application Software

The following applications are supported on the IxVM platform:

- IxNetwork
- IxExplorer
- IxLoad

You can download all three from Ixia's website.

The following tables lists the Ixia applications you can run on each combination of hypervisor and guest OS:

	Guest OS
Hypervisor or Host OS	**Ixia Kernel**
VMware ESX/ESXi 4.0	IxExplorer IxNetwork IxLoad
VMware ESXi 4.1	IxExplorer IxNetwork IxLoad
KVM (QEMU) over CentOS 5.6 64-bit	IxExplorer IxNetwork
CentOS 5.6 64-bit on bare metal	

	Guest OS	
Hypervisor or Host OS	**RedHat/CentOS 5.6 32-bit**	**RedHat/CentOS 5.6 64-bit**
VMware ESX/ ESXi 4.0	IxExplorer IxNetwork	IxExplorer IxNetwork
VMware ESXi 4.1	IxExplorer IxNetwork	IxExplorer IxNetwork
KVM (QEMU) over CentOS 5.6 64-bit	IxExplorer IxNetwork	IxExplorer IxNetwork
CentOS 5.6 64-bit on bare metal		IxExplorer IxNetwork

Hypervisor or Host OS	Guest OS SUSE LINUX ES 11 32-bit
VMware ESX/ESXi 4.0	IxExplorer IxNetwork
VMware ESXi 4.1	IxExplorer IxNetwork
KVM (QEMU) over CentOS 5.6 64-bit	IxExplorer IxNetwork
CentOS 5.6 64-bit on bare metal	

About the Red Hat and CentOS Kernels

RedHat Enterprise Linux 5.6 and CentOS 5.x are based on the same kernel. RedHat Enterprise Linux requires a subscription, in return for which Red Hat Inc. provides support and other services. CentOS is the Community Enterprise edition, and is free. The same RPM packages can be compiled and installed on both RedHat and CentOS.

Licensing

The following are the licensing requirements of IxVM and its related Ixia components:

Licensed:

- IxVM Server requires a license.
- IxLoad, IxNetwork, and IxNetwork-FT require licenses.
- Discovery Server requires a license.

Note: All IxVM-enabled test applications such as IxVM Server, IxExplorer, IxNetwork/IxNetwork-FT and IxLoad use floating licenses, meaning that a specified license server stores a number of licenses that can be re-used alternatively by a number of installed test applications.

Each time a test application starts, one license is used from those available on the licensing server. This allocation process continues as more applications request licenses, until the pool of remaining licenses is depleted.

For each of the test applications, you specify the licensing server in the following locations:

- For IxVM Server, specify the server host on the TOOLS > OPTIONS > DIALOG tab.
- For IxNetwork-FT, specify the server host on the IxExplorer TOOLS > OPTIONS > LICENSE MANAGEMENT tab.
- For IxNetwork, specify the server host on the FILE > PREFERENCES > ADVANCED tab, in the IXVM section.
- For legacy Network-FT TCL scripts, follow the instructions for setting the license server through IxExplorer / Network-FT. Once you set the Explorer / Network-FT license server, you can run your TCL scripts.
- For IxLoad, specify the server host by clicking OPTIONS > LICENSE SERVER on the toolbar.

If you change the license server location in any of the test applications, you must restart the application for the new location to take effect.

The license server host must have the IxProxy service running on it to traverse any firewalls between the license server host and the hosts running the test applications. IxProxy is supplied with IxVM Server and must be manually started using the SERVICES - ADMINISTRATIVE tool of Windows.

IxLicensing 3.00.58.23 or higher must be installed on the license server host.

Not Licensed:

- IxAdmin does not require a license.
- IxExplorer does not require a license.
- Analyzer does not require a license.

Note: If you add IxVM cards until all the licenses are consumed, disconnecting a connected card may not allow another card to be added.

For example, in the following scenario:

Action	Result
4 cards connected	All licenses used
Connect card 5	No license available
Disconnect card 4	License available
Connect card 5 again	Fails to reconnect

The solution is to disconnect both cards at the same time, and then re-connect the new card only.

The Ixia licensing process is described in the *Ixia Licensing Guide*.

IxVM Deployment Models

There are three general ways that you can deploy IxVM:

- vSphere: In an vSphere deployment, you use vSphere to create VMs that are based on the Ixia kernel OVA template or on one of the supported Linux distributions.
- KVM: In a KVM deployment, you install IxVM disk images on a KVM server, and the supporting software on either a Windows VM or Windows PC. You can also use the KVM self-extracting image to create Ixia Kernel VMs.
- Bare metal: In a bare metal deployment, you install IxVM RPM packages on a bare metal Linux server, and the supporting software on a Windows PC.

This section describes each method.

In this section:

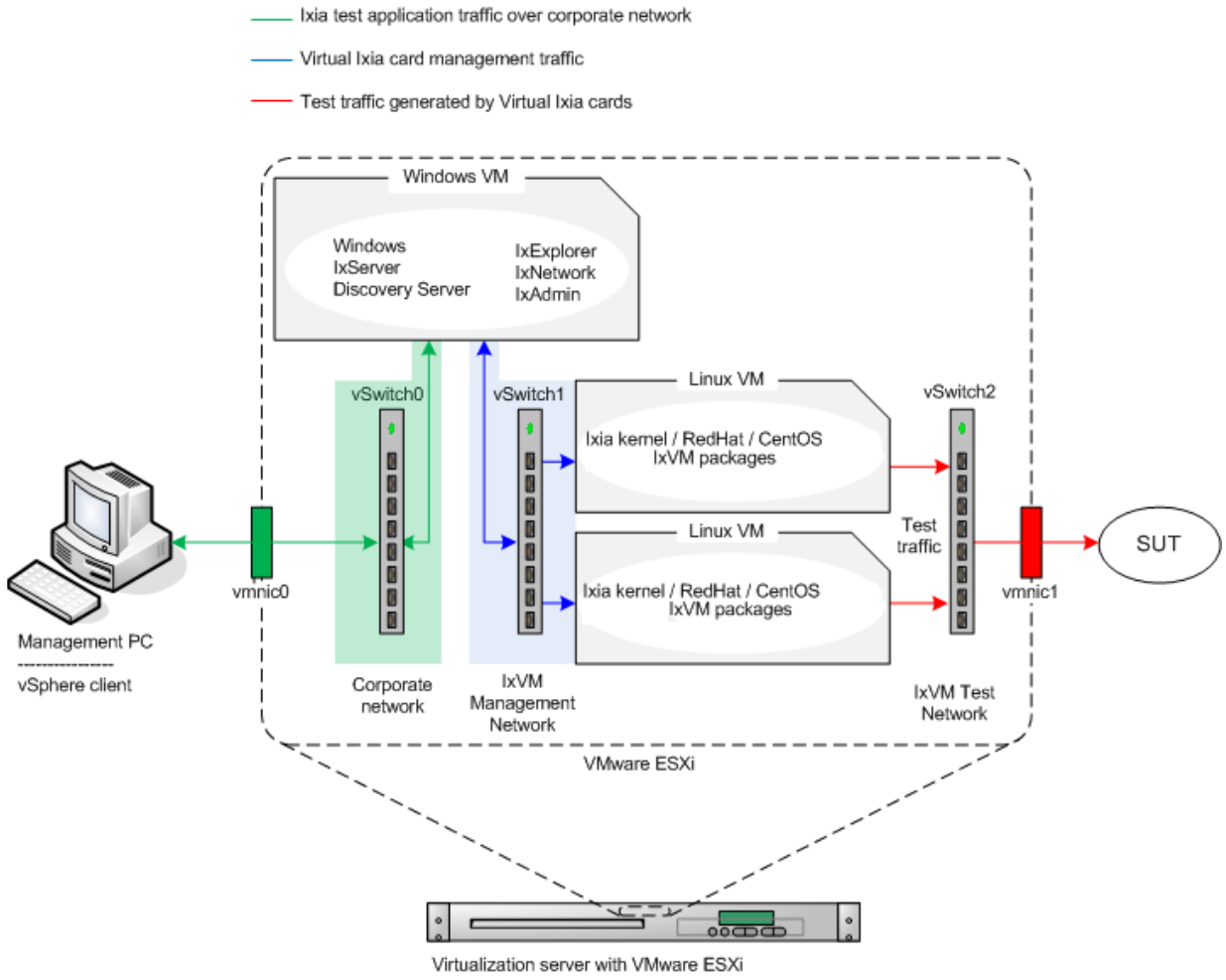
vSphere Deployment

In an vSphere deployment, you use vSphere to create VMs based on the Ixia kernel template file (.ova).

In the figure below, the following components are present:

- Virtualization server with VMware ESX(i): The virtualization server is the physical machine that hosts the ESX(i) virtualization operating system.
- Windows VM: The Windows VM is a virtual Windows PC hosted on the virtualization server, and functions as the IxVM chassis controller. It hosts the following applications:
  - IxServer, which manages traffic between Ixia applications and the virtual Ixia ports.
  - Discovery Server, which discovers virtual Ixia ports running on the virtualization server, and adds them to the lists of test ports in Ixia testing applications.
  - IxNetwork, IxExplorer, and IxLoad, the Ixia testing applications.
- Linux VMs: The Linux VMs are VMs hosted on the virtualization server that are running one of the supported Linux kernels and the IxVM packages that generate the test traffic. Each VM has two NICs: one for management traffic, and one for test traffic.
- Virtual switches: The vSwitches are virtual equivalents of physical switches and perform the same function, routing traffic to and from the virtual Ixia ports. The virtual switches are created using vSphere.

- Windows PC: The Windows PC is used to access and control the VMs on the ESX(i) host using vSphere.



KVM Deployment

In a KVM deployment, the virtual Ixia ports are created on virtual machines running under the KVM hypervisor on a KVM server. The figure below shows the components used in a KVM deployment.

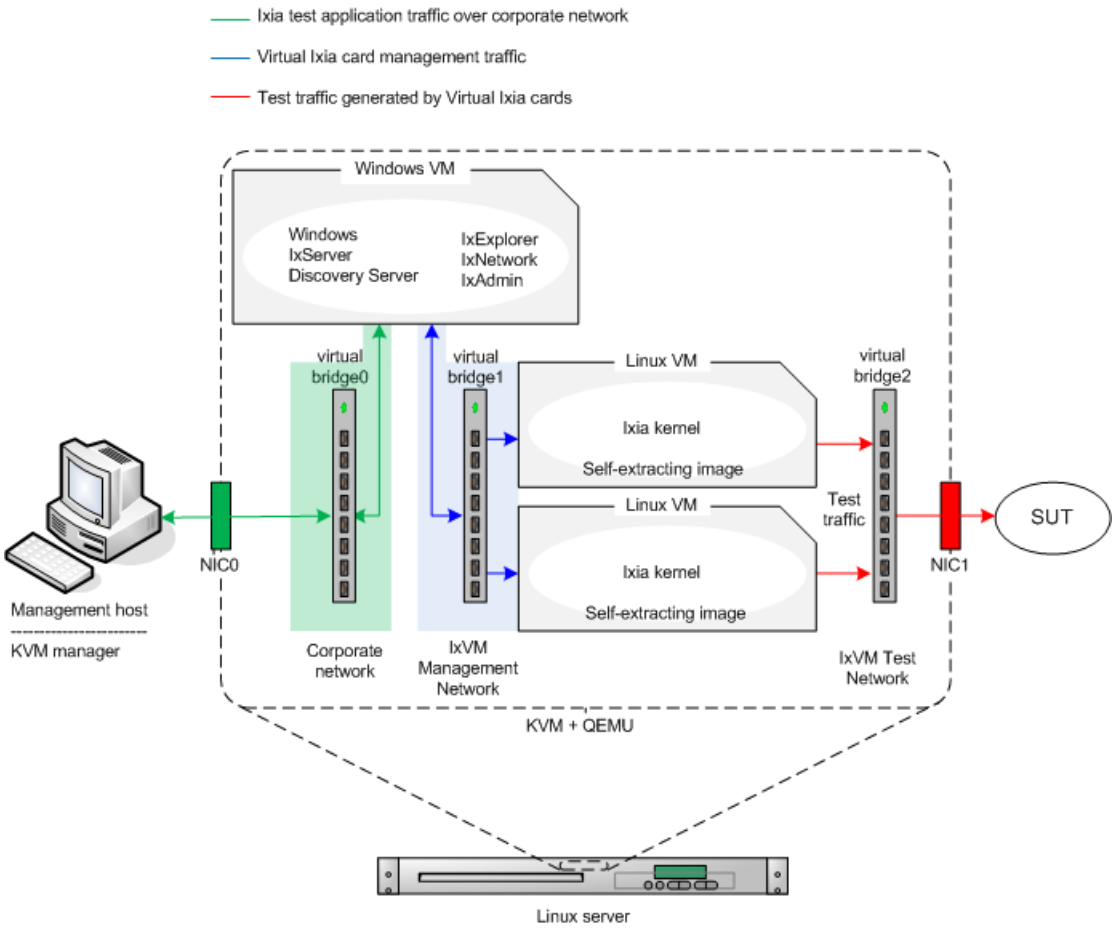
In the figure below, the following components are present:

- KVM server: The KVM server is the physical machine that hosts the KVM hypervisor.
- Windows VM: The Windows VM is a virtual Windows PC hosted on the KVM server, and functions as the IxVM chassis controller. It hosts the following applications:
  - IxServer, which manages traffic between Ixia applications and the virtual Ixia ports.

- Discovery Server, which discovers virtual Ixia ports running on the virtualization server, and adds them to the lists of test ports in Ixia testing applications.
- IxNetwork and IxExplorer, the Ixia testing applications.

  Alternatively, a physical PC can also be used as the IxVM controller.

- Linux VMs: The Linux VMs are VMs hosted on the virtualization server that are running one of the supported Linux kernels and the IxVM packages that generate the test traffic. Each VM has two NICs: one for management traffic, and one for test traffic.
- Virtual switches: The virtual switches are virtual equivalents of physical switches and perform the same function, routing traffic to and from the virtual Ixia ports. The virtual switches are created using KVM.
- Management host: The management host is used to manage the VMs on the KVM host using a KVM management utility.



Creating TLS Certificates

You can use the Virtual Chassis Builder to reboot IxVM cards from windows, or you can use or VMHardReboot.exe to reboot them from Tcl scripts (see Rebooting From a Tcl Script). However, for IxVM cards running on the KVM/QEMU hypervisor, you must configure a TLS certificate for the host before you can reboot them. Also, in order to use the hard reboot feature for VMWare ESX(i) hosts, you need to have a VMWare license installed.

This process is described in the libvirt wiki: http://wiki.libvirt.org http://wiki.libvirt.org

To create the TLS certificates:

1. Complete the following procedures described on the libvirt wiki pages:
   a: Create the Certificate Authority Certificate (http://wiki.libvirt.org/page/TLSCreateCACert http://wiki.libvirt.org/page/TLSCreateCACert).
   b: Create the Server Certificates (http://wiki.libvirt.org/page/TLSCreateServerCerts http://wiki.libvirt.org/page/TLSCreateServerCerts).
2. Afterwards, edit the libvirt configuration file (/etc/libvirt/libvirtd.conf).

   Uncomment the following two lines (remove the leading "#"):

```
#listen_tcp = 1
#tcp_port  = "16509"
Uncomment the following line:
#auth_tcp = "sasl"
and change it to:
auth_tcp = "none"
```

3. Restart the libvirtd service.

Bare-metal Linux Deployment

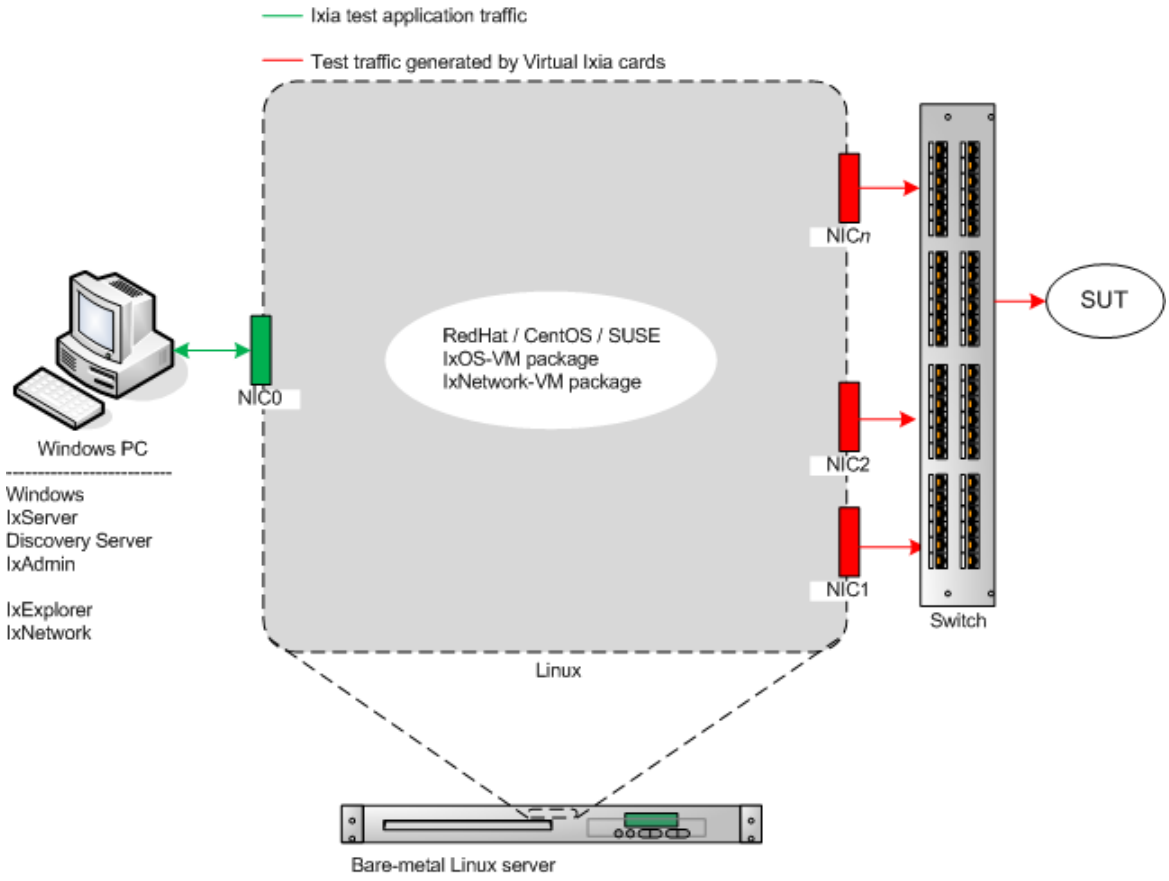
Although deploying IxVM as a series of VMs is the most typical scenario for using IxVM, it can also hosted on a bare-metal Linux server. The figure below shows the components used in a bare-metal deployment of IxVM.

In the figure below, the following components are present:

- Linux server: The Linux server runs one of the Linux kernels supported by IxVM, and the supporting IxVM packages that generate the test traffic.
- Windows PC: The Windows PC hosts the following applications:
  - IxServer, which manages traffic between Ixia applications and the virtual Ixia ports.
  - Discovery Server, which discovers virtual Ixia ports running on the virtualization server, and adds them to the lists of test ports in Ixia testing applications.
  - IxAdmin, which updates IxVM software.

- IxExplorer and IxNetwork, the Ixia applications used to configure and run tests, and that use the virtual Ixia ports to generate traffic.

- Switch: The switch routes the test traffic to and from the SUT.



Windows components

The Windows components required to manage and use IxVM virtual cards can be installed in any of the following places:

- On a Windows VM

  If you have a vSphere or KVM environment, you can create a Windows VM (or use an existing one) and then install the IxVM components on it.

- On a physical Windows PC

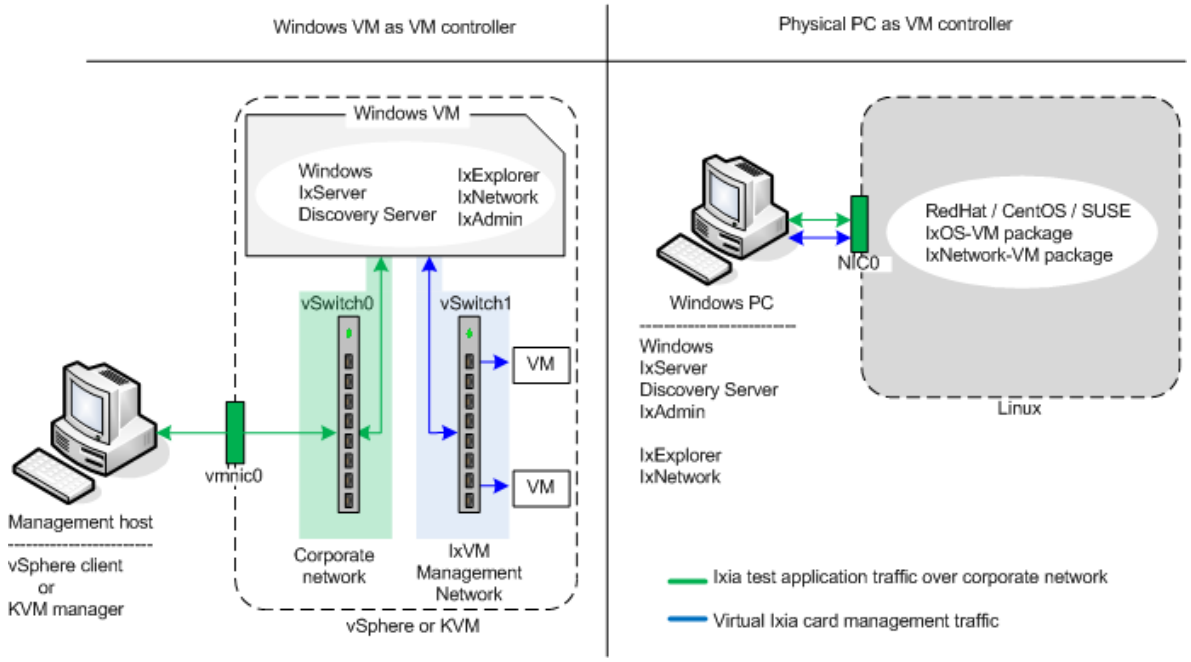
  In vSphere or KVM deployments, you can also use a physical PC as the IxVM controller. If you are deploying on bare metal, a physical PC is the only option for the IxVM controller.

Note: You cannot install the IxVM component on an Ixia chassis.

Installing IxVM Components on a Physical PC or Windows VM

To use a physical PC or Windows VM as the IxVM controller, install the following applications on the PC or Windows VM, making sure to select the options for IxVM support when you install them:

- IxOS
- Discovery Server
- IxAdmin
- IxExplorer



TCP/UDP Ports Required

The following ports are needed for communication between Windows VM and Linux VMs:

TCP

- 998 betaftpd_shadow
- 999 inetd
- 1000 ixdiscoveryagent
- 6001 ixServiceManager
- 6665 InterfaceManager
- 9101 ixStatDaemon
- 9102 ixStatDaemon
- 9613 ixDodClient

- 9614 pcpuManagerar
- 10116 ixdiscoveryagent

UDP

- 123 ntpd
- 1000 ixdiscoveryagent
- 10116 ixdiscoveryagent

Windows VM ports

Windows VM ports are as follows:

- **TCP ports**: 1000, 1080, 5285, 6001, 6005, 8021, 9101, 9102, 9613, 17668, 17669, 17670, 17672, 33000, 57843, 57845, 57846, 57847, 61248, 61260, 61272, 61274
- **UDP ports**: 1000, 65031

Installing IxVM

The installation process for IxVM depends on the deployment type you are using:

- vSphere: In an vSphere deployment, you can install IxVM by creating VMs in vSphere and basing them on the Ixia kernel OVA template. The OVA template includes all the supporting software required for IxVM pre-installed.
- KVM: In a KVM deployment, you use self-extracting disk images to create VMs that have all the IxVM packages already installed, or you use RPMs to install the IxVM packages on VMs that you have created yourself.
- Bare-metal: In a bare-metal deployment, you use RPM to install the IxVM packages on a bare-metal server that is running one of the supported Linux distros.

The following sections describe each method:

- *OVA-based Installation*
- *KVM Installation*
- *Bare-metal (RPM) Installation*

OVA-based Installation

The sequence for deploying IxVM on vSphere is as follows:

1. Download and install VMware ESX(i) on your VMware server (if you have not already done so).
2. If you intend to use a VM as the IxVM chassis controller, create a Windows VM in VMware, and install IxServer and the supporting applications on it.
3. Download the Ixia kernel template (.ova) file, and use the template to create the one or more Linux VMs to host the virtual Ixia ports
4. Configure Discovery Server.

The following sections describe each of these steps.

After you have completed the steps, you can begin using the virtual Ixia ports with your Ixia testing application.

Downloading and Installing vSphere

If you have not already installed VMware's ESX(i), you must install it on your server. ESX(i) is available free and has the same user interface as the enterprise versions of vSphere and vCenter Server.

Note: ESX(i) is a Type 1hypervisor -- a virtualization operating system. It is not a virtualization application that you can run on top of another operating system. If you install ESX(i), it replaces the existing operating system on your server

A video is available showing the ESX(i) installation process: http://www.youtube.com/watch?v=FX1O0Q5Z82I (http://www.youtube.com/watch?v=fx1o0q5z82i). Note the steps at the end of the video for configuring the password and IP address of the server.

1. Access the VMware web site and register for a free account: https://www.vmware.com/tryvmware/index.php?p=free-esxi&lp=1 (https://www.vmware.com/tryvmware/index.php?p=free-esxi&lp=1)
2. Download the VMware ESX(i) ISO image, and then burn it to a CD-ROM. Make sure that you save the ESX(i) license key.
3. Power on your server and enter the BIOS setup utility.
4. Enable all the virtualization features in the BIOS.
5. In the BIOS, make sure that the boot order shows the CD-ROM first and the internal hard disk second.
6. Insert the CD-ROM into your server's CD-ROM drive, save the changes to the BIOS and then reboot the server.
7. Install ESX(i) on your server.
8. On the PC that you will use to access the server, open a web browser and enter the server's IP address in the URL field.
9. Install vSphere client on the PC.

Creating the Source and Destination Networks

Before you create and deploy the VMs, you should already have created the virtual networks that they will use. To create the virtual networks, you use vSphere client. You will need two networks:

On the Windows VM (virtual chassis):

- An access network that enables you to access the virtual chassis. This network connects to your corporate LAN. The default network created for this purpose in vSphere is named "VM Network".
- A card management network to act as "virtual backplane" that connects to the IxVM cards.

Two networks are pre-configured on the Ixia kernel OVA:

- IxVM Management Network, the virtual backplane.
- IxVM Test Network 1, the path for test traffic to the DUT or SUT.

During the process of creating the VMs, you map the source networks configured in the .ova template to the destination networks on your VMware server.

To create the networks, use the following procedure:

1. Open vSphere client, and display the Inventory tab.
2. Click the Configuration tab.
3. In the Hardware pane, click Networking.

4. Click Add Networking.

   The Add Networking wizard starts, and displays the Connection Type window.

5. Click Virtual Machine, then click Next.

   The Network Access window displays

6. Click Create a Virtual Switch.

   The Connection Settings window displays.

7. In the Network Label field type a name, then click Next.

8. Repeat for the additional vSwitches (networks).

Deploying the IxVM Appliances (OVAs)

The IxVM Ixia kernel is available as an Open Virtual Appliance (.ova) file, which is a template for a virtual machine. The .ova template creates a VM with a Linux kernel that has been modified by Ixia for greater performance in some testing scenarios. To use the .ova file, you use vSphere client to create a VM, and specify the .ova file as the template for the VM.

Note: Before you create and deploy the VMs, you must already have created the virtual networks that they will use in vSphere. See *Creating the Source and Destination Networks* on page 35-15.

To create a VM based on an IxVM OVA file:

1. Download the .ova file from the Ixia website. Store them in a location where they can be accessed from the ESX(i) server.

2. From the vSphere client menubar, choose FILE | DEPLOY OVF TEMPLATE.

   The Source window displays.

3. Choose DEPLOY FROM FILE:, then click BROWSE, and select the .ova file. Click NEXT.

   The OVF Template Details window displays.

4. Make a note of the Username and Password shown on the OVF Template Details window. The default usernames and passwords are:

   root/ixia123

   Click NEXT.

   The End User License window displays.

5. Click ACCEPT to accept the license, then click NEXT.

   The Name and Location window displays.

6. Enter a unique name for the VM, then click NEXT.

The Datastore window displays.

7. Select the data store where you want your VM files to be stored, then click NEXT.

   The Network Mapping window displays. On this window, you map the networks configured in the .ova template to the networks on your virtualization server.

8. Map the template's networks to your VMware networks, then click NEXT.

   The Ready to Complete window displays, showing a summary of the deployment options you have selected.

9. Choose one:

   - If you are installing using vSphere client with vCenter, the wizard displays windows enabling you to select the IP address allocation method. Choose the method you want to use.
   - If you are installing using vSphere client without vCenter, the VM is automatically created with IP address allocation set to DHCP. If you want to use static IP addresses, you must use the VM's console interface to specify the IP addresses of the VM after it boots. See Configuring static Addresses (see "Configuring Static Addressing" on page 2).

   Review the final deployment details, then click FINISH. Allow the VM several minutes to deploy.

10. Boot the VM.

11. Repeat the deployment procedure for the remaining VMs that you want to create.

Configuring Static Addressing

If you created an IxVM template using vSphere without vCenter, the VM is automatically created with IP address allocation set to DHCP. If you want to use static IP addresses, you must use the VM's console interface to specify the IP addresses of the VM after it boots.

To configure a static address on a VM:

1. In vSphere client, select the VM that you want to configure.

2. Click the CONSOLE tab.

   A console session for the VM starts, and prompts you to login.

3. Login to the VM with the user name and password configured on it when it was created.

Note: You can display the user name and password by clicking the Summary tab, then select Annotations, and then click Edit. Scroll through the window untill the user name and password displays.

4. Start the vi editor and load the IP address script for the eth0 interface by typing the following command:

```
vi /etc/sysconfig/network-scripts/ifcfg-eth0
```

5. Type I or press the INSERT key to switch to edit mode.
6. Change BOOTPROTO to static.
7. Add a new line that contains the following:

   ```
   IPADDR=<ipaddress>
   ```

   where <ipaddress> is the address you want to assign to VM's eth0 interface.

   ```
   NETMASK=<mask>
   ```

   where <mask> is the netmask to be applied to the IP address.
8. Close and save the file: Press ESC, then type: : W Q ! (colon, w(rite), q(uit), exclamation point).
9. Repeat for the eth1 interface (edit the file ifcfg-eth1).
10. Issue the following commands to bring the interfaces up:

    ```
    ifup eth0
    ifup eth1
    ```

Optimizing Performance

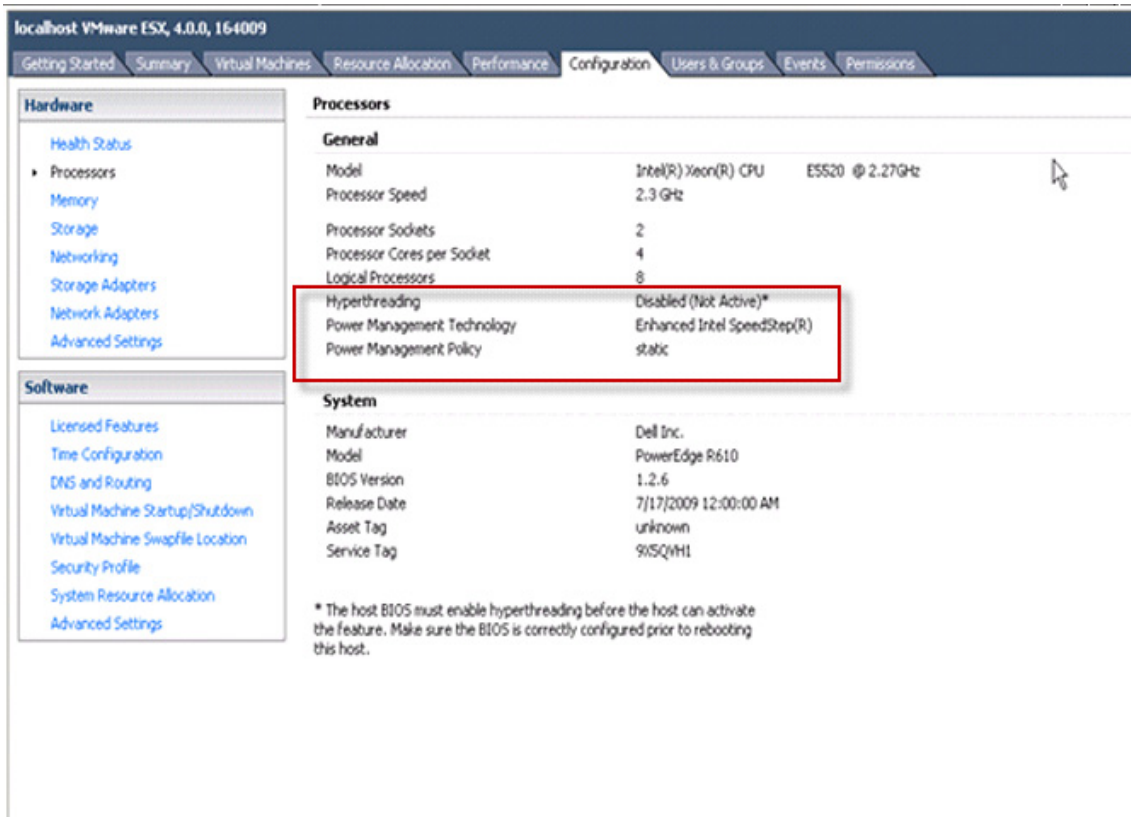
You may be able to improve performance by applying the following optimizations:

Power Management

In the ESX(i) server BIOS, ensure that Power Management is set to High Performance.

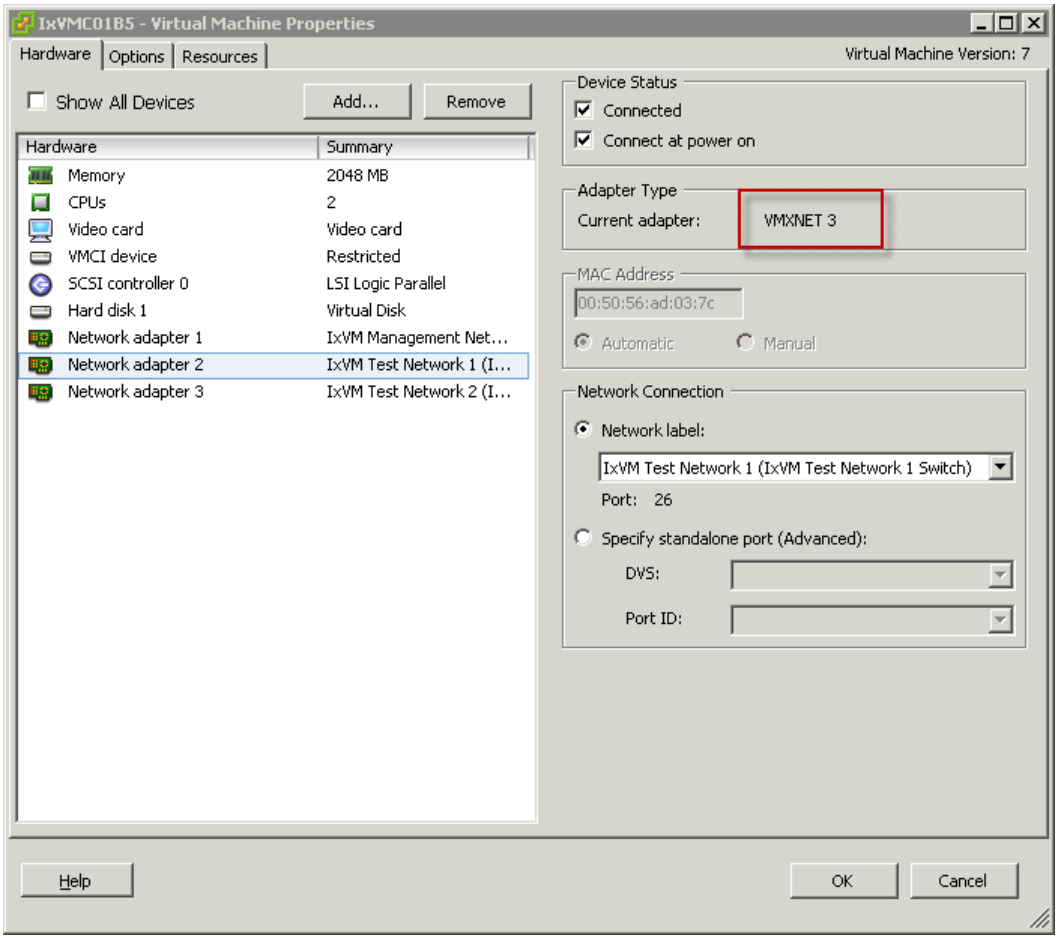
Hyperthreading

In vSphere, click the Configuration tab, then click Processors, and disable hyperthreading. Reboot the ESX(i) server.



NIC Type

In vSphere, click the Hardware tab, and change the test NIC Interface types to VMXNET3.



Visit VMware's Networking Blog for more details on how to enable Jumbo Frames: http://blogs.vmware.com/networking/

KVM Installation

For KVM deployments, Ixia supplies IxVM in two forms:

- as a script containing a self-extracting disk image (.img) that creates a new VM running the Ixia kernel

  To install using the script, follow the procedure below.

- as RPM packages that you can install on existing Linux VMs

  To install using the RPMs, follow the same procedure as for a bare metal deployment. For details see *Bare-metal (RPM) Installation* on page 35-49.

Before Installation

Before you install IxVM:

- Install and configure KVM/Qemu, if you have not already done so.

  In KVM, create the bridges (virtual networks) for the VMs you will create. You will need two bridges:

  - one for the card management traffic
  - one for the generated test traffic

Note: For details on the various switches the script accepts, run the script with the help switch before you run it to install IxVM:

```
./VM_IxVM_IXIAKernel_QemuKVM-<version>.sh -help
```

Installing IxVM on KVM

1. The script requires root-level privileges to run. Login to the KVM host using an account that has root privileges.
2. Copy the VM_IxVM_IXIAKernel_QemuKVM-<version>.sh script to the KVM host. If you are copying using WinSCP, set the Transfer Settings to Binary mode .
3. Make the script file executable:

   ```
   chmod +x VM_IxVM_IXIAKernel_QemuKVM-<version>.sh
   ```

4. Set your path to the location where you want to store the VM (or use -d to specify a different path when you run the script).
5. Run the script.

   ```
   ./VM_IxVM_IXIAKernel_QemuKVM-<version>.sh
   ```

   If you want to create the the VM in a different location, use the -d switch followed by the path:

   ```
   ./VM_IxVM_IXIAKernel_QemuKVM-<version>.sh -d <path>
   ```

   The script starts, and prompts you for a name for VM.

6. Enter a name for the VM, then press ENTER.

   The script displays a list of the bridges and virtual networks on the KVM host. You must choose two bridges or virtual networks:

   - one for the card management traffic
   - one for the generated test traffic

7. Type the name of the bridge or virtual network you want to use for the management traffic, then press ENTER.
8. Type the name of the bridge or virtual network you want to use for the test traffic, then press ENTER.

   The script unpacks the .img file and creates a VM in the current directory.

9. If you are using Virtual Machine Manager (VMM), restart it before you start the new VM.

   The password for the VM's root account is ixia123.

Note: In addition to the .img file, the script also creates an .xml file in

```
/etc/libvirt/qemu/
```

that describes the VM's hardware configuration.

If you delete the VM from VMM, only the .xml file is deleted; you must manually delete the .img file

KVM Tutorial

Introduction

KVM (Kernel-based Virtual Machine) is a full virtualization solution for Linux that takes advantage of CPU based hardware acceleration such as Intel VT or AMD-V. KVM itself exists as a kernel module and can be installed on a Linux system that has the supported set of Intel/AMD processors.

This document will demonstrate one use case of virtualization by leveraging the capabilities of the KVM Linux kernel extensions and open source virtualization software such as Red Hat's Virtual Machine Manager.

Other sources of information

http://www.linux-kvm.org

KVM Homepage.
http://libvirt.org

libvirt Homepage.

http://libvirt.org/docs.html

libvirt Documentation.

Before you begin

Please make sure that you have followed the first part of this guide: "Preparing Ixia Application Controller for KVM based IxVM" and ensure that you have VNC remote connectivity to your server.

Hardware requirements

This document focuses on the Ixia Application controller (also known as “AppServer”) and the time of writing, this is a single-processor Intel Xeon (quad core), 24GB of DDR2 RAM, two integrated GbE LAN ports, and one slim DVD-ROM drive.

Software requirements

- Windows XP SP3 ISO or CD/DVD.
- IxOS 6.20 EA SP1 + IxVM Server component.
- IxNetwork 6.20 EA SP1.

Time requirements

Start to finish, Windows XP installation, IxOS and IxNetwork installation can take from an hour to three hours (not including the time to download).

CentOS version requirements

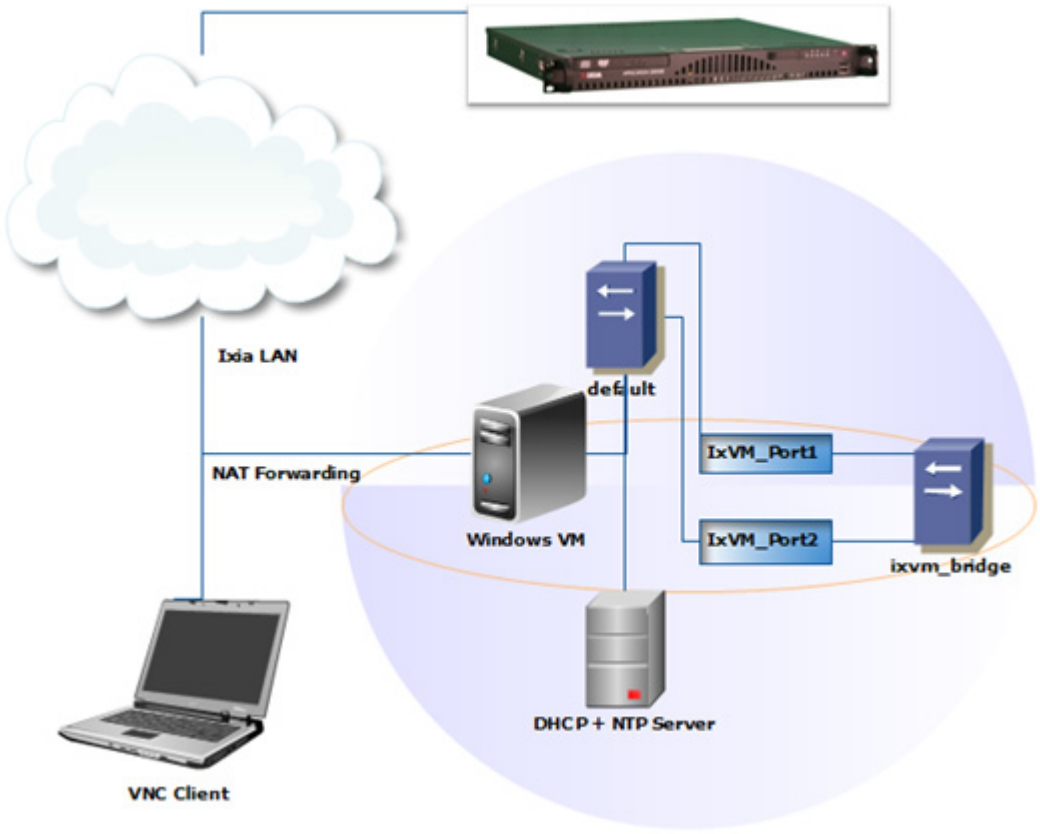
At the time of writing this document, only CentOS 5.6 is supported for IxVM – it is also important to note that performing an update (for i.e. `yum update`) will upgrade the version of CentOS to an unsupported version -- please do not run such commands when working with Ixia IxVM software.

In addition, make sure you ignore popup messages such as the following!

Topology

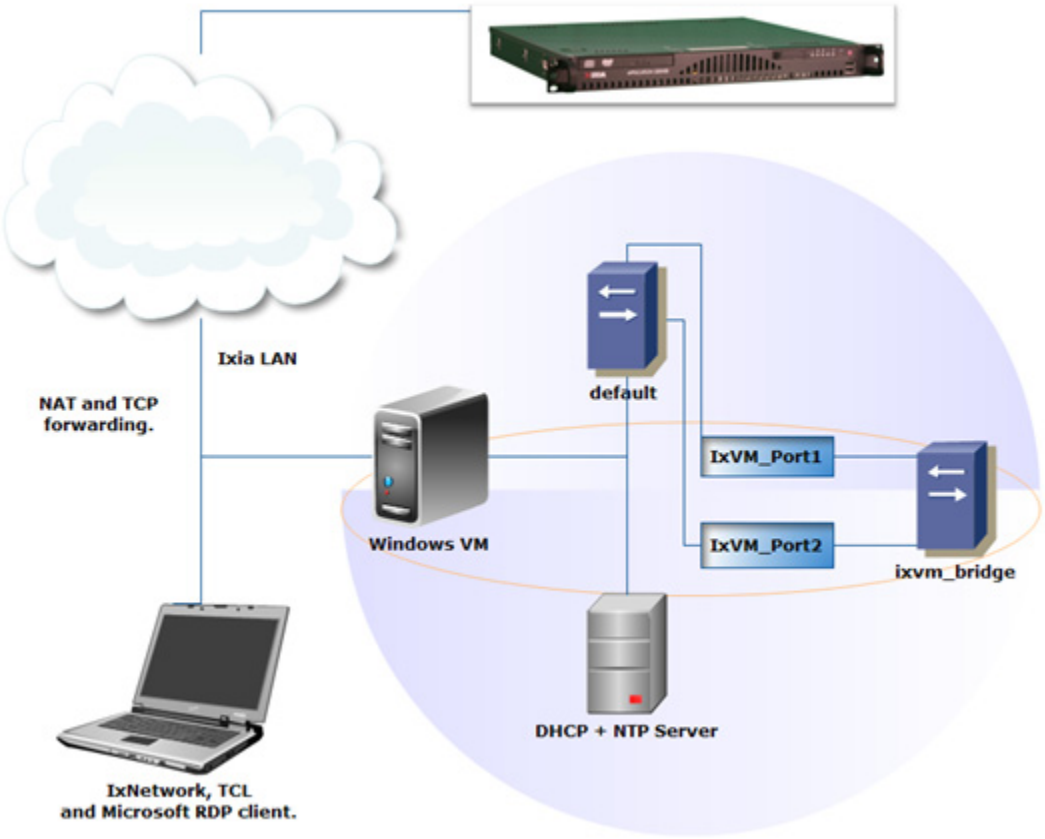
Use case 1 – Back to back test

The sphere in the following topology represents all virtualized components that are hosted by the Ixia application controller including the DHCP and NTP server.



Use case 2 – External connectivity

Building upon the previous use-case, this will focus on enabling port forwarding on the host, which will allow non-virtualized components such as IxTCL wish shell, IxNetwork and the Microsoft Remote Desktop client to remotely connect to the virtualized Windows VM without consuming CPU or memory resources on the host – this would considerably benefit customers that are conservative regarding host CPU/memory consumption by the Windows VM.



Use case 1 – Back to back test

Prerequisites

Ensure that you have the following:

- License for IxVM/IxNetwork.
- Ixia web login to access Ixia's Downloads & Updates.
- Windows XP SP3 ISO DVD (or the ISO file itself) and a genuine license key.

Introduction to libvirt daemon

Ensure that the libvirtd is running:[root@localhost ~]# service libvirtd status

libvirtd (pid xxxx) is running…

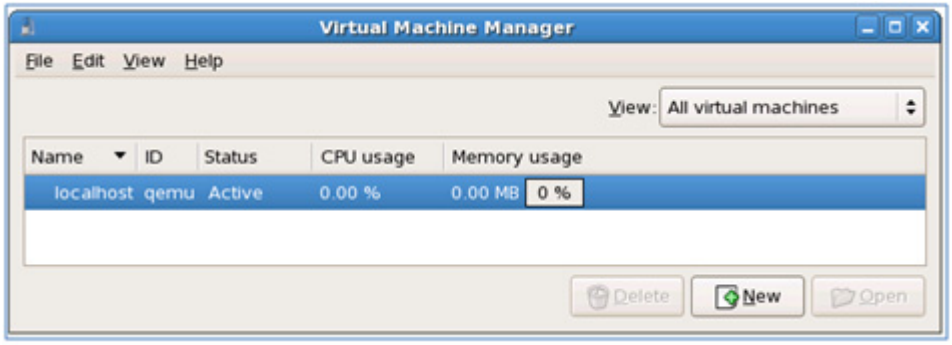
If for some reason, the service/daemon is not running, manually start of the service:

```
[root@localhost ~]# service libvirtd start
```

```
Starting libvirtd daemon:[OK]
```

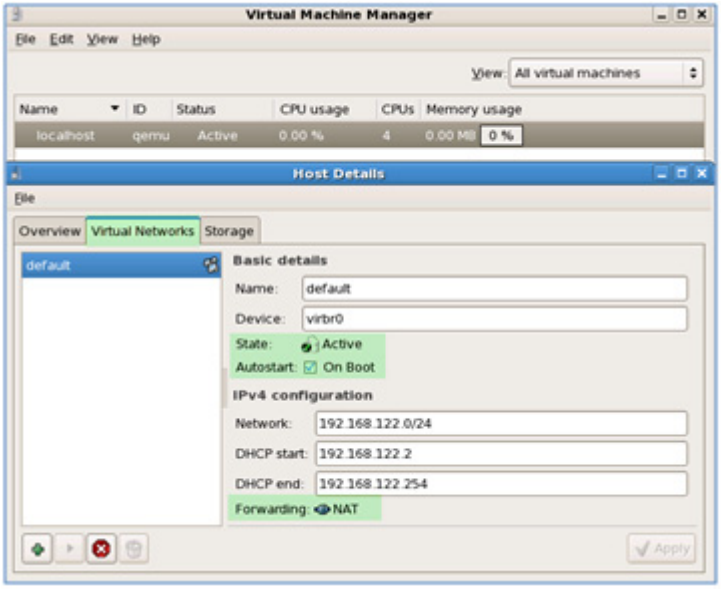
Establish the QEMU connection

Launch VMM (Virtual Machine Manager) from Applications -> Systems Tools -> Virtual Machine Manager.



Establish a connection to the QEMU/KVM hypervisor via File -> Add Connection -> Connect:

Note: Make sure the hypervisor is set to QEMU and not XEN. The default hypervisor for the GUI is XEN.



Create Ethernet Bridge for Management network

On the main dialog of Virtual Machine Manager, click on the connection to localhost (ID: qemu) to highlight it and then navigate to: Edit -> Host Details -> Virtual Networks. Click on the default network to highlight it and ensure that it is Active and enabled for “Autostart on Boot”:

VMM has utilized the Linux brctl command to setup and maintain an Ethernet bridge. The name of the device/network from libvirt’s perspective is default and the Linux Ethernet bridge identifier is virbr0; to determine the status of this bridge you can simply run: `ifconfig virbr0` from the shell. The purpose of the bridge is to simply connect different multiple Ethernet capable virtual devices together just as a real layer-2 switch would operate. In the context of this particular use case, the bridge will serve as the management network that will interconnect the Windows VM and two IxVM ports.

VMM will also provide the DHCP start and end addresses as parameters to a process called dnsmasq, which is a lightweight DHCP server (among other capabilities) to provide DHCP addresses to all connected hosts on the default bridge, and for this use case this will translate to the Windows VM and the eth0 interface of the two IxVM ports.

For more information on libvirt networking:

- http://wiki.libvirt.org/page/Networking
- http://wiki.libvirt.org/page/Libvirtd_and_dnsmasq

Create Ethernet bridge for test ports

To establish a dedicated and isolated bridge between the IxVM ports, create a new virtual network (click on the button with the + icon):

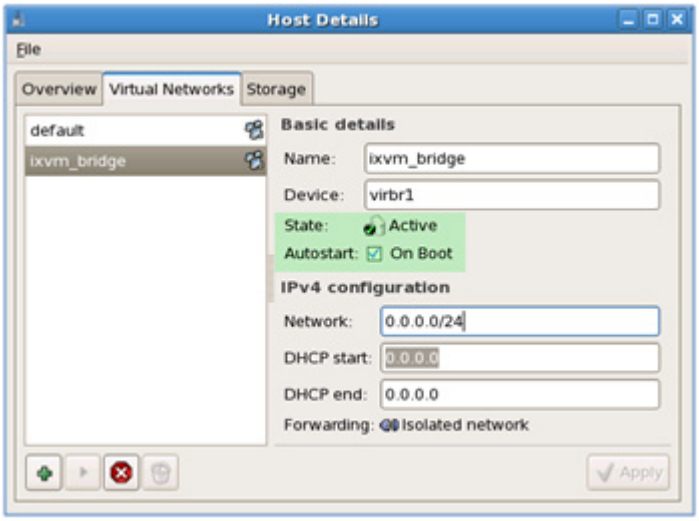
Network Name: ixvm_bridge

Network: 0.0.0.0/24

DHCP Start/End range: 0.0.0.0

Physical network: Isolated virtual network

Ethernet Bridge: ixvm_bridge should now be running and DHCP (through dnsmasq) should NOT be providing out any addresses since the range is null:



Now, close VMM and create a new shell using Terminal (from Applications -> Accessories).

Note: This step assumes you have a separate file system mounted under / nobackup as defined in the first document. If you need to mount this directory, you must do so via `mkdir /nobackup` && `mount /dev/sda2 /nobackup`.

Create the following directories (if they do not already exist):

```
[root@localhost /]# cd /nobackup
[root@localhost nobackup]# mkdir libvirt
[root@localhost nobackup]# cd libvirt/
[root@localhost libvirt]# mkdir images
[root@localhost libvirt]# cd images
[root@localhost images]# pwd
/nobackup/libvirt/images
```

Download the latest KVM IxVM image into the above directory and ensure executable permissions for root:

```
[root@localhost images]# chmod u+x
VM_IxVM_IXIAKernel_QemuKVM-1.0.0.68.sh
```

Instantiate IxVMPort1

```
Run the script to create instance for IxVM_Port1:
[root@localhost images]# ./VM_IxVM_IXIAKernel_QemuKVM-
1.0.0.68.sh
Host System: CentOS
```

```
Creating virtual machine
Enter virtual machine(domain) name: IxVM_Port1
 Setting up network configuration
        NETWORKS_LIST
default
ixvm_bridge
Enter management network name: default
Enter test network name: ixvm_bridge
Stopping libvirtd daemon: [  OK  ]
Starting libvirtd daemon: [  OK  ]
VIRTUAL MACHINE INFO
Machine name: IxVM_Port1
Management NIC: default
Test NIC: ixvm_bridge
##########################################################
# [warn]: libvirt daemon has just been restarted in order
that  #
# new configuration to take effect; note that it may be #
# needed to restart Virtual Machine Manager also        #
##########################################################
```

Note: The script has essentially created a new QEMU-KVM instance and connected the new VM's eth0 virtual interface to the default network and eth1 to the ixvm_bridge (created earlier). When the IxVM_Port1 starts, it will attempt to retrieve an IP address from the DHCP server through eth0 interface.

Instantiate IxVMPort2

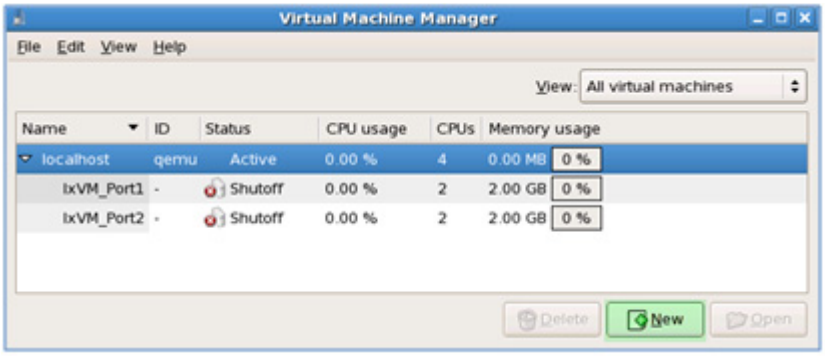
```
Run the script again for IxVM_Port2:
[root@localhost images]# ./VM_IxVM_IXIAKernel_QemuKVM-
1.0.0.68.sh
Host System: CentOS
Creating virtual machine
Enter virtual machine(domain) name: IxVM_Port2
 Setting up network configuration
NETWORKS_LIST
default
ixvm_bridge
Enter management network name: default
Enter test network name: ixvm_bridge
```

```
Stopping libvirtd daemon: [  OK  ]
Starting libvirtd daemon: [  OK  ]
VIRTUAL MACHINE INFO
Machine name: IxVM_Port2
Management NIC: default
Test NIC: ixvm_bridge
#########################################################
# [warn]: libvirt daemon has just been restarted in order
that  #
# new configuration to take effect; note that it may be #
# needed to restart Virtual Machine Manager also        #
#########################################################
```

Note: This second VM is connected to the same default network and ixvm_bridge. The two VMs will be able to talk to each other and to the Windows VM via the default network; moreover, the two VMs will have a private and isolated connection to each other via the eth1 interfaces and ixvm_bridge.

Create and instantiate IxVM management VM

Go back to the VMM GUI, highlight the “qemu” connection and click on “New” to create a new VM instance:



Note: The VM status for both instances is in the Shutoff state and while they are in this state they will not consume any host CPU cycles as it will need all available processing power to complete the following task of instantiating a Windows VM as fast as possible.

Name: IxVM

Virtualization method: Fully virtualized (CPU architecture: x86_x64)

Hypervisor: KVM

Installation method: Local installation media.

OS Type:Windows

OS Variant:Microsoft Windows XP (x86_64)

Installation media:<Select ISO or CD-ROM>

Storage:File (disk image)

Location:/nobackup/libvirt/images/IxVM.img

Size:60000 MB

Allocate:Uncheck (this option will allocate disk space on the fly as needed).

Network:Virtual Network -> Network: default.

Memory

Max memory:4000 MB

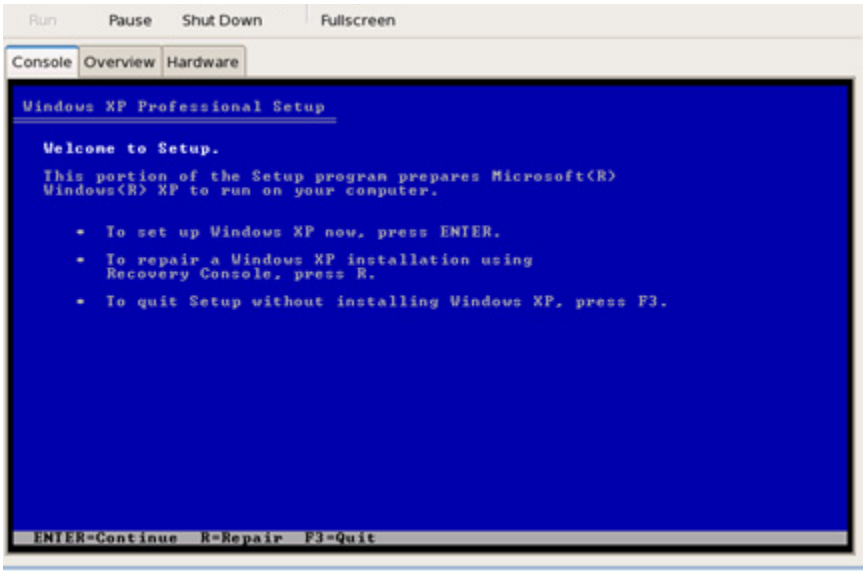
Startup mem.:1024 MB

Virtual CPUs:2

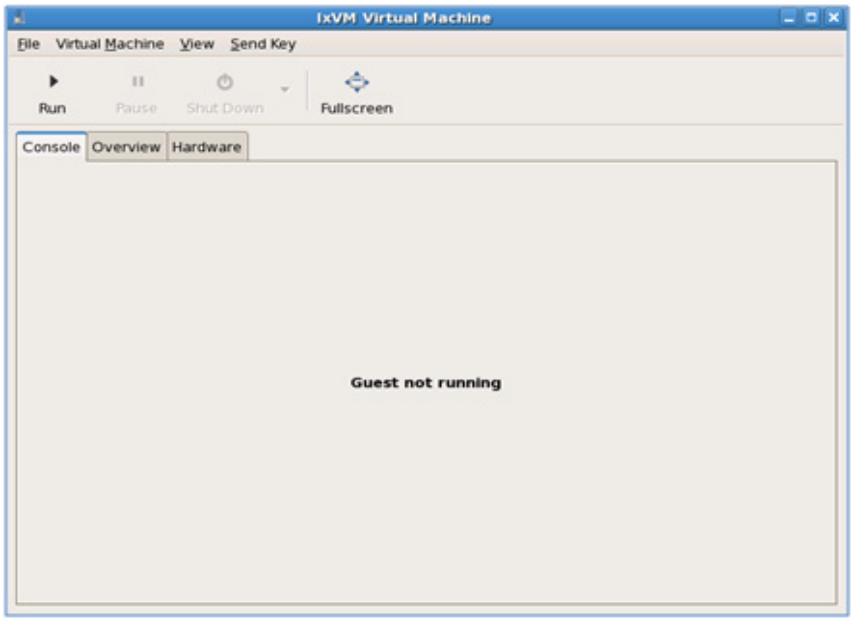
Click on “Finish” in the last dialog to create and launch the VM.

Install Windows XP

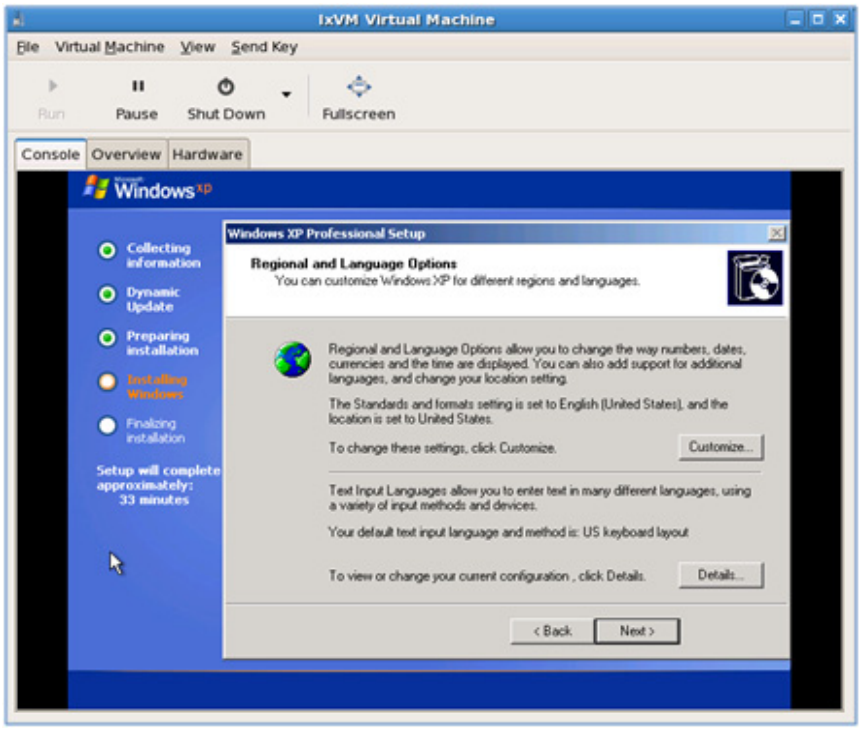
Once the VM has been successfully instantiated, follow and select the default options of installing Windows:



Upon the successful completion of the Windows Install, the VM will shut down and you will need to manually restart the VM (click on “Run”):



Enter the default settings and you will be asked to input your Windows license key:



Computer name:IxVM

Administrator password:<leave it blank>

Confirm password:<leave it blank>

Network settings:Typical

Workgroup:“No, this computer is not on a network…” WORKGROUP

Note: Leaving the password blank is optional but will provide an advantage as it will allow the Windows VM to login automatically without a blocking login prompt.

Select the “Not right now option”:

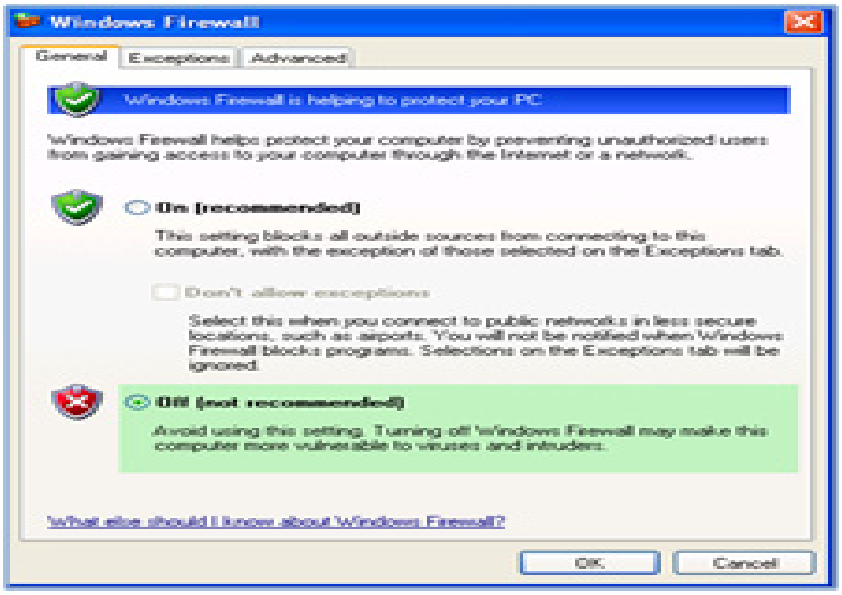
Select, “No, this computer will connect directly to the Internet”:

Select a user name (for i.e. “IxVM User”):

Customize Windows XP

By default, Windows XP will display alerts relating to the status of the Firewall, Windows Automatic Updates and Virus Protection. Since none of these services are required, disable the alerts:

Start -> Control Panel -> Security Center -> “Change the way Security Center alerts me”



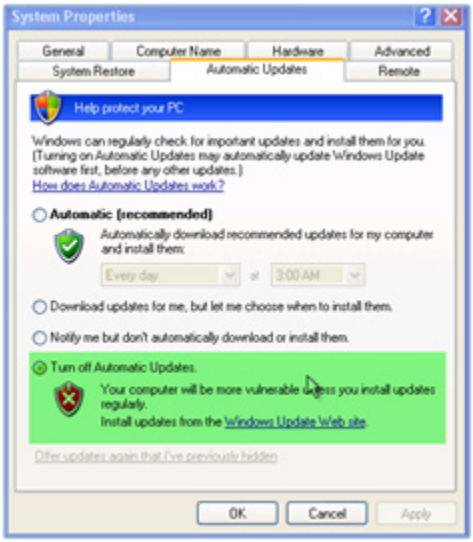
Make sure all checkboxes are unchecked, and then click OK:

Ensure the Windows Firewall is disabled (since it will interfere with IxVM management traffic):

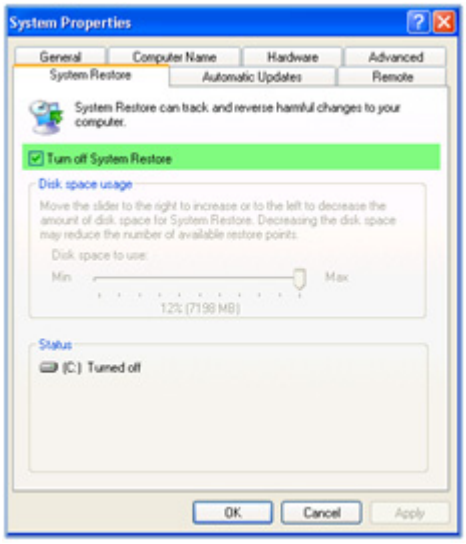
Start -> Control Panel -> Network and Internet Connections and select “Off” and click on OK to close the dialog.

Ensure the Automatic Updates functionality is turned off:

In the Start window, right click on “My Computer” -> “Properties” and navigate to the “Automatic Updates” tab. Select: “Turn off Automatic Updates” then “Apply”:



While in the System Properties dialog, navigate to “System Restore” and ensure that System Restore is disabled then “Apply” and “OK”:



Install IxOS and IxNetwork

From the Windows VM instance, download and install IxOS 6.10 EA SP2 and IxNetwork 6.10 EA (respectively). You will be asked to reboot after the IxOS installation and once more after the IxNetwork 6.10 EA installation. In addition, please ensure that that the appropriate IxVM/IxNetwork licenses are also installed.

Note: When installing IxOS, make sure Client, IxVMServer and Tcl Server are selected to be installed. In the “Custom setup” dialog, you will be given a choice over Demo Server or IxVM Server. Select IxVM Server.

Install and configure NTP server on the host

For this use case, we will be using the Linux host as the NTP server. To do this, the NTP package should be installed:

```
[root@localhost ~]# yum install ntp
[root@localhost ~]# service ntpd start
Starting ntpd:[ OK ]
```

To allow the host to serve NTP requests, modify /etc/ntp.conf and append the following line:

```
restrict 192.168.122.0 mask 255.255.255.0 nomodify notrap
```

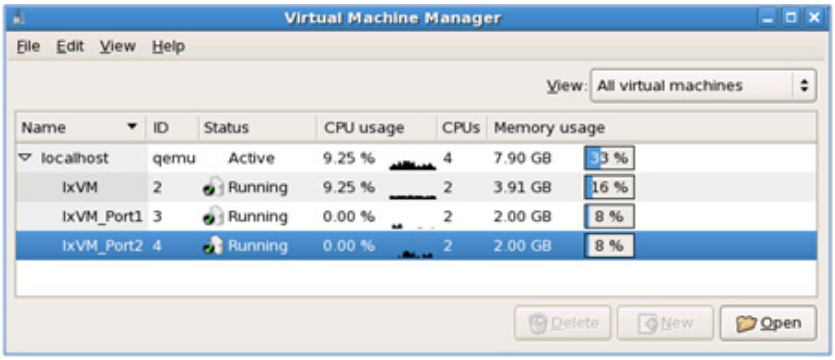
Note: 192.168.122/24 is the default network for libvirt and since we have used the default network for the management bridge, the entry for /etc/ntp.conf should match.

Allow the NTP service to run at boot-time and manually restart the service for the new modifications to take affect:

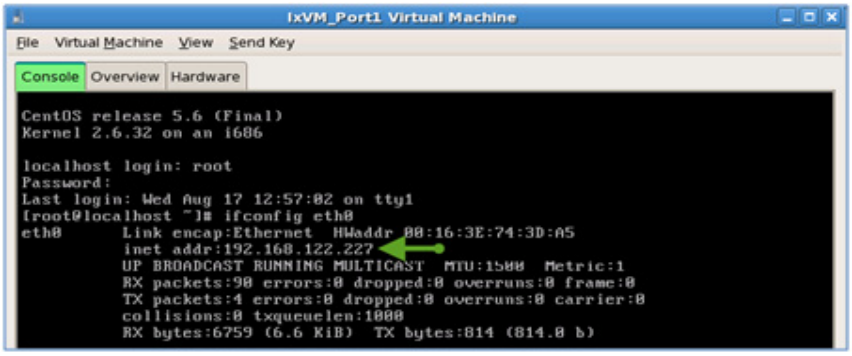
```
[root@localhost ~]# chkconfig ntpd on
[root@localhost ~]# service ntpd restart
Shutting down ntpd:[ OK ]
Starting ntpd:[ OK ]
```

Instantiate IxVM test ports

Now that the Windows VM has been successfully established, it's time to bring up the IxVM ports. In the Virtual Machine Manager main GUI, right click on IxVM_Port1 and click on Run (do the same for IxVM_Port2). This will take about 2-5 minutes for the ports to boot up, initialize and obtain an IP address from DHCP.

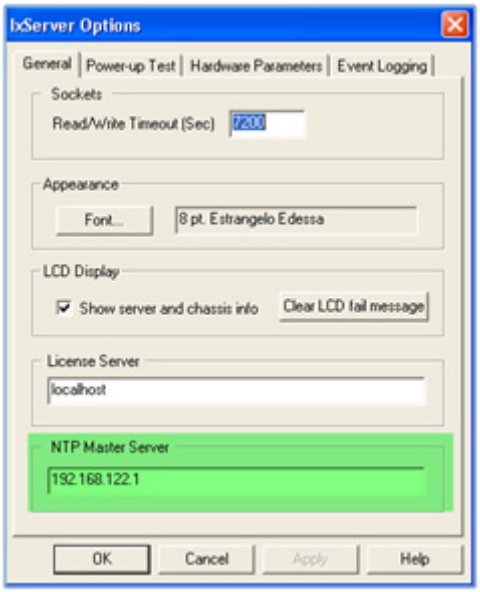


Double-click on IxVM_Port1 (for console); login as root and make a note of the IP address for eth0 (do the same for IxVM_Port2):



Note: At the time of writing, the password for root is ixia123.

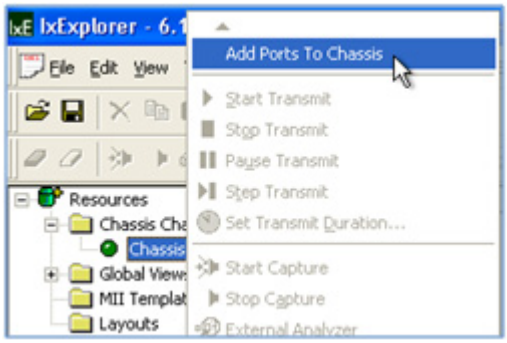
Go back into VMM, double-click on the Windows VM and navigate to IxServer -> Tools -> Options. Once you are in the IxServer Options menu, set the NTP Master Server to 192.168.122.1 (the host):



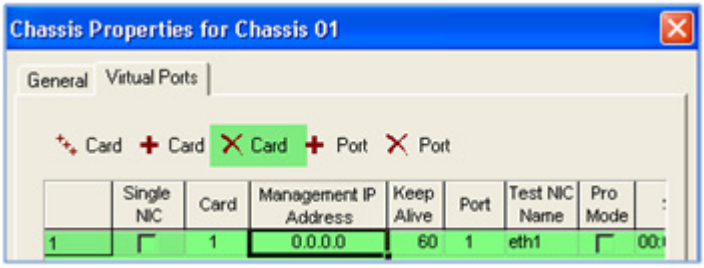
For the changes to take affect; restart IxServer, launch IxExplorer (by connecting to the localhost). Stop the firewall:

```
[root@localhost ~]# /etc/init.d/iptables stop
Flushing firewall rules: [  OK  ]
Setting chains to policy ACCEPT: filter [  OK  ]
Unloading iptables modules: [  OK  ]
[root@localhost ~]#
```

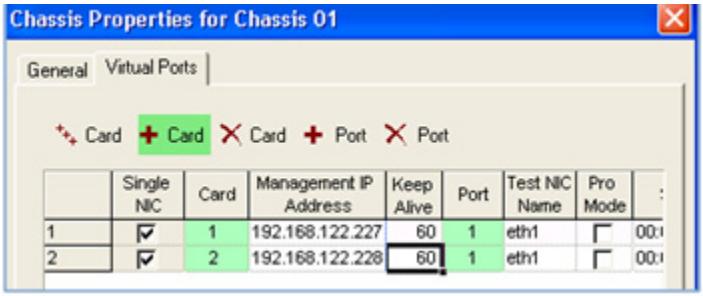
Right click on the chassis (should be in a green state) and click on “Add Ports to Chassis”:



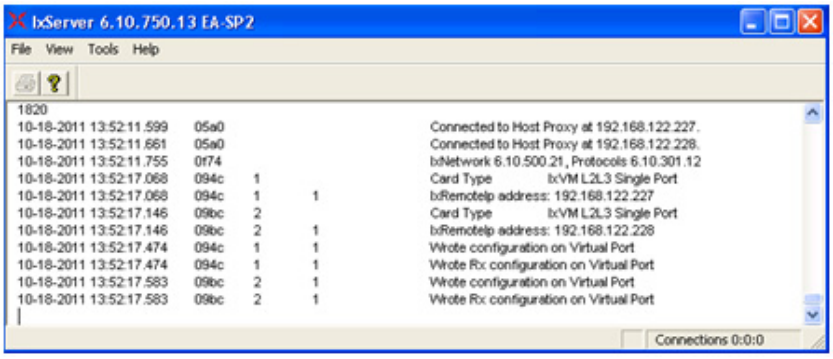
The initial virtual ports dialog contains a default IxVM card/port; delete this by highlighting it and clicking on the following button:



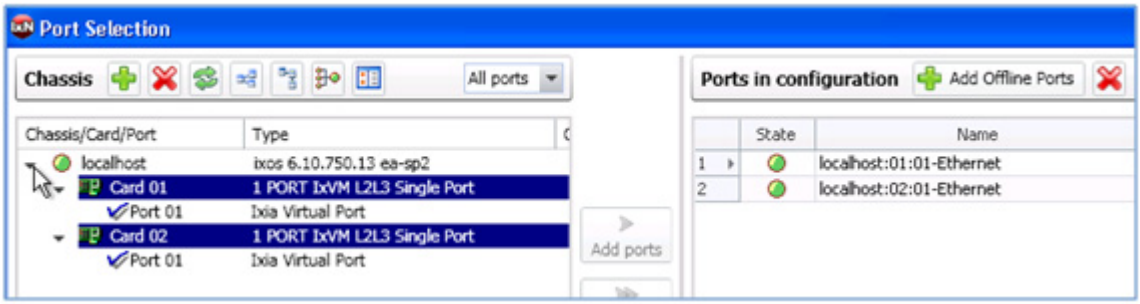
Then add your new cards, apply and OK:



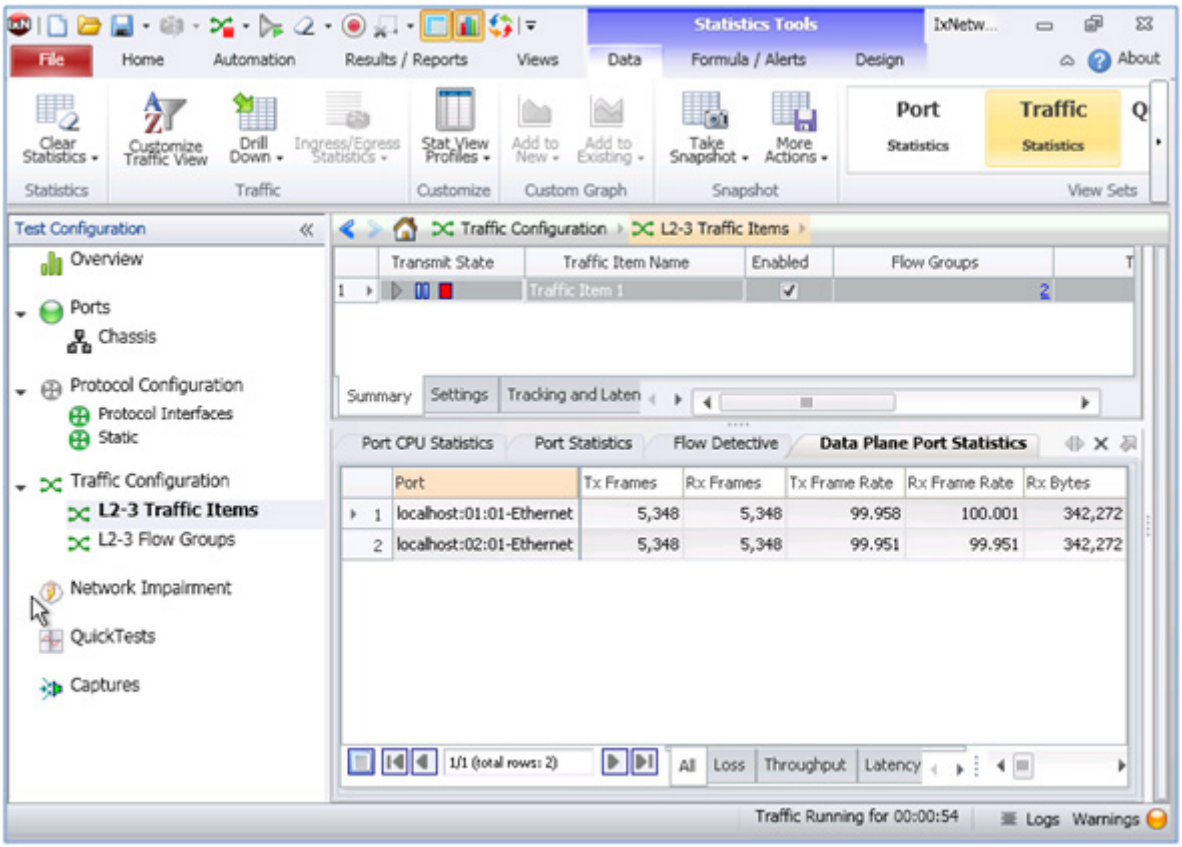
A successful IxVM connection should appear as the following:



Launch IxNetwork 6.10, use the localhost as the chassis, and add both IxVM ports.



Create a back-to-back configuration by adding IPv4/IPv6 protocol interfaces on each port and send some test traffic through at low-rates (for e.g. 100 pps) to verify traffic:



To look at the raw counters (vnet2 maps to -> IxVM_Port1:eth1 and vnet4 -> IxVM_Port2:et1),

```
[root@localhost ~]# ifconfig vnet2
vnet2     Link encap:Ethernet  HWaddr FE:16:3E:58:F0:42
UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
```

```
RX packets:1561980 errors:0 dropped:0 overruns:0 frame:0
TX packets:1558030 errors:0 dropped:0 overruns:635040
carrier:0
collisions:0 txqueuelen:500
RX bytes:93718728 (89.3 MiB)  TX bytes:92541680 (88.2
MiB)
[root@localhost ~]# ifconfig vnet4
vnet4     Link encap:Ethernet  HWaddr FE:16:3E:58:74:0E
UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
RX packets:1882045 errors:0 dropped:0 overruns:0 frame:0
TX packets:1352794 errors:0 dropped:0 overruns:513842
carrier:0
collisions:0 txqueuelen:500
RX bytes:112922556 (107.6 MiB)  TX bytes:80227696 (76.5
MiB)
[root@localhost ~]#
```

Use case 2 – External connectivity

Prerequisites

Ensure that you have the following:

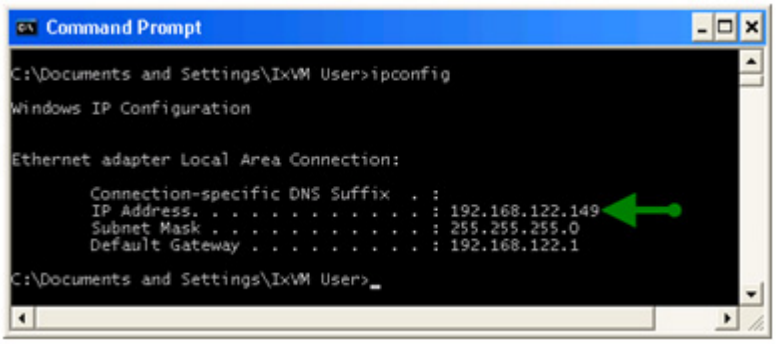
- Use-case 1 successfully working and IxVM ports established (back-to-back).
- IxNetwork client installed on your Windows laptop (or an external AppServer).

Introduction to xinet.d

In the open source Linux world, xinetd, the eXtended InterNET Daemon is a process-daemon that provides services such as access control, logging, cron services, and port forwarding. Since this service is a fast, secure and efficient means of forwarding traffic from the Windows VM to the external client, xinetd will suffice.

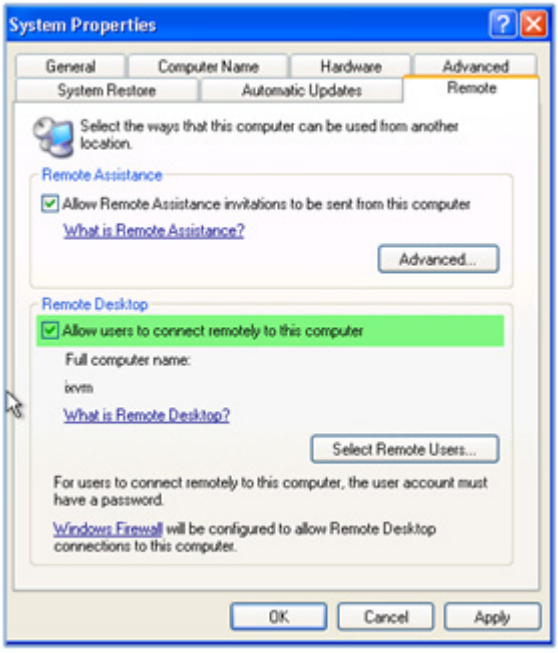
Discover the Windows VM IP

From the VMM GUI, navigate to the Windows VM console, enter the command prompt (Start -> Run -> cmd) and make a note of the IPv4 address that it is assigned (in the following case, the address is 192.168.122.149):

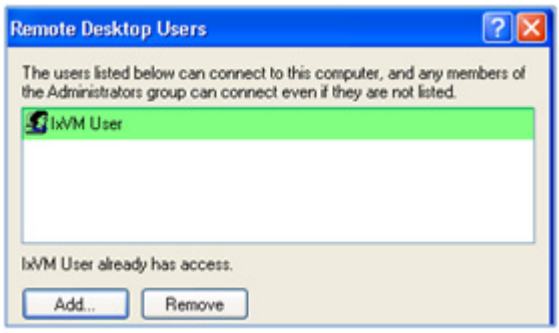


Enable remote desktop for IxVM User

Goto System Properties (from Start -> Run -> right click on “My Computer”), navigate to the “Remote” tab and enable “Allow users to connect remotely to this computer”.



Click on “Select Remote Users…” and add IxVM User:



Install xinetd on the host

```
[root@localhost init.d]# yum install xinetd
…
Installed:
  xinetd.x86_64 2:2.3.14-13.el5
Configure common Ixia TCP ports as xinetd services
```

On the host, edit the /etc/services file and at the end of file (under "# Local services") add the following three entries:

```
ixostcl4555/tcp# IxOS TCL server.
ixnetclient6809/tcp# IxNetwork server.
ixnettcl8009/tcp# IxNetwork TCL server.
```

Create port-forwarding definition file for xinetd

Create a file called ixia in the /etc/xinetd.d directory with the following contents (making a note of 192.168.122.149 as the destination for all services):

```
service ixostcl
{ flags = REUSE
     socket_type = stream
     wait = no
     user = root
     server = /usr/bin/nc
     server_args = 192.168.122.149 4555
     log_on_failure += USERID
}
service ixnetclient
{
     flags = REUSE
     socket_type = stream
```

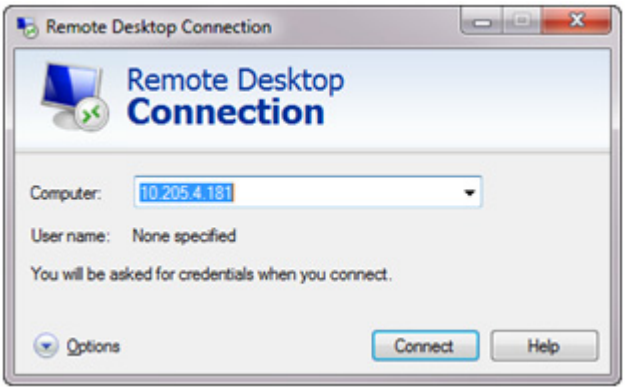
```
        wait = no
        user = root
        server = /usr/bin/nc
        server_args = 192.168.122.149 6809
        log_on_failure += USERID
}
service ixnettcl
{
        flags = REUSE
        socket_type = stream
        wait = no
        user = root
        server = /usr/bin/nc
        server_args = 192.168.122.149 8009
        log_on_failure += USERID
}
service ms-wbt-server
{
        flags = REUSE
        socket_type = stream
        wait = no
        user = root
        server = /usr/bin/nc
        server_args = 192.168.122.149 3389
        log_on_failure += USERID
}
```

Save and exit the editor, ensure executable permissions for the ixia file, allow xinetd to be automatically restarted on boot-up and manually start the xinet.d service:

```
[root@localhost init.d]# chmod +x ixia
[root@localhost init.d]# chkconfig xinetd on
[root@localhost init.d]# service xinetd start
Starting xinetd: [  OK  ]
```

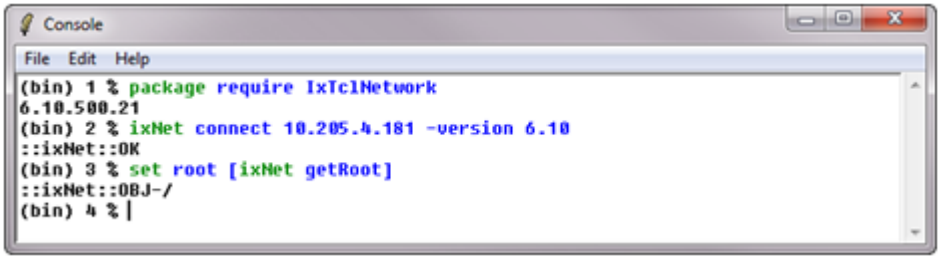
Test Microsoft Remote Desktop connection

From your laptop client, connect to your server, for example:



Test IxNetwork TCL server

From your laptop client, connect to your server, for example:



Bare-metal (RPM) Installation

The sequence for a bare-metal installation of IxVM with RPMs is as follows:

1. Download one of the supported Linux OSes, and install it on your bare metal server.
2. Download the IxVM RPMs, and install them on the bare metal server.
3. Install IxServer, Discovery Server, and IxAdmin on a Windows PC.

The following sections describe each of these steps.

After you have completed the steps, you can begin using the virtual Ixia ports with your Ixia testing application.

Installing Linux

Download one of the supported Linux distributions, and install it on your bare metal server. See Requirements (see "Requirements" on page 2) or the release notes for the list of supported Linux distributions.

For whichever distribution you choose, you must use the default (unpatched) kernel.

Installing IxVM Server, IxExplorer, and IxNetwork

For a bare-metal Linux deployment, you install IxServer, IxExplorer, IxNetwork, Discovery Server, and IxAdmin on a 32-bit Windows XP PC that can access the bare-metal server.

- IxServer and IxExplorer are packaged with IxOS and are offered as options during IxOS installation.
- IxNetwork, Discovery Server, and IxAdmin have their own installers, and you install them as you would if you were going to use them with a physical Ixia chassis.

All components can be downloaded from Ixia's website.

To install IxVM Server, IxExplorer, IxNetwork, Discovery Server, and IxAdmin:

1. Download the IxVM IxOS installer, and install IxOS on the Windows PC. Make sure that you select the following two components:
   - IxServer
   - Client
2. Download the IxNetwork installer, and install IxNetwork on the Windows PC. Select all the components, including the one marked IxVM Server (an IxNetwork-specific component required for IxVM, not to be confused with the IxOS IxVM Server component).
3. Download and install Ixia Discovery Server on the Windows PC.
4. Download and install IxAdmin Client on the Windows PC.

Installing the IxVM RPM Packages

Three IxVM components must be installed on the bare metal server:

- IxOS-VM
- IxNetwork-VM
- IxAdminAgent-VM

All three components are supplied as RPM packages compiled for the supported Linux distributions.

To install the IxVM RPM packages:

1. Log on to the bare-metal server under an account with admin privileges.
2. Download the IxVM RPM packages appropriate for the Linux distribution installed on the bare metal server.
3. Type the following to install the IxOS-VM package:

   `rpm –i <ixvm>.rpm`

   where <ixvm> is the name of the IxOS-VM RPM package.
4. Type the following to install the IxNetwork-VM package:

   `rpm –i <ixnetwork>.rpm`

   where <ixnetwork> is the name of the IxNetwork-VM RPM package.
5. Type the following to install the IxAdminAgent-VM package:

   `rpm –i <ixadminagent>.rpm`

   where <ixadminagent> is the name of the IxAdminAgent-VM RPM package.
6. Start the software agent using either of the following methods:
   - Reboot the machine
   - Enter: `/etc/init.d/ixvm start`
7. Enter `ps -e` to verify that `bin/InterfaceManager` is running.
8. After installation, if you need to find the build numbers of the RPMs that are installed, you can use the following commands:
   - IxOS-VM: `rpm –qa ixvm`
   - IxNetwork-VM: `rpm –qa ixnetwork_ixvm`
   - IxAdminAgent-VM: `rpm –qa ixadminagent`

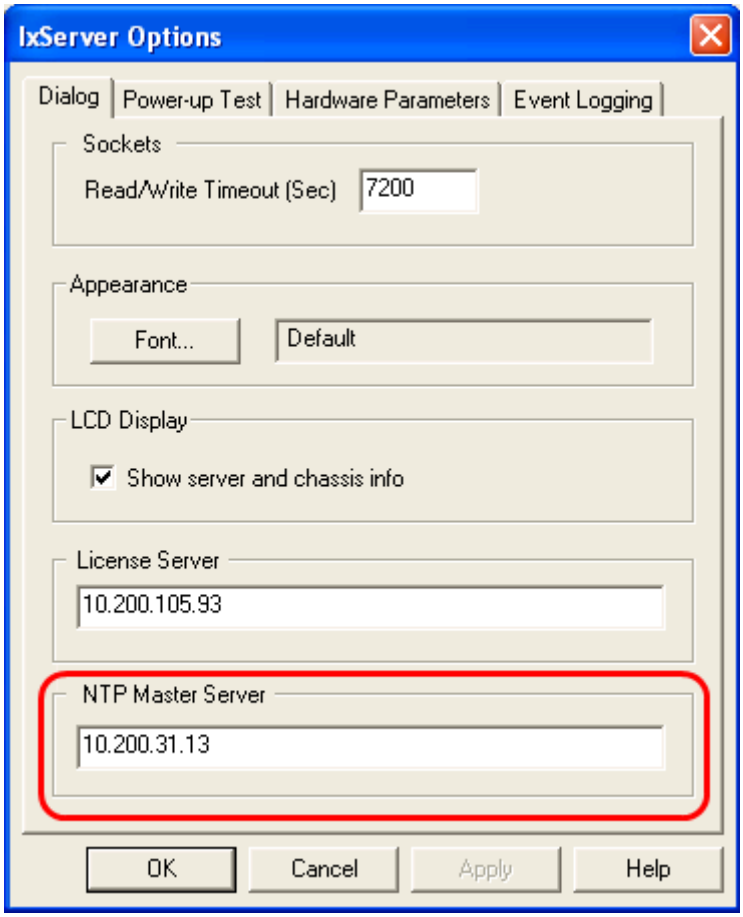
Configuring NTP

If you are using IxVM ports from different instances of IxVM Server, or you are using a combination of IxVM ports and Ixia hardware ports, you must configure a common NTP time source so that traffic can be synchronized among the ports.

The NTP time source must be configured in IxVM server (for IxVM ports) and in IxOS server (for hardware ports).

To configure an NTP time source:

1. Open IxVM Server or IxServer.
2. On the menu bar, click `TOOLS| OPTIONS | DIALOG`.
3. In the `NTP MASTER SERVER` field, specify the `NTP` server.
4. Click OK.



NTP server options for IxVM cards

The IxVM-enabled version of IxServer supports a number of options for using an NTP time server. To configure NTP for IxVM:

1. Display the copy of IxServer running on the IxVM Windows controller host.
2. Click `TOOLS| OPTIONS | DIALOG`.
3. In the NTP Master Server field, enter one of the following:
   - IP address of an NTP server that is reachable by the IxVM cards
   - Hostname of an NTP server (the host name must be resolvable by DNS and reachable by the IxVM cards)
   - 0, to disable the IxVM cards from sourcing NTP through Ixia applications. If you use this option, you must supply a time source to the IxVM cards by some other means.

Single-port vs. Multi-port Cards

There are two types of IxVM virtual load modules: single-port and multi-port.

- Single-port load modules have one interface (virtual port) for generating test traffic.
- Multi-port load modules have multiple interfaces for generating test traffic.

All IxVM virtual load modules require one interface for management traffic, and at least one interface to generate test traffic.

- Single-port modules are virtual appliances operating in a mode that supports the management interface and one test traffic interface. On a single-port card, all the resources are dedicated to a single test port, which can yield higher per-port performance than on a multi-port card (because there is only one test port). On a single-port card, the eth0 interface is the card management interface, and eth1 is the single test traffic interface. With a single-port card, the test traffic and the emulated routing topology traverse a single virtual network.
- Multi-port modules are virtual appliances operating in a mode that supports the management interface and one or more test traffic interfaces. On a multi-port card, the resources are distributed across multiple test ports. On a multi-port card, eth0 interface is the card management interface (same as a single-port card), and eth1 through ethN are the multiple test interfaces. With a multi-port card, the test traffic and the emulated routing topology may traverse multiple virtual networks.

Some test traffic and routing protocols are only supported on single-port cards, while others are supported on either type.

One virtual chassis can control up to 32 virtual cards.

Converting Single-port cards into Multi-port cards

You can convert a single-port card into a multi-port card, or add ports to an existing multi-port card. There are three tasks required for this process:

1. For each test port that you want to add, create an additional test network.
2. Add the additional test ports to the VM card.
3. In the test application (IxExplorer, IxNetwork, or IxLoad), add or discover the ports added to the card.

Step 1. Create the Additional Test Networks

If you are adding ports to a multi-port card, each port should have its own network in vSphere. Use the procedure below to create an additional test network.

To create an additional test network in vSphere:

1. Login to vSphere client.
2. Select the ESX(i) host.

3. Click the CONFIGURATION tab.
4. In the Hardware area, click NETWORKING.
5. Click ADD NETWORKING (upper right).

   The Add Network Wizard displays, with the Connection Type set to Virtual Machine.
6. Click NEXT.

   The Network Access pane displays.
7. Select CREATE A VIRTUAL SWITCH, then click NEXT.
8. In the NETWORK LABEL field, enter a label for the additional test network, then click NEXT, then click FINISH.

Step 2. Add Ports to the Card

To add ports to an IxVM card, use the procedure below.

To add ports to an IxVM card:

1. Login to vSphere client.
2. Select the VM you want to add ports to.
3. SHUT DOWN or POWER OFF the VM.
4. Select the VM, and then click EDIT VIRTUAL MACHINE on the Getting Started tab.

   The Virtual Machine Properties window displays.
5. On the Hardware tab, click ADD.

   The Add Hardware wizard displays, with the Device Type pane selected.
6. Select Ethernet Adapter, then click NEXT.

   The Network Connection pane displays.
7. In the Adapter Type field, select VMXNET3.
8. In the Network Label field, select the destination test network, then click NEXT, then click FINISH.
9. Repeat steps 4-8 for any additional ports you want to add.
10. Click OK to close the window.
11. Power on the VM.

Step 3. (IxExplorer): Adding a Multi-port Card

In IxExplorer, after adding ports to a card, you must manually add (or re-add) a card to the card list.

To manually add a multi-port card to an IxVM chassis:

1. In vSphere client, select the chassis, click CONSOLE, and login to Windows.
2. Start IxExplorer.
3. Right-click the chassis, and then select PROPERTIES.

4. Select VIRTUAL PORTS.
5. If the card you added ports to is already in the card list, select the card, and remove it.
6. Click the MULTI-ADD CARD (the +++Card) button.

   IxExplorer adds the card as a multi-port card (the SINGLE-NIC checkbox is not checked).
7. Select the card, then click ADD PORT. Repeat for each additional port you are want to add.
8. Click OK.

   In the chassis/card/port list, the card should now display multiple ports.

Step 4. (IxNetwork): Discovering a Multi-port Card

In IxNetwork, after adding ports to a card, you use Discovery Server to automatically add the card and its ports to the chassis/card/port list.

To discover a card in IxNetwork:

1. After you have added ethernet adapters to the VM, you must rebuild the chassis in IxNetwork, in order for Discovery Server to discover them.
2. In vSphere client, select the chassis, click CONSOLE, and login to Windows.
3. Start IxNetwork.
4. Select TEST CONFIGURATION.
5. Select PORT MANAGER.
6. Click ADD PORTS.
7. If the chassis is in the chassis list, select it. If the chassis is not in the list, add it.

   The Add Virtual Chassis window displays.
8. Make sure the PERFORM AUTOMATIC DISCOVERY is checked, then click AUTOMATIC.

IxNetwork triggers Discovery Server to discover IxVM cards. After the discovery process is complete, the card should now display multiple ports in the chassis/card/port list.

Sample Configuration

This section describes the steps in creating a sample IxVM configuration. You can use the steps in this section as a guide in creating your own configuration.

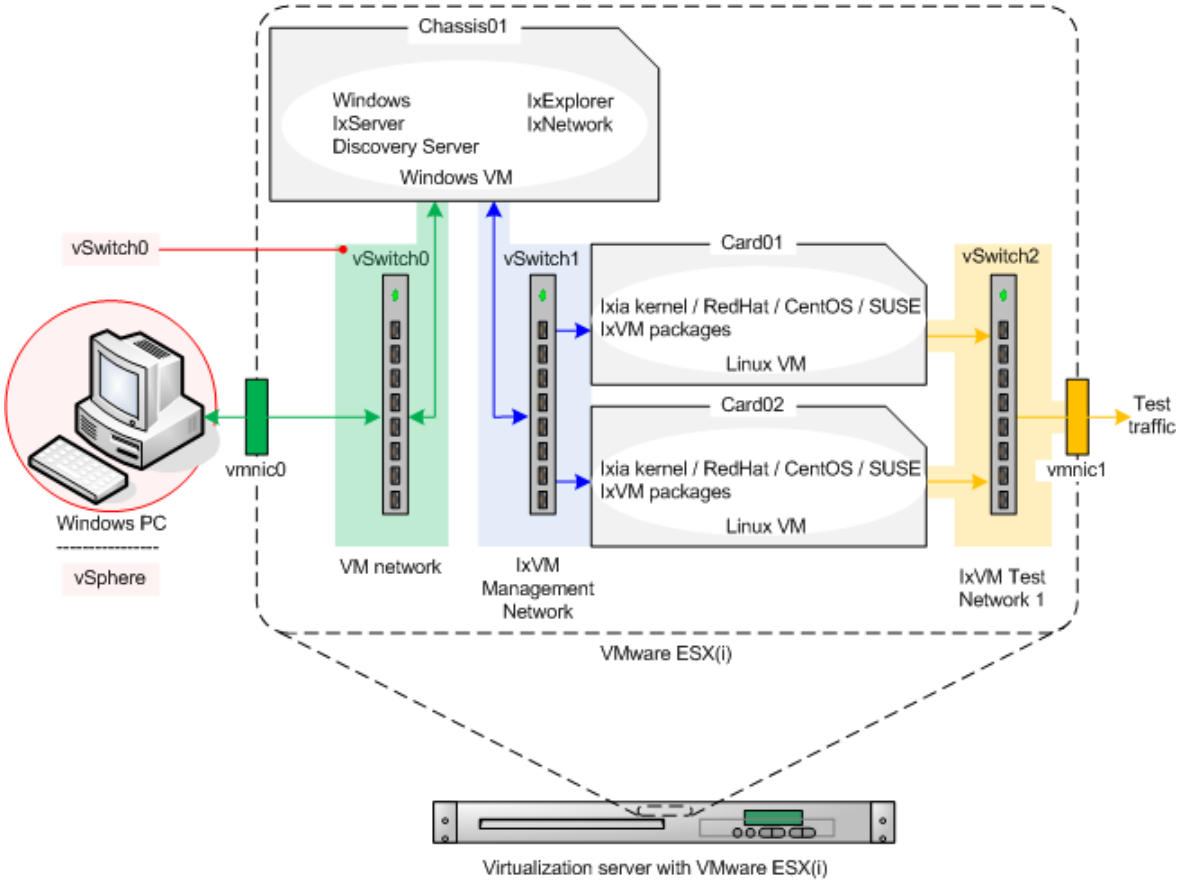
Step 1. Install vSphere

If you have not already installed vSphere, follow the procedure for installing vSphere.

For details see *Downloading and Installing vSphere* on page 35-14.

Configuration Details

By default, VMware creates one virtual switch, vSwitch0, which is used to access the ESX(i) server over the corporate LAN. VMware applies the name VM Network to the network served by vSwitch0. In the IxVM Windows VM in this example, this network is labeled Corporate Network.



Step 1. Configure the Source and Destination Networks

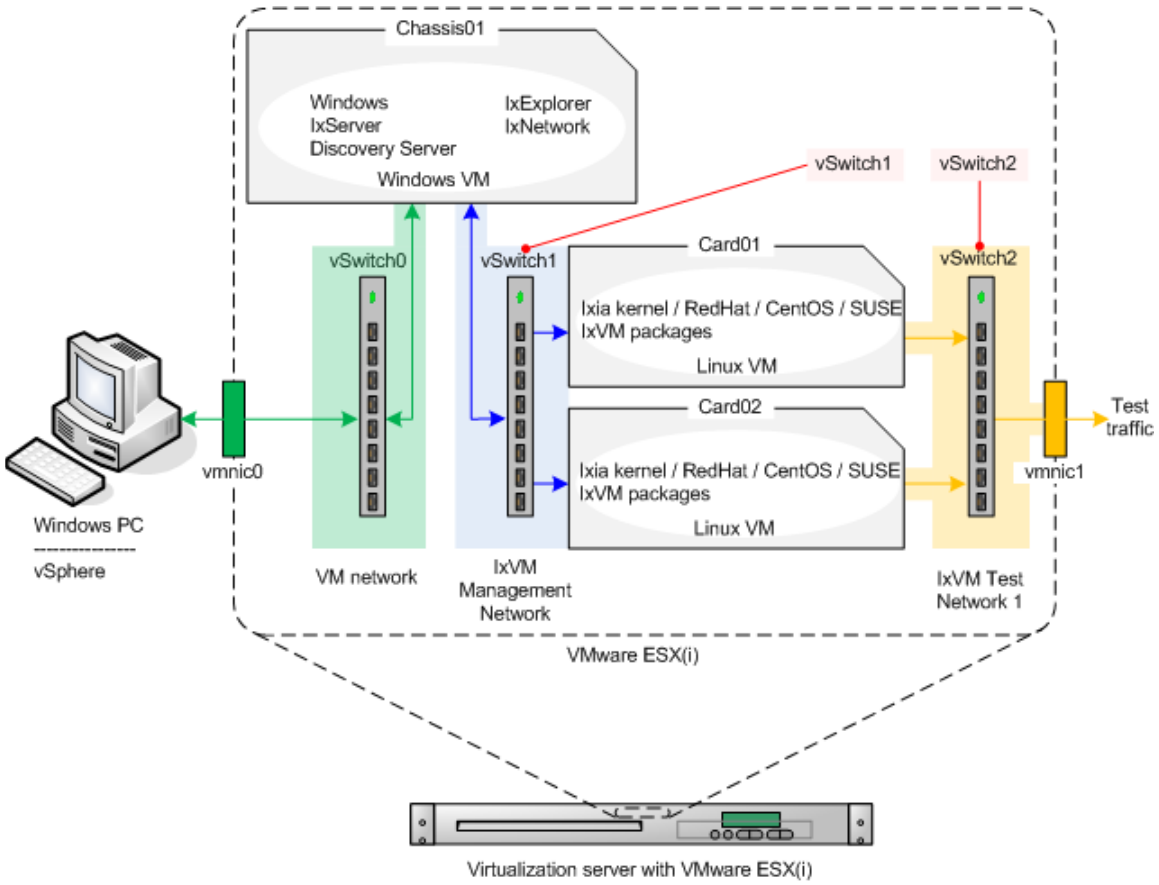
In vSphere, create two virtual switches (vSwitches): one to serve the network that carries the IxVM card management traffic, and one for the network that carries the test traffic. In vSphere, these are named source and destination networks.

For details see *Creating the Source and Destination Networks* on page 35-15.

Configuration Details

Name the networks as follows:

- vSwitch1: IxVM Management Network
- vSwitch2: IxVM Test Network 1



Step 3. Deploy a Windows VM

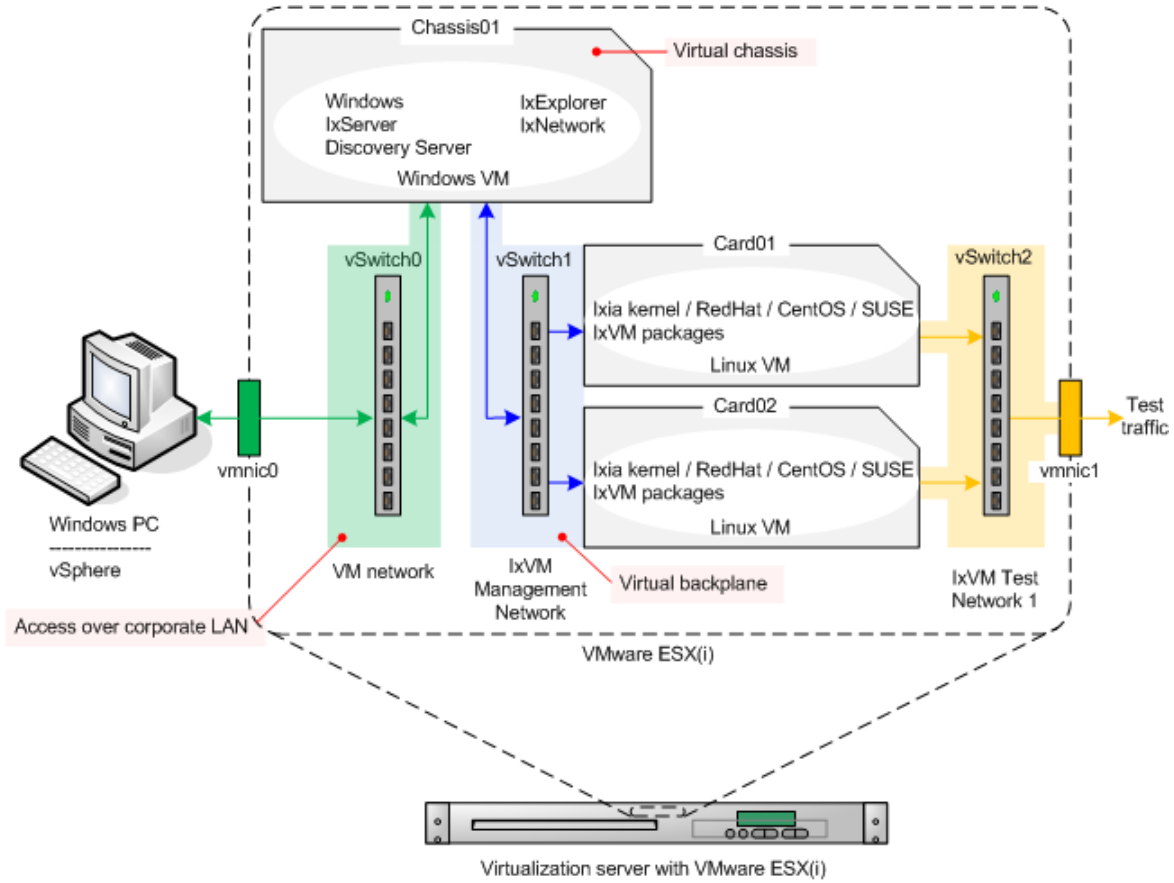
In vSphere, create a Windows VM with two NICs. Refer to the IxOS release notes for the list of Windows versions that IxVM supports.

Configuration Details

- Name the VM Chassis01.

- Create two networks, named and mapped as follows:

vSphere Network	Function
VM Network (default name)	Access to the virtual chassis from the corporate LAN
IxVM Management Network	IxVM card virtual backplane



Step 4. Deploy the Linux OVA Template

Deploy two Linux VMs based on the Ixia kernel OVA.

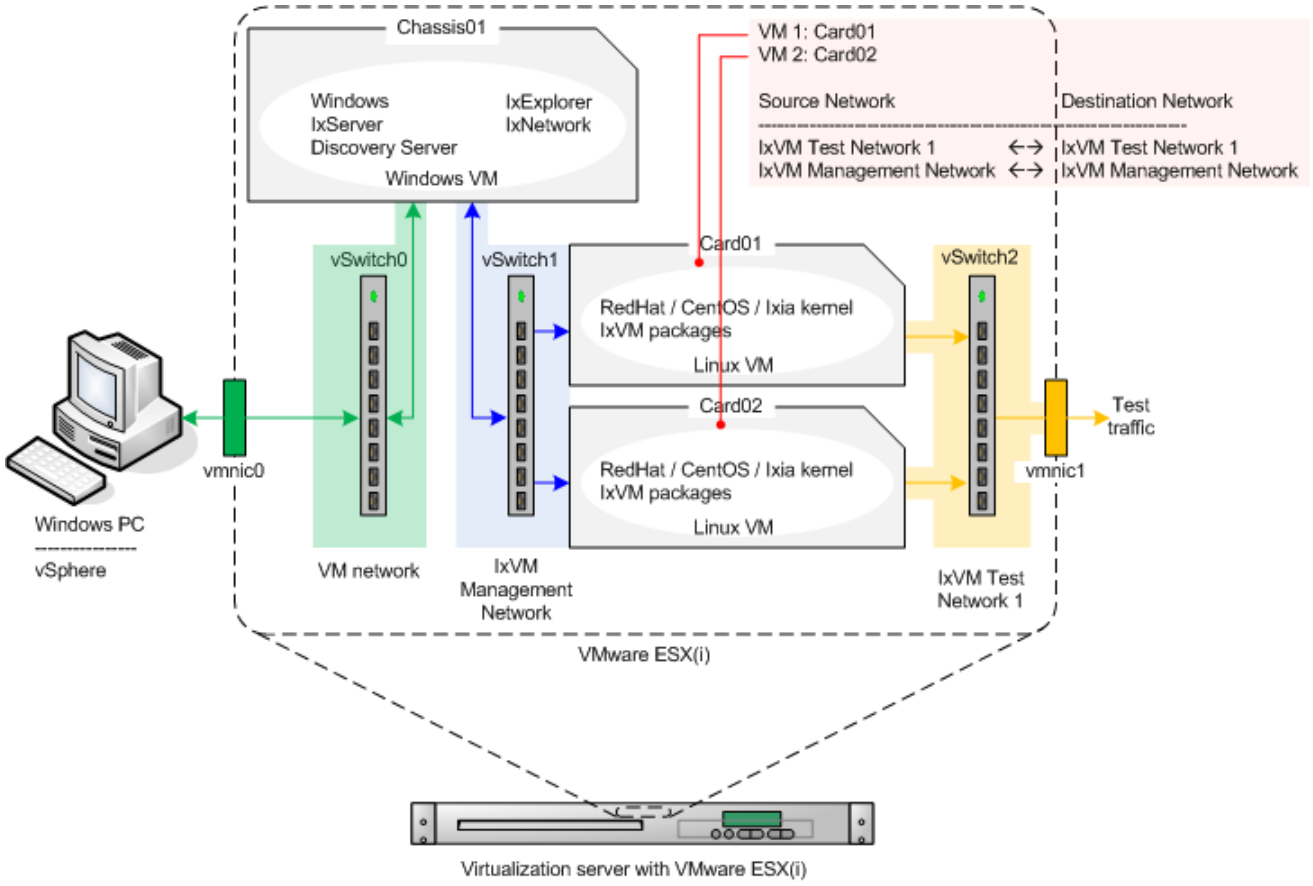
For details see *Deploying the IxVM Appliances (OVAs)* on page 35-16.

Configuration Details

- Name the first VM Card01
- Name the second VM Card02

- Map the networks as follows:

Source Network	Destination Network
IxVM Test Network 1	IxVM Test Network 1
IxVM Management Network	IxVM Management Network



Step 5. Configure the IxVM card (Linux OVA) Addresses

If you configured the IxVM cards (Card01, Card02, Linux OVAs) to use DHCP addressing, skip this step.

If you configured the IxVM cards to use static addressing, configure their addresses.

For details see *Configuring Static Addressing* on page 35-17.

Configuration Details

- Card01 addresses:

eth0: 10.0.0.1

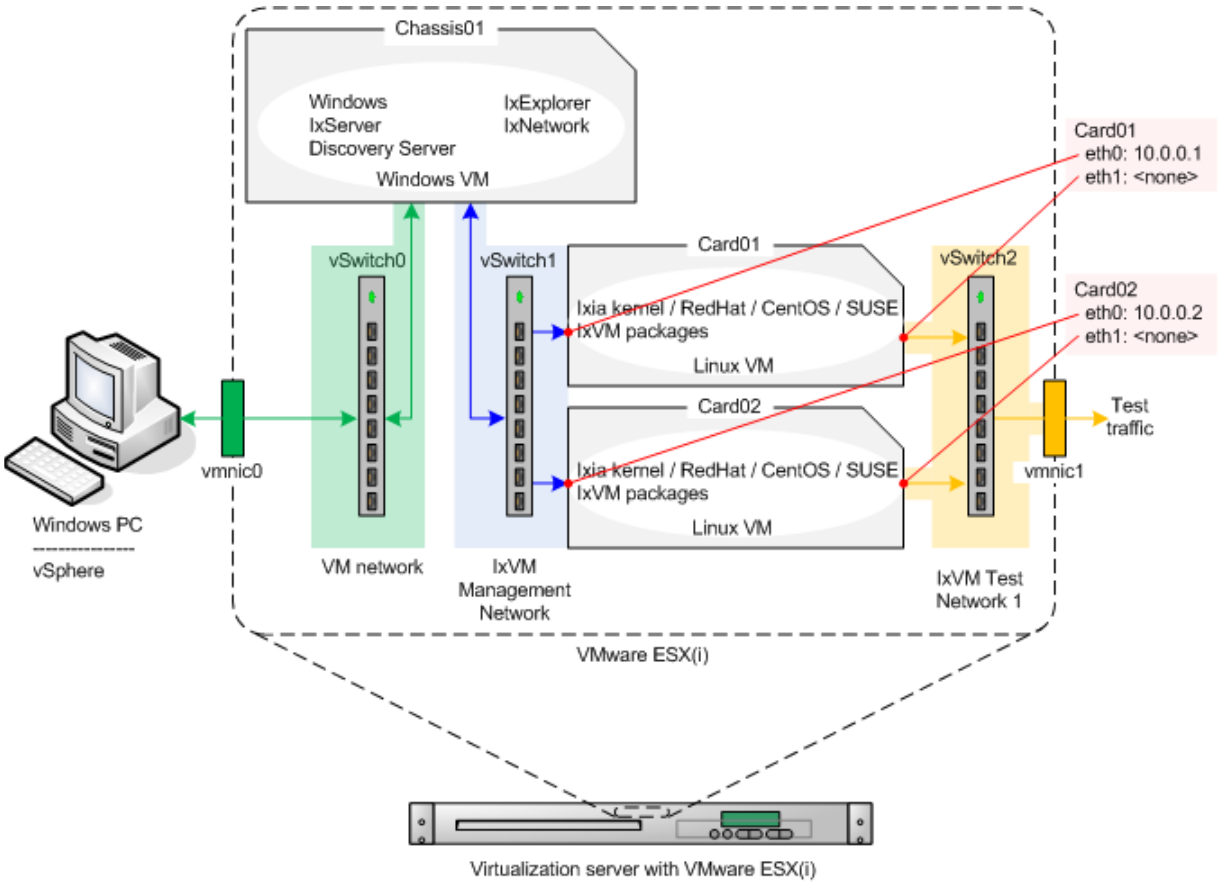
eth1: <no address>

- Card02 addresses:

  eth0: 10.0.0.2

  eth1: <no address>

Use the console to test connectivity by pinging card02 from card01 (or vice-versa).



Step 6. Configure the IxVM Chassis Addresses

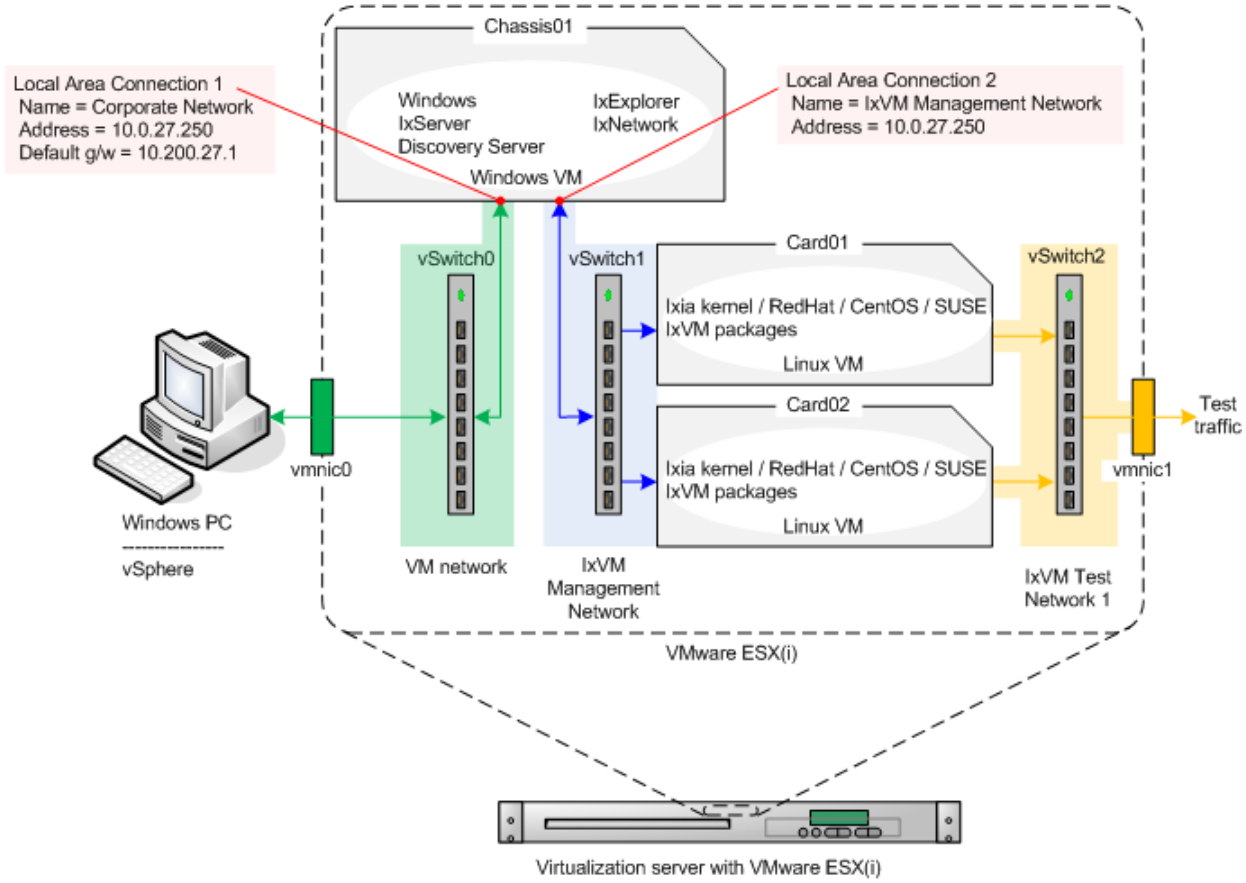
Configure the IxVM chassis controller (the Windows VM), and start IxVM and the supporting services on it.

1. Login to the Windows VM, and go through the procedure to license Windows.
2. Download and install the following components on the IxVM chassis controller.
   - IxVM Server
   - Discovery Server

3. Rename the two local area connections as follows:
   - Local Area Connection 1: VM network
   - Local Area Connection 2: IxVM Management Network
4. If you configured the IxVM chassis controller to use static addressing, configure its addresses as follows:

   VM network: 10.200.27.250/24 (Default gateway: 10.200.27.1)

   IxVM Management Network = 10.0.0.250/24 (Default gateway: none)



Step 7. Discover the IxVM Cards

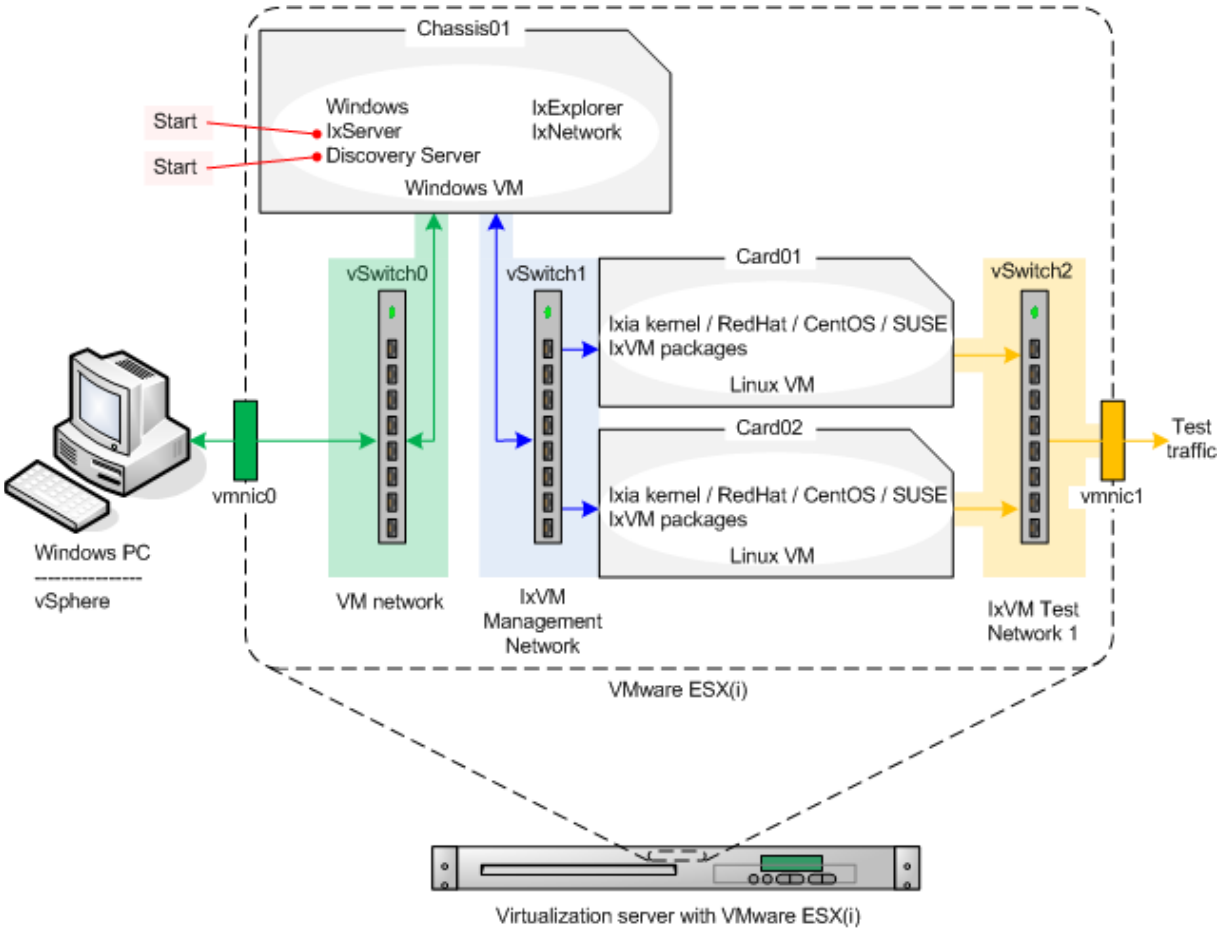
Start the Windows services, and discover the IxVM cards:

1. Start IxServer.
2. Start Discovery Server.
3. In Discovery Server, uncheck CORPORATE NETWORK (10.200.x.x, there are no VMs on this network).
4. Click SERVER | START BROADCAST to start Broadcast Discovery.

5. Click the AUTODISCOVERY tab. This tab should indicate that two end-points (the IxVM cards) have been discovered.
6. Close the Discovery Server window.

   The Discovery Server minimizes and continues to run.

   The IxVM cards are ready for use. Start IxExplorer, IxNetwork, or IxLoad and add them to your list of ports.



What to do Next

After you have installed IxVM, you can begin using it. There are two things you need to do to use IxVM with an Ixia testing application:

- Confirm that IxVM supports the protocols that you want to use.
- Find the IxVM virtual load modules running on your test network, and add them to your test configuration.

Supported Protocols

To confirm that IxVM supports the protocols you want to use in a test, check the list of supported protocols in the the test application's user guide.

Finding and Adding IxVM Load Modules

To find and add IxVM load modules, use the Discovery Server. Directions for using Discovery Server are included in the test application's user guide.

Using IxAdmin to Upgrade IxVM

You can use IxAdmin to inventory and upgrade software on IxVM virtual cards. IxAdmin communicates with Discovery Server to determine the assets that are in the network and then allows you to specify upgrade packages to be deployed to virtual test ports when new releases of IxVM become available.

To use IxAdmin to find and upgrade IxVM cards:

1. Start IxAdmin Console by clicking START | ALL PROGRAMS | IXIA | IXADMIN | IXADMIN CONSOLE.
2. In the toolbar, click DISCOVER APPLIANCES to start the discovery process.

   IxAdmin begins communicating with Discovery Server to identify all the virtual appliances in the system. When it finds them, it lists them in the popup window.

   Discovery Server needs to have discovered the IxVM cards (endpoints) in order to list them as candidates for upgrade. Alternatively, you can add the IxVM cards manually by clicking FILE | NEW | EQUIPMENT.
3. IxAdmin processes each virtual asset and then adds it to the inventory.
4. To display a list of the current software and revisions installed on an IxVM card, click on a Virtual Linux Machine, then click the INSTALLED SOFTWARE tab.
5. Click FILE | NEW | APPLICATION, and select the IxVM and IxNetwork packages (available in IxAdmin Packages folder on the Windows desktop).
6. Click INSTALL to install a new software package on a selected Linux VM.

   The Application Installation Wizard launches.
7. Click NEXT to accept the currently selected equipment.
8. Click ADD and then click INSTALL to select an Ixia Software package
9. Use the file browser to select the Ixia software package to be installed.
10. Click OK to begin the installation process.
11. To follow the installation process, click GO TO MONITOR VIEW.

Troubleshooting and Tips

Following are some of the troubleshooting tips:

- **IxNetwork fails to connect to Virtual Chassis (Retrying…)**

  Symptoms: IxServer is running and VM is IP reachable.

  Attempts to restart Hardware Manager still do not resolve the issue.

  Verify that the IP Address present in the file C:\Program Files\Ixia\IxOS\<IxOS_Version>\IxiaChassisIpEntry.txt matches the valid IP address of the interface used to communicate with the IxNetwork client.

- **IxVM RPM fails to install on Bare-Metal RHEL or CentOS machine**

  Symptoms: rpm –ivh command fails with error messages indicating that dependencies are missing.

  Before you install the IxVM RPMs, download and install the compat-libstdc++-33-* RPM that matches your version of Linux.

```
[root@Card01 ~]# rpm -ivh ixvm-5.50.508.86-rhel53_i686.rpm
error: Failed dependencies:
        compat-libstdc++-33 is needed by ixvm-5.50.508.86-1.0Beta5.i386
        libstdc++.so.5 is needed by ixvm-5.50.508.86-1.0Beta5.i386
        libstdc++.so.5(CXXABI_1.2) is needed by ixvm-5.50.508.86-1.0Beta5.i386
        libstdc++.so.5(GLIBCPP_3.2) is needed by ixvm-5.50.508.86-1.0Beta5.i386
[root@Card01 ~]#
```

- **Management network connectivity issues in a Bare-Metal Linux Installation**

  Try using the following settings:

Firewall Configuration -> Security Level, try using Disabled

Firewall Configuration -> SELinux, try using Disabled

- **Statistics De-synchronization and Clock Synchronization**

  Symptoms: Stats in the IxNetwork stat views are intermittently vanishing and re-appearing.

  VM-VM scenarios

  Ensure that all of your VMs are synchronized to the same NTP server, by calling "ntpq –p" on the linux console, and ensure that the server listed is the name/IP address of the system running IxServer VM.

  If your VMs which are connected to one instance of IxServer are not synchronized to the same time source, then you may have a third party application updating your local NTP time. See below as to how to customize your NTP Server configuration.

  In order to customize the NTP Server being used to synchronize each VM, you can specify the NTP Server used to synchronize all VMs connected to an instance of IxServer with the "NTPServerLocation" registry string, located in the "HKEY_LOCAL_MACHINE\Software\Ixia Communications\IxServer\Debug" registry key.

  Set to the IP Address of a valid NTP Server.

  Set to "0" to prevent IxVM from managing any synchronization with NTP (if you would like to manage it for each VM on your own).

In case you have multiple instances of IxServer VM managing all of your VMs, set the value on all machines running IxServer VM to the same IP address.

VM-HW scenarios

In order to synchronize IxVM cards between VMs and Ixia HW, the following steps are needed.

The NTPServerLocation registry key (see 10.1.2.2) needs to be set to an external NTP server based off of UTC time (see pool.ntp.org for more information) and the VMs need external internet connectivity to be able to communicate with those IP addresses.

The hardware-based ports need to be synchronized to use an AFD1 GPS server as their time source.

- **One Way Latency Measurement**

  Symptoms: User sees negative min/max/average latency in the IxNetwork traffic flow views, and IxExplorer's latency view.

  When running traffic between multiple different VM cards, IxVM is using software to synchronize the VM cards with each other, which does not give enough precision and leads to one VM card having a local time ahead of the other VM card. Inter Arrival time does not have this issue.

- **Cannot run Control Plane Traffic over MPLS**

  In IxNetwork, one of the the default settings for MPLS (LDP) is to run Control Plane traffic over MPLS. The RedHat/CentOS kernel does not support this; the Ixia kernel does.

Tips

- IxVM virtual ports cannot be attached to multiple IxVM Servers. You should disconnect the virtual port from one server, reboot the virtual port's host OS and reconnect to the port from the other server.
- Latency measurement in software is low-precision. You should expect to see typical accuracy of tens of milliseconds, and will occasionally see negative latency values.
- atency statistics are only available from one IxExplorer or TCL client per port. Two IxExplorer users (or an IxExplorer user and a TCL client session) cannot access latency stats simultaneously for the same virtual port.
- The IxVM Server must be on the same network as the virtual ports – no firewalls or NAT devices should be placed between the IxVM Server and virtual ports.
- Firewalls and SELinux policies should be disabled on the virtual port OS.

TclAPI Support

This section describes the IxOS TclAPI commands and statistics that you can use with an IxVM virtual load module.

In this section:

IxOS Tcl API Commands

You can use the following IxOS TclAPI commands with IxVM virtual load modules:

- `arp`
- `arpServer`
- `autoDetectInstrumentation`
- `byte2IpAddr`
- `card`
- `chassis`
- `chassisChain`
- `cleanUp`
- `clearAllMyOwnership`
- `dectohex`
- `errorMsg`
- `filter`
- `filterPallette`
- `hextodec`
- `host2addr`
- `ip`
- `ipAddressTable`
- `ixCheckLinkState`
- `ixCheckOwnership`
- `ixCheckTransmitDone`
- `ixClearArpTable`
- `ixClearOwnership`
- `ixClearPacketGroups`
- `ixClearPerStreamStats`

- ixClearPortPacketGroups
- ixClearScheduledTransmitTime
- ixClearStats
- ixClearTimeStamp
- ixCollectStats
- ixConnectToChassis
- ixConnectToTclServer
- ixDisconnectFromChassis
- ixDisconnectTclServer
- ixEnableArpResponse
- ixErrorInfo
- ixGetChassisID
- ixGlobalSetDefault
- ixInitialize
- ixLogin
- ixLogout
- ixPortClearOwnership
- ixPortTakeOwnership
- ixPuts
- ixRequestStats
- ixSetAdvancedStreamSchedulerMode
- ixSetPacketStreamMode
- ixSetPortPacketGroupMode
- ixSetPortPacketStreamMode
- ixSetScheduledTransmitTime
- ixSource
- ixStartPacketGroups
- ixStartPortPacketGroups
- ixStartPortTransmit
- ixStartTransmit
- ixStopPacketGroups
- ixStopPortPacketGroups
- ixStopPortTransmit
- ixStopTransmit
- ixTakeOwnership

- ixTransmitArpRequest
- ixWriteConfigToHardware
- ixWritePortsToHardware
- logMsg
- logOff
- logOn
- map
- mpexpr
- packetGroup
- port
- portGroup
- protocol
- showCmd
- stat
- stream
- streamTransmitStats
- tableUdf
- tableUdfColumn
- tcp
- udf (udf set 2/3 not supported)
- user
- version
- vlan

IxOS Statistics

You can use the following IxOS statistics IxVM virtual load modules:

Note: Some statistics may only work if the protocol or feature they measure is enabled. For example, bgpTotalSessions only returns a valid value if BGP is enabled. This is the same behavior as for physical load module.

- asynchronousFramesSent
- bfdAutoConfiguredSessionsUp
- bfdRoutersConfigured
- bfdRoutersRunning
- bfdSessionFlap

- bfdSessionsAutoConfigured
- bfdSessionsConfigured
- bfdSessionsUp
- bgpSessionFlap
- bgpTotalSessions
- bgpTotalSessionsEstablished
- bitsReceived
- bitsReceivedSStream
- bitsSent
- bitsSentSStream
- bytesReceived
- bytesReceivedSStream
- bytesSent
- bytesSentSStream
- captureFilter
- captureTemperature
- cfmBridgesConfigured
- cfmBridgesRunning
- cfmMasConfigured
- cfmMasRunning
- cfmMepsConfigured
- cfmMepsRunning
- cfmRemoteMepsLearned
- cfmSessionFlap
- cfmTrunksConfigured
- cfmTrunksRunning
- droppedFrames
- egressDroppedFrames
- eigrpNeighborDeleted
- eigrpNeighborsLearned
- eigrpRoutersConfigured
- eigrpRoutersRunning
- enableArpStats
- enableBfdStats
- enableBgpStats

- enableCfmStats
- enableEigrpStats
- enableIgmpStats
- enableIsisStats
- enableLdpStats
- enableMldStats
- enableMplsTpStats
- enableNeighborSolicitStats
- enableOamStats
- enableOspfStats
- enableOspfV3Stats
- enablePimsmStats
- enableProtocolServerStats
- enableRsvpStats
- enableStpStats
- framesReceived
- framesReceivedSStream
- framesSent
- framesSentSStream
- isisIpV4GroupRecordsLearned
- isisIpV6GroupRecordsLearned
- isisL1DBSize
- isisL2DBSize
- isisMacGroupRecordsLearned
- isisNeighborsL1
- isisNeighborsL2
- isisRBridgesLearned
- isisSessionFlapL1
- isisSessionFlapL2
- isisSessionsConfiguredL1
- isisSessionsConfiguredL2
- isisSessionsUpL1
- isisSessionsUpL2
- ldpBasicSessionsUp
- ldpSessionFlap

- ldpSessionsConfigured
- ldpSessionsUp
- link
- mode
- portCpuBytesReceived
- portCpuFramesReceived
- portCPUFramesSent
- portCpuStatus
- protocolServerRx
- protocolServerTx
- protocolServerVlanDroppedFrames
- rxArpReply
- rxArpRequest
- rxNeighborAdvertisements
- rxNeighborSolicits
- rxPingReply
- rxPingRequest
- scheduledFramesSent
- scheduledTransmitTime
- sequenceErrors
- sequenceFrames
- streamTrigger1
- streamTrigger2
- transmitDuration
- transmitState
- txArpReply
- txArpRequest
- txNeighborAdvertisements
- txNeighborSolicits
- txPingReply
- txPingRequest
- userDefinedStat1
- userDefinedStat2
- vlanTaggedFramesRx

A XAUI Connector Specifications

Description

The following cable and accessories for the 10GE XAUI cards are described in this appendix. These include the following:

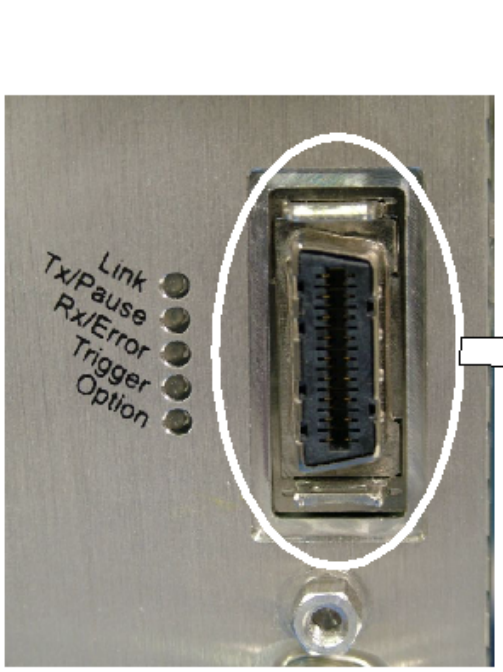
- *Standard Connector Specifications*: The signals carried on the Load Module's XAUI connector.
- *Front Panel Loopback Connector*: A connector used to loopback XAUI signals at the external connector.
- *Standard Cable Specification*: The CAB10GE500S1 (20") and CAB10GE500S2 (40") cables.
- *SMA Break-Out Box*: The BOB10GE500 SMA break-out box.
- *XAUI Fujitsu to XENPAK Adapter*: An adapter used with Ixia XENPAK load modules to create a XAUI interface.
- *XAUI Tyco Interoperability Backplane HM-Zd Adapter*: An adapter used to connect to the Tyco Interoperability Backplane.

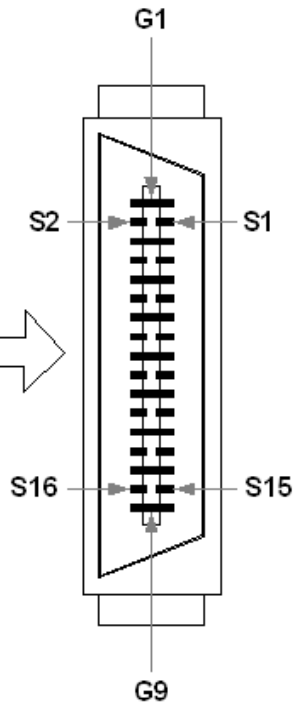
Standard Connector Specifications

The Ixia XAUI Load Module's front panel connector is the Fujitsu MicroGiGa. This connector can be mounted on the Device Under Test (DUT), eliminating the need for SMA cables. This part is also available directly from Fujitsu as part number FCN-268D008-G/1D-/2D.

The connector as mounted on the Ixia load module is shown in Figure A-1, along with the signal names, functional description, and connector pin assignments. The same pinouts apply to XENPAK load modules which use the XENPAK to XAUI adapter.

Figure A-1. Fujitsu MicroGiGa Connector Mounted on Load Module

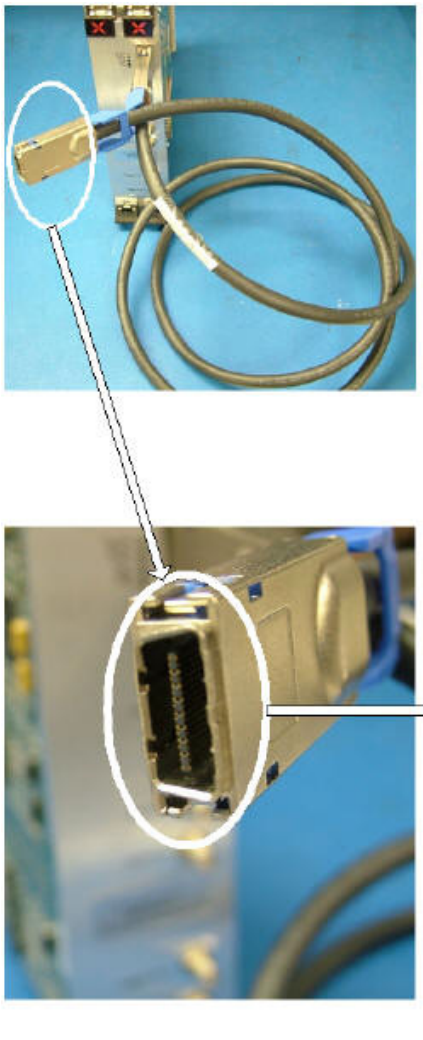




XAUI Pinout (XAUI LM or XENPAK with Adapter)		
PIN	SIGNAL	Direction
S1	TX3-	Out of Load Module
S2	TX3+	
S3	TX2-	
S4	TX2+	
S5	TX1-	
S6	TX1+	
S7	TX0-	
S8	TX0+	
S9	RX3-	Into Load Module
S10	RX3+	
S11	RX2-	
S12	RX2+	
S13	RX1-	
S14	RX1+	
S15	RX0-	
S16	RX0+	
G1-G9	GND	N/A

The XAUI Cable plugs into the load module and transposes the transmit and receive signals, as shown in the following figure.

Figure A-2. XAUI Cable Pinouts

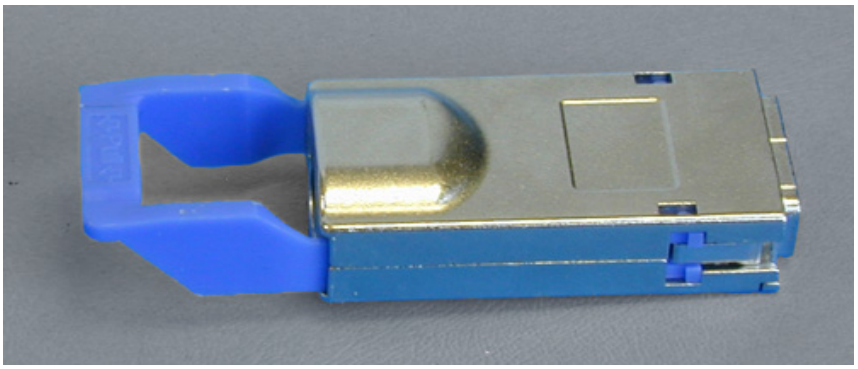


XAUI Cable Pinout (830-0072-XX) (Plugged into Load Module - Transposes TX and RX signals)		
PIN	SIGNAL	Direction
S1	RX3-	Into Cable End
S2	RX3+	
S3	RX2-	
S4	RX2+	
S5	RX1-	
S6	RX1+	
S7	RX0-	
S8	RX0+	
S9	TX3-	Out of Cable End
S10	TX3+	
S11	TX2-	
S12	TX2+	
S13	TX1-	
S14	TX1+	
S15	TX0-	
S16	TX0+	
G1-G9	GND	N/A

Front Panel Loopback Connector

In order to verify that the Ixia XAUI Load Module is operational, a loopback connector may be used to test external loopback on the front panel. You can remove the connector by pulling back on the blue handle, releasing the connection to the Fujitsu MicroGiGa connector. The loopback connector (Ixia P/N LPG10GE500) is shown in the following figure.

Figure A-3. XAUI Front Panel Loopback Connector



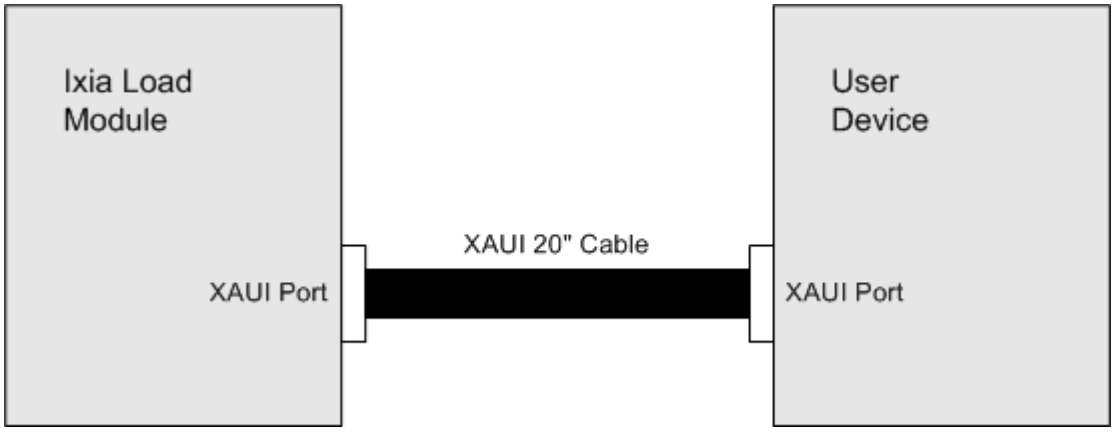
Standard Cable Specification

The same connector and pin assignments used on the Load Module can also be used on the Device Under Test (DUT). Ixia supplies a 20-inch cross-pinned cable assembly (CAB10GE500S1) that allows a straight connection as shown in Figure A-5. This cable can also be used for loopback testing on an Ixia chassis equipped with two or more XAUI ports. Longer cable assemblies can be made on request, but we do not recommend that the cable length exceed 2 meters, because losses and skew may become unacceptable. Ixia makes a 40” cable available as part number CAB10GE500S2. The 40” cable is shown in Figure A-4.

Figure A-4. Ixia XAUI Cable (CAB10GE500S2)

Note: The 50cm maximum length suggested in the XAUI section of 802.3ae is a rough guideline for keeping the losses on PCB traces under 7.5 dB. Well designed cables usually have much lower losses per meter than PCB traces, so cables can be much longer than 50cm.

Figure A-5. Direct XAUI Interface Using Ixia Supplied Cable



SMA Break-Out Box

If the DUT uses coaxial connectors for the XAUI interface, a special break-out box (BOB10GE500) is required in addition to the XAUI cable, as shown in Figure A-6. You must provide the sixteen 50 ohm coaxial cables with a male SMA connector on the end that mates to the BOB. The actual break-out box is shown in Figure A-6.

Figure A-6. XAUI SMA Break-Out Box

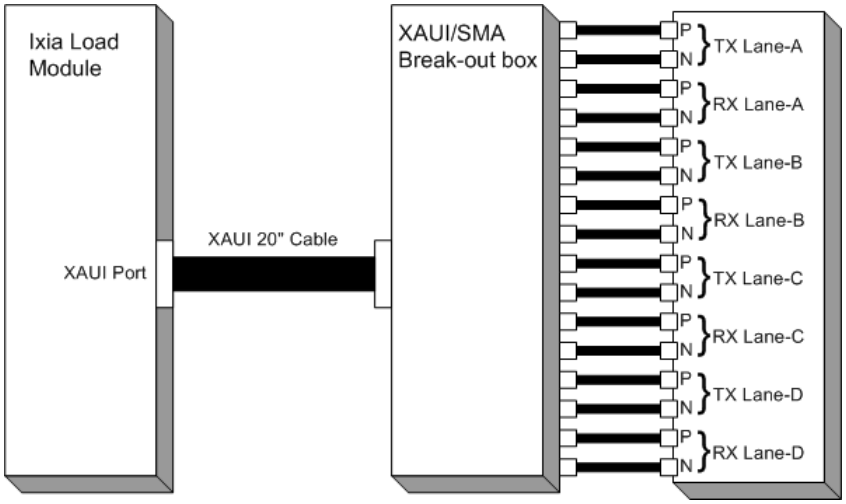


Figure A-7. XAUI SMA Break-Out Box

When using coaxial cables for the XAUI interface, extreme care should be taken to match the electrical lengths of the two cables in each pair. The pairs can be of different lengths, since the XAUI SerDes should automatically correct for skew between lanes. Skew between the ‘P’ and ‘N’ lines within a pair, however, can introduce bit errors. The XAUI edge-rates can be as short as 60ps. Therefore, the total in-pair skew should be kept below 30 ps to avoid bit-errors. Some of this in-pair skew must be budgeted to the Load Module, Ixia XAUI cable, BOB, and the DUT. Allocating 10ps of in-pair skew to the coax cables would require length

matching them to within about 0.08” (for RG-174). The propagation velocity of coax can vary slightly between manufacturers, lots, and as it is bent or stretched. Therefore, we recommend that coax cables be kept as short as possible.

Table A-1. XAUI Electrical Interface Performance

Parameter		Characteristic
Tx Outputs	Impedance	100 ohm balanced differential, AC coupled.
	Amplitude	1.2Vpp minimum (with 0 pre-emphasis)
	Pre-emphasis	Software selectable (0, 18%, 38% or 75%)
	Jitter	0.35 UI max. (UI is Unit Interval = 320ps nominal).
Rx Inputs	Impedance	100 ohm differential, AC coupled.
	Amplitude	0.2 to 2.3 Vpp.
	Jitter tolerance	0.55 UI.

XAUI Fujitsu to XENPAK Adapter

The electrical interface to XENPAK is XAUI, which uses an industry standard 70-pin connector. Ixia’s XAUI Load Module, however, uses a Fujitsu MicroGiGa connector to both transmit and receive four XAUI lanes through eight twisted pairs through a 20” cable. Ixia offers an adapter (part number FXN10GE500) that routes the XAUI lanes from the Fujitsu connector to the pins on the XENPAK connector.

This enables a XENPAK Load Module to act as a XAUI Load Module. However, the XENPAK Load Module can only run in Ethernet mode and transmit and verify Layer 2 or 3 traffic. Furthermore, there is an FD D-sub connector for MDIO on the front panel of the XENPAK Load Module (shown in Figure A-9 on page A-9). Both the MDIO and power are available through pins on the adapter and serve the same function as the D-sub connector on the XAUI Load Module.

The adapter is shown in Figure A-8.

Figure A-8. Fujitsu to XENPAK Adapter

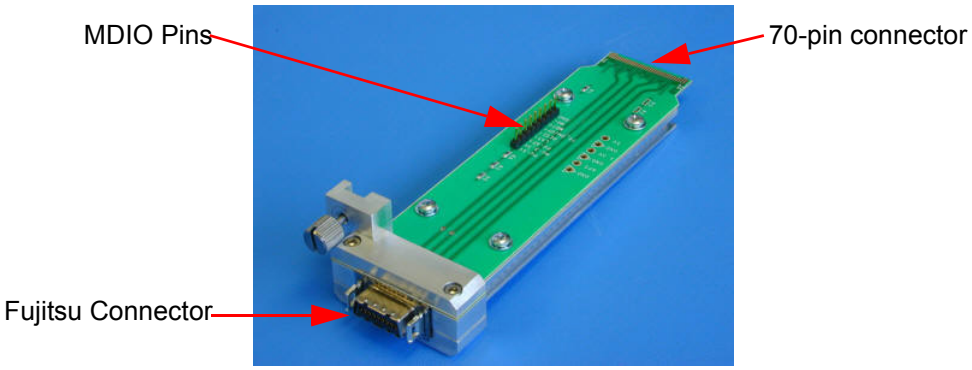
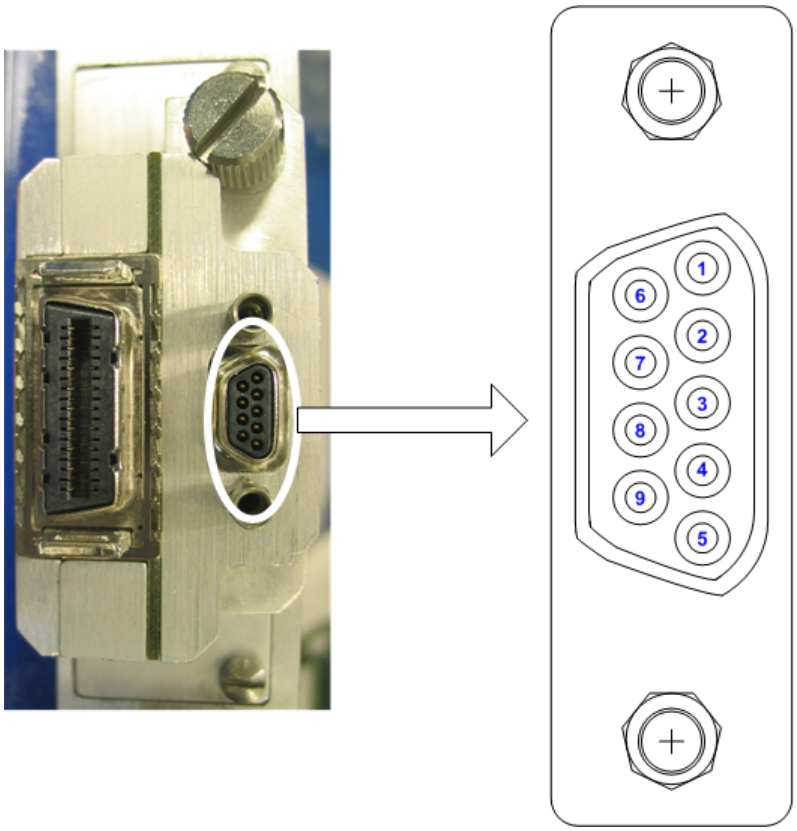


Figure A-9. CX4 and XAUI MDIO Pinouts

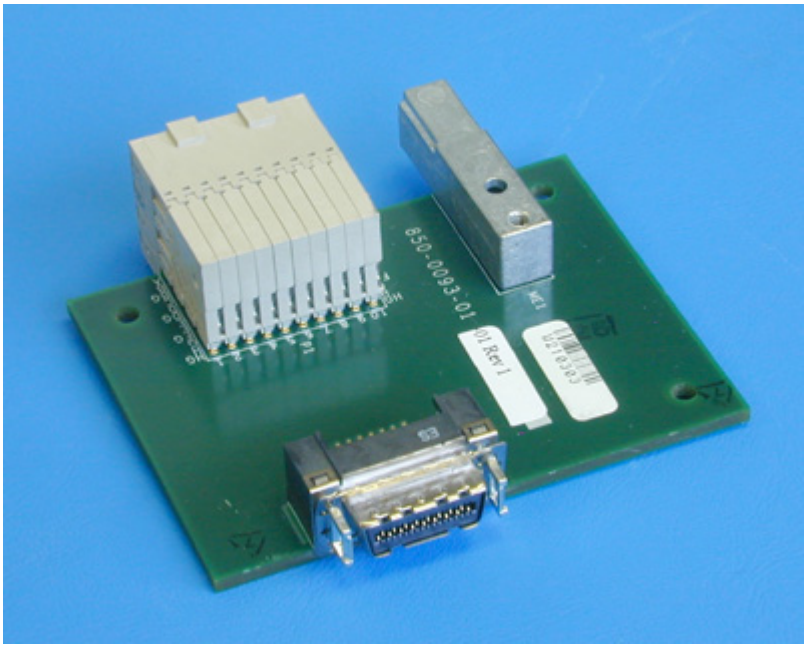


Front Panel MDIO Pinout		
PIN	SIGNAL	Direction
1	5V	OUT
2	3.3V	OUT
3	APS	OUT
4	LASI	OUT
5	RESET	OUT
6	TX_ON	OUT
7	MDIO	OUT
8	MDC	OUT
9	GND	OUT

XAUI Tyco Interoperability Backplane HM-Zd Adapter

XAUI interoperability testing has been conducted using a Tyco built simulated backplane. Each XAUI vendor has been required to build a line card to connect to the backplane through the Tyco HM-Zd connector. Tyco had also built an SMA adapter to connect to the backplane, but it is too time-consuming and difficult to connect through SMAs. Ixia has built an HM-Zd adapter (P/N FTY10GE500), which allows direct connection to the backplane through the Fujitsu connector, saving significant setup time. This is shown in Figure A-10.

Figure A-10. Tyco Interoperability Backplane HM-Zd Adapter



B Available Statistics

This appendix covers the available statistics for the following different card types:

- *Statistics for 10/100 Cards*. These cards include the following:
  - 10/100 TX (LM100TX)
  - 10/100 TX3 (LM100TX3)
  - 10/100 MII (LM100MII)
  - 10/100 Reduced MII
  - 100 Base FX MultiMode (LM100FX)
  - 100 Base FX SingleMode (LM100FXSM)
  - Copper 10/100/1000 running at 10/100 Mbps (LM1000T-5)
- *Statistics for 10/100 TXS Modules*. These cards include the following:
  - 10/100 TX8 (LM100TX8)
  - 10/100 TXS8 (LM100TXS8)
- *Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards*. These cards include the following:
  - 10/100/1000 TX4 (LM1000TX4)
  - 10/100/1000 TXS4 (LM1000TXS4)
  - 10/100/1000 STX2, STX4, STX24 (LM1000STX2/4, OLM1000STX24)
  - 10/100/1000 STXS2, STXS4, STXS24 (LM1000STXS2/4, OLM1000STXS24)
  - 10/100/1000 XMS12, XMSR12 (LSM1000XMS12, LSM1000XMSR12)
  - 1000 SFP4 (LM1000SFP4)
  - 1000 SFPS4 (LM1000SFPS4)
- *Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards*. These cards include the following:

- 10/100/1000 XMV4/8/12/16, XMVR4/8/12/16 (LSM1000XMV4/8/12/16, LSM1000XMVR4/8/12/16)
- 10/100/1000 ASM XMV12X

- *Statistics for Gigabit Modules*. These cards include the following:
  - 1000 Base SX MultiMode (LM1000SX)
  - 1000 Base SX SingleMode (LM1000SX3)
  - GBIC (LM1000GBIC)
- *Statistics for OC12c/OC3c Modules*. These cards include the following:
  - OC12c/OC3c (LMOC12c, LMOC3c)
- *Statistics for OC48c Modules with BERT*, *Statistics for OC48c Modules with SRP and DCC*, and *Statistics for OC48c Modules with RPR and DCC*. These cards include the following:
  - OC48c POS (LMOC48cPOS, LMOC48cPOS-M)
  - OC48 POS VAR (LMOC48VAR)
  - OC48c BERT (LMOC48cBERT)
  - OC48c BERT Rx
  - OC48c POS/BERT (LMOC49POS/BERT)
- *Statistics for 2.5G MSM POS modules*. These cards include the following:
  - 2.5 Gigabit MSM POS OC-48c modules (MSM2.5G1-01)
- *Statistics for OC192c Modules with BERT*, *Statistics for OC192c Modules with SRP and DCC*, and *Statistics for OC192c Modules with RPR and DCC*. These cards include the following:
  - OC192c with optional BERT and 10 Gigabit Ethernet. (LMOC192cPOS+BERT, LMOC192cPOS+BERT+WAN)
  - OC192c VSR. Note that all VSR cards have available all of the VSR statistics listed in the **VSR** section of **Table B-6** on page B-25. (LMOC192cVSR-POS, LMOC192cVSR-BERT, LMOC192cVSR-POS+BERT)
- *Statistics for 10GE Modules with BERT*. These cards include the following:
  - 10 Gigabit Ethernet with optional BERT. (LM10GELAN, LM10GELAN-M, LM10GEWAN, LM10GEXAUI+BERT, LM10GEXAUI BERT only, LM10GEXENPAK+BERT, LM10GEXENPAK-M+BERT, LM10GEXENPAK BERT only)
- *Statistics for 10G UNIPHY Modules with BERT*. These cards include the following:
  - 10 Gigabit UNIPHY with optional LAN/WAN, POS and BERT. (LM10G)
- *Statistics for 10GE LSM Modules (except NGY)*. These cards include the following:
  - 10 Gigabit LSM modules using XFP, XENPAK, or X2 carrier cards. (LSM10GL1-01, LSM10G1-01)

- 10 Gigabit LSM modules supporting MACSec. (LSM10GMS-01) See also Table B-32 on page B-160 for MACSec statistics.
- 10 Gigabit LSM XL6 modules (for Optixia X16). (LSM10GXL6-01)
- 10 Gigabit LSM XM3, XMR3 (LSM10GXM3, LSM10GXMR3)
- NGY LSM10GXM(R)8(XP)(S)-01, LSM10GXM(R)4(XP)(S)-01, LSM10GXM2XP-01, LSM10GXMR2(S)-01, LSM10GXM2S-01, including 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01

- *Statistics for NGY Modules*. These cards include the following:
  - NGY LSM10GXM(R)8(XP)(S)-01, LSM10GXM(R)4(XP)(S)-01, LSM10GXM2XP-01, LSM10GXMR2(S)-01, LSM10GXM2S-01, including 10GBASE-T versions LSM10GXM(R)2/4/8GBT-01
- *Statistics for 10G MSM modules*. These cards include the following:
  - 10 Gigabit Ethernet MSM modules. (MSM10G1)
- *Statistics for ATM Modules*. These include the following:
  - ATM 622 Multi-Rate (LM622MR, LM622MR-512)
- *Statistics for PoE Modules*. These include the following:
  - Power over Ethernet (PLM1000T4-PD, LSM1000POE4-02)
- *Statistics for 10/100/1000 AFM*. These include the following:
  - 10/100/1000 AFM Stream Extraction Module. (AFM1000SP-01)
- *Statistics for IxNetwork*. These statistics are common to all cards that support IxNetwork.
- *Statistics for 1GbE and 10GbE Aggregation Load Modules*. These include the following:
  - ASM1000XMV12X-01 (in 1GbE Aggregated Mode or 10GbE Aggregated Mode)
- *ALM, ELM and CPM Statistics*. These include the following:
  - ALM1000T8, ELM1000ST2, and CPM1000T8-01 load modules
- *40/100 GE Statistics*. These include the following:
  - 40GE LSM XMV1 and 100GE LSM XMV1 load modules
  - Lava 40/100GE load modules

Table Organization

Each of the following tables details the statistics available for that set of cards. Available statistics are controlled by three sets of controls.

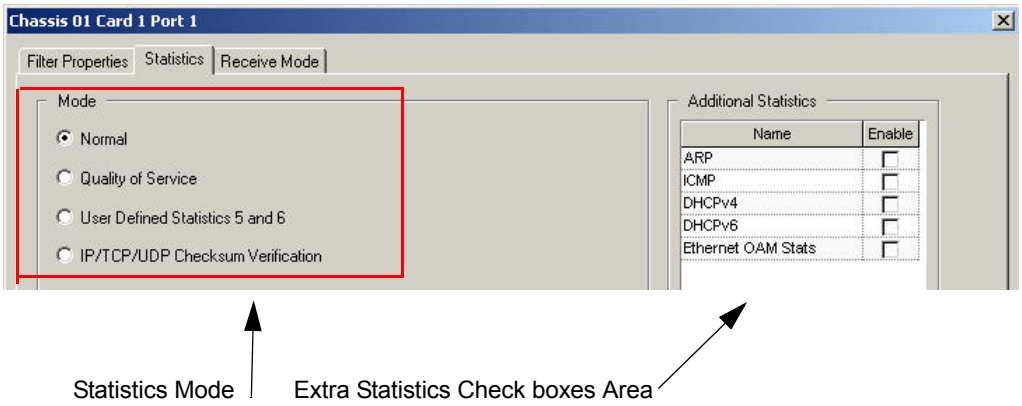
IxExplorer

Statistics Modes

From the IxExplorer pane, select a port and select **Filter, Statistics, Receive Mode** from the right-hand pane. Select the tab at the top labelled **Statistics**. This

is shown here for a Gigabit module with the statistics modes highlighted. The choices here are mutually exclusive. In most cases, when one is selected new statistics are available at the expense of others.

Figure B-1. Statistics Mode Selection



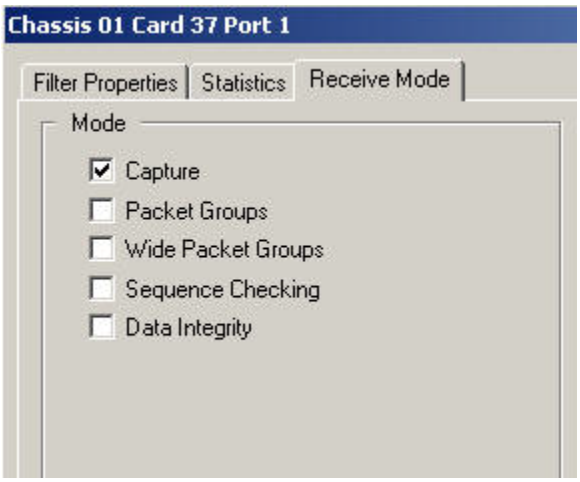
Extra Statistics Check Boxes

Additional statistics are selected through a set of check boxes located on the same **Statistics** tab, in the **Additional Statistics** section. These statistics are always in addition to those in the **Statistics Mode** section.

Receive Mode

From the IxExplorer pane, select a port and select **Filter, Statistics, Receive Mode** from the right-hand pane. Select the tab at the top labelled **Receive Mode**. This is shown here for a 10GE LAN module. The check boxes generally result in additional statistics.

Figure B-2. Receive Mode Selection



Key to Tables

Table B-1 lists the headings that appear in the tables in this appendix and their correspondence to IxExplorer dialogs and selections.

Table B-1. Key for Statistics Table

Heading Item	IxExplorer Dialog	IxExplorer Label
Statistics Mode		
UDS 5&6	Statistics	User Defined Statistics 5 and 6
QoS	Statistics	Quality of Service
Normal	Statistics	Normal
Checksum Errors	Statistics	IP/TCP/UDP Checksum Verification
Data Integrity	Statistics	Data Integrity
Extra Statistics Check boxes		
IxRouter	Statistics	IxRouter Stats
ARP STATS	Statistics	ARP Stats
ICMP STATS	Statistics	ICMP Stats
BGP STATS	Statistics	BGP Stats
OSPF STATS	Statistics	OSPF Stats
ISIS STATS	Statistics	ISIS Stats
RSVP-TE STATS	Statistics	RSVP-TE Stats
LDP STATS	Statistics	LDP Stats
POS Ext	Statistics	POS Extended Stats
DHCPv4	Statistics	DHCPv4 Stats
DHCPv6	Statistics	DHCPv6 Stats
Temp Sensors	Statistics	Temperature Sensor Stats
OAM Stats	Statistics	Ethernet OAM Stats
PTP Stats	Statistics	Ptp Stats
Receive Mode		
Rx Capture	Receive Mode	Capture
Rx Seq Checking	Receive Mode	Sequence Checking
Rx Data Integrity	Receive Mode	Data Integrity
Rx Packet Group	Receive Mode	Packet Group

Table B-1. Key for Statistics Table

Heading Item	IxExplorer Dialog	IxExplorer Label
Rx Mode Bert	Receive Mode	Mode Bert
Rx Mode ISL	Receive Mode	Mode ISL
Rx Bert Channelized	Receive Mode	Bert Channelized
Rx Mode Echo	Receive Mode	Mode Echo
Rx Mode DCC	Receive Mode	Mode DCC
Rx Wide Packet Group	Receive Mode	Wide Packet Groups
Rx Mode PRBS	Receive Mode	PRBS
Rx Rate Monitoring	Receive Mode	Rate Monitoring
Rx Per Flow Error Stats	Receive Mode	Per PGID Checksum Error Stats

Statistics Mode

The statistics mode is controlled by the use of the Tcl `stat mode` command. Table B-2 lists the available choices and their correspondence to IxExplorer choice .

Table B-2. Tcl Stat Mode Options

Option	IxExplorer Choice
statNormal (0) (default)	Normal
statQos (1)	Quality of Service
statStreamTrigger (2)	User Defined Statistics 5 and 6
statModeChecksumErrors (3)	IP/TC@/UDP Checksum Verification
statModeDataIntegrity (4)	Data Integrity

Access to Statistics

Most statistics are accessed through the use of `stat` command. VSR statistics are access through the use of the `vsrStat` command.

Receive Mode

The receive mode is controlled through the use of the `port receiveMode` option. The choices available are or'd together and list the bits available to control the receive mode.

Table B-3. Tcl Port Receive Options

Option	IxExplorer Choice
portCapture (1)	Capture
portPacketGroup (2)	Packet Groups
portRxTcpSessions (4)	Does not affect statistics.
portRxTcpRoundTrip (8)	Does not affect statistics.
portRxDataIntegrity (16)	Data Integrity
portRxFirstTimeStamp (32)	Does not affect statistics.
portRxSequenceChecking (64)	Sequence Checking
portRxModeBert (128)	BERT Mode
portRxModeBertChannelized (128)	Channelized BERT Mode
portRxModeIsl	ISL Mode
portRxModeEcho	Echo Mode
portRxModeDcc	DCC Mode
portRxModeWidePacketGroup	Wide Packet Groups
portRxModePrbs	PRBS Mode
portRxModeRateMonitoring	Rate Monitoring
portRxModePerFlowErrorStats	Per PGID Checksum Error Stats

C++ Development

Statistics Mode

The statistics mode is controlled by the use of the `stat.mode` member. Table B-1 on page B-4 lists the available choices and their correspondence to IxExplorer choices and the labels used in the tables in this appendix.

Table B-4. C++ Stat Members

Member Value	IxExplorer Choice
statNormal (0) (default)	Normal
statQos (1)	Quality of Service
statStreamTrigger (2)	User Defined Statistics 5 and 6
statModeChecksumErrors (3)	IP/TCP/UDP Checksum Verification
statModeDataIntegrity (4)	Data Integrity

Access to Statistics

Most statistics are accessed through the use of `TCLStatistics` class. VSR statistics are accessed through the use of the `TCLvsrStat` class.

Receive Mode

The receive mode is controlled through the use of the `port.receiveMode` member. The choices available are or'd together and list the bits available to control the receive mode.

Table B-5. Tcl Port Receive Options

Member Value	IxExplorer Choice
portCapture (1)	Capture
portPacketGroup (2)	Packet Groups
portRxTcpSessions (4)	Does not affect statistics.
portRxTcpRoundTrip (8)	Does not affect statistics.
portRxDataIntegrity (16)	Data Integrity
portRxFirstTimeStamp (32)	Does not affect statistics.
portRxSequenceChecking (64)	Sequence Checking
portRxModeBert (128)	BERT Mode
portRxModeBertChannelized (128)	Channelized BERT Mode
portRxModeIsl	ISL Mode
portRxModeEcho	Echo Mode
portRxModeDcc	DCC Mode
portRxModeWidePacketGroup	Wide Packet Groups
portRxModePrbs	PRBS Mode
portRxModeRateMonitoring	Rate Monitoring
portRxModePerFlowErrorStats	Per PGID Checksum Error Stats

Description of Statistics

Table B-6 lists all of the available statistics, along with an explanation of those statistics.The following three columns are used:

- Counter: the name of the statistics as it appears in IxExplorer. These are organized by general category, as used in the remaining tables in this appendix.
- Interpretation: the description of the statistics.
- Internal Baseame: the internal *basename* used to describe the statistics in the TCL and C++ API. The base name is used to form other names:
  - TCL *stat* command options: the *basename* is the name of the option.
  - TCL *stat* command `get` sub-command *counterType* argument : the *counterType* name needed to fetch a particular statistic is formed by prepending the letters *stat* to the *basename*, while capitalizing the first letter of the statistic. For example, for *basename* alignmentErrors, the *counterType* name is *statAlignmentErrors*.
  - C++ *statistic* class members: the *basename* is the name of the member.
  - C++ *statistic* command *get* method *counterType* argument: the *counterType* name needed to fetch a particular statistic is formed by prepending the letters *stat* to the *basename*, while capitalizing the first letter of the statistic. For example, for *basename* alignmentErrors, the *counterType* name is *statAlignmentErrors*.

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Optixia X16 Chassis		
Opix Power Supply 1 Status	The status of the #1 (left most) power supply.	Not available.
Opix Power Supply 2 Status	The status of the #2 power supply.	Not available.
Opix Power Supply 3 Status	The status of the #3 power supply.	Not available.
Opix Power Supply 4 Status	The status of the #4 power supply.	Not available.
Opix Power Supply 1 Current	The current of the #1 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Power Supply 2 Current	The current of the #2 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Power Supply 3 Current	The current of the #3 power supply. This should be within 3 amps of other installed power supplies.	Not available.

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Opix Power Supply 4 Current	The current of the #4 power supply. This should be within 3 amps of other installed power supplies.	Not available.
Opix Fan Bank 1 Status	The status of the #1 bank of fans, located in the fan tray.	Not available.
Opix Fan Bank 2 Status	The status of the #2 bank of fans, located in the fan tray.	Not available.
Opix Fan Bank 3 Status	The status of the #3 bank of fans, located in the fan tray.	Not available.
Opix Fan Bank 4 Status	The status of the #4 bank of fans, located in the fan tray.	Not available.
Optixia X16 Load Modules	A variable number of the statistics in this category are available for OLM load modules.	
5V Power Status	Indicates that the 5VDC bus A rail is on and valid.	Not available.
3.3V Power Status	Indicates that the 3.3VDC bus A rail is on and valid.	Not available.
3.3V/5V Power Status	Indicates that either the bus A 5VDC or 3.3VDC rail had an overcurrent event and shut down.	Not available.
LM Other Power Output	Indicates that power is good for the miscellaneous power supplies.	Not available.
LM 48V Power Output	Indicates that the -48VDC input is on.	Not available.
LM Temperature 1 Status	LM 83 programmable interrupt - over temperature alarm.	Not available.
LM Temperature 2 Status	LM 83 critical temperature alarm.	Not available.
LM Bus B 5V Power Status	Indicates that the 5VDC bus B rail is on and valid.	Not available.
LM Bus B 3.3V Power Status	Indicates that the 3.3VDC bus B rail is on and valid.	Not available.
LM Bus B 3.3V/5V Power Status	Indicates that either the bus B 5VDC or 3.3VDC rail had an overcurrent event and shut down.	Not available.
LM Temperature Central FPGA	Nominal board temperature in area 3.	Not available.
LM Temperature LM83	Nominal board temperature in area 1.	Not available.
LM Temperature LM87	Nominal board temperature in area 2.	Not available.

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
LM -48VDC Status	Indicates that the -48VDC input is in the valid input range.	Not available.
LM System V1	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM SMBUS 3.3V	Measures the SM bus. This value should be 3.3VDC =/- 10%.	Not available.
LM System V2	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM System V3	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM System V4	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM System V5	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM System V6	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
LM System V7	Dependent on each Optixia Load Module. Monitors one of several system buses.	Not available.
User Configurable		
User Defined Stats 1 and 2 & Rate	Counters that increment each time the statistics conditions are met. The user-defined statistics conditions are set up in the Capture Filter window.	userDefinedStat1 userDefinedStat2
Capture Trigger (UDS3) & Rate	A counter that increments each time the capture trigger conditions are met, as defined in the Capture Filter window.	captureTrigger
Capture Filter (UDS4) & Rate	A counter that increments each time the capture filter conditions are met, as defined in the Capture Filter window.	captureFilter
User Defined Stats 5 and 6 & Rate	Counters that increment each time the statistics conditions are met. The user-defined statistics conditions are set up in the Capture Filter window. (N/A to OC192 modules.)	streamTrigger1 streamTrigger2
States		
Link State	'Up' when a link is established with another device, 'Loopback' when the port has loopback enabled, 'Down' when there is no connection to another device. (See note 2 in *Notes*.)	link

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Line Speed	'10,' '100,' or '1000' (denoting Mbps) and OC-12, OC-3 or OC-48 for POS modules. (See note 6 in *Notes.*)	lineSpeed
Duplex Mode	'Half' or 'Full.' Half duplex only applies to 10/100 Load Modules. (See note 7 in *Notes.*)	duplexMode
Transmit State	Not shown in IxExplorer. The current transmit state of the port. See the *stat* command in the *Tcl Development Guide* and *C++ Development Guide.*	transmitState
Capture State	Not shown in IxExplorer. The current capture state of the port. See the *stat* command in the *Tcl Development Guide* and *C++ Development Guide.*	captureState
Pause State	Not shown in IxExplorer. The current pause state of the port. See the *stat* command in the *Tcl Development Guide* and *C++ Development Guide.*	pauseState
Common		
Frames Sent & Rate	A counter that increments only when a frame is successfully transmitted. This counter does not count collision attempts.	framesSent
Valid Frames Received & Rate	The valid frame size is from 64 bytes to 1518 bytes inclusive of FCS, exclusive of preamble and SFD and must be an integer number of octets. This 32 bit counter only counts frames with good FCS. VLAN tagged frames that are greater than 1518 but less than 1522 bytes in size are also counted by this counter.	framesReceived
Bytes Sent & Rate	A counter that counts the total number of bytes transmitted.	bytesSent
Bytes Received & Rate	A counter that counts the total number of bytes received.	bytesReceived
Bits Sent & Rate	A counter that counts the total number of bits transmitted.	bitsSent
Bits Received & Rate	A counter that counts the total number of bits received.	bitsReceived
Scheduled Transmit Time	The scheduled transmit time associated with the port.	scheduledTransmitTime
CPU Status	The status of the port's CPU.	portCpuStatus
CPU DoD Status	The status of the port's DoD process.	portCpuDodStatus

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Transmit Duration		
Transmit Duration	Reserved for future use	transmitDuration
Quality of Service		
Quality of Service 0 - 7 & Rate	Counters which increment each time a frame with that particular QoS setting is received. (N/A to OC192-3)	qualityOfService0 qualityOfService1 ...
Framer Stats		
Framer CRC Errors	CRC errors detected by the POS framer.	framerFCSErrors
Framer Abort	POS frames aborted by the Framer.	framerAbort
Framer Min Length & Rate	POS frames received with less than the minimum length.	framerMinLength
Framer Max Length & Rate	POS frames received with more than the maximum length.	framerMaxLength
Extended Framer Stats		
Framer Frames Sent	Reserved for future use.	framerFramesTx
Framer Frames Received	Reserved for future use.	framerFramesRx
Checksum Stats		
IP Packets Received	The number of IP packets received.	ipPackets
UDP Packets Received	The number of UDP packets received.	udpPackets
TCP Packets Received	The number of TCP packets received.	tcpPackets
IP Checksum Errors	The number of IP checksum errors detected.	ipChecksumErrors
UDP Checksum Errors	The number of UDP checksum errors detected.	udpChecksumErrors
TCP Checksum Errors	The number of TCP checksum errors detected.	tcpChecksumErrors
Data Integrity		
Data Integrity Frames	The number of data integrity frames received.	dataIntegrityFrames
Data Integrity Errors	The number of data integrity errors detected.	dataIntegrityErrors
Sequence Checking		
Sequence Frames	The number of sequence checking frames received.	sequenceFrames

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Sequence Errors	The number of sequence checking errors detected.	sequenceErrors
Small Sequence Errors	The number of times when the current sequence number minus the previous sequence number is less than or equal to the error threshold and not negative, or when the current sequence number is equal to the previous sequence number.	smallSequenceErrors
Big Sequence Errors	The number of times when the current sequence number minus the previous sequence number is greater than the error threshold.	bigSequenceErrors
Reverse Sequence Errors	The number of times when the current sequence number is less than the previous sequence number.	reverseSequenceErrors
Total Sequence Errors	The sum of the small, bug and reverse sequence errors.	totalSequenceErrors
Packet Group Mode		
Packets Skipped In Packet Group Mode	The number of packets which were not assigned to a packet group. This can occur if the packet contains the anticipated packet group signature, but is too short to hold the group ID.	packetsSkippedIn PacketGroupMode
IxRouter Stats		
General		
IxRouter Server Transmit	Packets transmitted by the protocol handler.	protocolServerTx
IxRouter Receive	Packets received by the protocol handler.	protocolServerRx
VLAN Dropped Frames	The number of VLAN frames dropped by the IxRouter.	protocolServerVlan DroppedFrames
ARP		
Transmit Arp Reply	Number of ARP replies generated.	txArpReply
Transmit Arp Request	Number of ARP requests generated.	txArpRequest
Receive Arp Reply	Number of ARP replies received.	rxArpReply
Receive Arp Request	Number of ARP requests received.	rxArpRequest
ICMP		
Receive Ping Reply	Number of Ping replies received. (N/A to OC192-3)	rxPingReply

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Receive Ping Request	Number of Ping requests generated. (N/A to OC192-3)	rxPingRequest
Transmit Ping Reply	Number of Ping replies generated. (N/A to OC192-3)	txPingReply
Transmit Ping Request	Number of Ping requests received. (N/A to OC192-3)	txPingRequest
Asynchronous Frames Sent	The number of frames sent as a result of user request	asynchronousFramesSent
Scheduled Frames Sent	The number of frames originating from the stream engine.	scheduledFramesSent
Port CPU Frames Sent	The number of frames originating from the port's CPU as opposed to the stream engine.	portCPUFramesSent
DHCPv4		
DHCPv4 Discovered Messages Sent	The number of Discovered messages sent	dhcpV4Discovered MessagesSent
DHCPv4 Offers Received	The number of Offer messages received.	dhcpV4OffersReceived
DHCPv4 Requests Sent	The number or Request messages sent.	dhcpV4RequestsSent
DHCPv4 ACKs Received	The number or ACK messages received.	dhcpV4AcksReceived
DHCPv4 NACKs Received	The number of NACK messages received	dhcpV4NacksReceived
DHCPv4 Releases Sent	The number of Release messages sent.	dhcpV4ReleasesSent
DHCPv4 Enabled Interfaces	The number of enabled interfaces.	dhcpV4EnabledInterfaces
DHCPv4 Addresses Learned	The number of address learned.	dhcpV4Addresses Learned
DHCPv6		
DHCPv6 Solicits Sent	The number of DHCPv6 Solicits Sent	dhcpV6SolicitsSent
DHCPv6 Advertisements Received	The number of DHCPv6 Advertisements Received.	dhcpV6Advertisements Received
DHCPv6 Requests Sent	The number of DHCPv6 Requests Sent.	dhcpV6RequestsSent
DHCPv6 Declines Received	The number of DHCPv6 Declines Received.	dhcpV6DeclinesSent
DHCPv6 Replies Received	The number of DHCPv6 Replies Received.	dhcpV6RepliesReceived
DHCPv6 Releases Sent	The number of DHCPv6 Releases Sent.	dhcpV6ReleasesSent
DHCPv6 Enabled Interfaces	The number of DHCPv6 Enabled Interfaces.	dhcpV6EnabledInterfaces
DHCPv6 Addresses Learned	The number of DHCPv6 Addresses Learned.	dhcpV6Addresses Learned

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Ethernet OAM Stats		
EOAM Information PDUs Sent	The number of OAM Information PDUs Sent	ethernetOAMInformation PDUs Sent
EOAM Information PDUs Received	The number of OAM Information PDUs Received	ethernetOAMInformation PDUs Received
EOAM Event Notification PDUs Received	The number of OAM Event Notification PDUs Received	ethernetOAMEventNotification PDUsReceived
EOAM Loopback Control PDUs Received	The number of OAM Loopback Control PDUs Received	ethernetOAMLoopback Control PDUsReceived
EOAM Organization PDUs Received	The number of OAM Organization PDUs Received	ethernetOAMOrgPDUs Received
EOAM Variable Request PDUs Received	The number of OAM Variable Request PDUs Received	ethernetOAMVariable Request PDUsReceived
EOAM Variable Response PDUs Received	The number of OAM Variable Response PDUs Received	ethernetOAMVariable Response PDUsReceived
EOAM Unsupported PDUs Received	The number of OAM Unsupported PDUs Received	ethernetOAMUnsupported PDUs Received
BGP		
BGP Sessions Configured	The number of BGP4 sessions that were configured.	bgpTotalSessions
BGP Sessions Established	The number of configured BGP4 sessions that established adjacencies.	bgpTotalSessionsEstablished
IGMP		
Received IGMP Frames	The number of IGMP frames received by all logical hosts after being internally broadcast (For newer IGMPv3 emulation).	rxIgmpFrames
Transmitted IGMP Frames	The number of IGMP frames transmitted. (For newer IGMPv3 emulation).	txIgmpFrames
ISIS		
ISIS L1 Sessions Configured	The total number of level 1 configured sessions.	isisSessionsConfiguredL1
ISIS L2 Sessions Configured	The total number of level 2 configured sessions.	isisSessionsConfiguredL2
ISIS L1 Sessions Up	The total number of level 1 configured sessions that are fully up.	isisSessionsUpL1
ISIS L2 Sessions Up	The total number of level 2 configured sessions that are fully up.	isisSessionsUpL2
MLD		

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
MLD Frames Received	The number of MLD frames received by all logical hosts after being internally broadcast.	rxMldFrames
MLD Frames Transmitted	The number of MLD frames transmitted.	txMldFrames
OSPF		
OSPF Total Sessions	The number of OSPF sessions that were configured.	ospfTotalSessions
OSPF Neighbors in Full State	The number of OSPF neighbors that are fully up.	ospfFullNeighbors
OSPFv3		
OSPFv3 Sessions Configured	The number of OSPFv3 sessions that were configured.	ospfV3SessionsConfigured
OSPFv3 Neighbors in Full State	The number of OSPFv3 neighbors that are fully up.	ospfV3SessionsUp
PIM-SM		
PIM-SM Routers Configured	The number of configured PIM-SM routers.	pimsmRoutersConfigured
PIM-SM Routers Running	The number of PIM-SM routers in the run state.	pimsmRoutersRunning
PIM-SM Learned Neighbors	The number of learned PIM-SM neighbors.	pimsmNeighborsLearned
RSVP		
RSVP Ingress LSPs Configured	The number of ingress LSPs configured.	rsvpIngressLSPsConfigured
RSVP Ingress LSPs Up	The number of ingress LSPs configured and running.	rsvpIngressLSPsUp
RSVP Egress LSPs Up	The number of egress LSPs configured and running.	rsvpEgressLSPsUp
LDP		
LDP Sessions Configured	The number of LDP sessions configured for targeted peers.	ldpSessionsConfigured
LDP Sessions Up	The number of LDP sessions configured and running with targeted peers.	ldpSessionsUp
LDP Basic Sessions Up	The number of LDP sessions up for broadcast peers.	ldpBasicSessionsUp
Ethernet		
Fragments & Rate	A counter that counts the number of frames less than 64 bytes in size with a bad FCS.	fragments

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Undersize & Rate	A counter that counts the number of frames less than 64 bytes in size with a good FCS.	undersize
Oversize & Rate	A counter that counts the number of frames greater than 1518 bytes in size. The following modules count oversize packets with both good and bad FCSs: 10/100 TX, and 10/100 MII. All other modules include oversize packets with a good FCSs only.	oversize
CRC Errors & Rate	A counter that counts all valid size frames that have CRC errors.	fcsErrors
Vlan Tagged Frames & Rate	A counter that counts the number of VLAN tagged frames.	vlanTaggedFrames Received
Line Errors & Rate	A counter that counts the number of 4B/5B (100Mbps) or 8B/10B (Gigabit) symbol errors.	symbolErrors
Flow Control Frames & Rate	A counter that counts the number of PAUSE frames received. This counter only increments when Flow Control is enabled for that port (using the port properties dialog).	flowControlFrames
10/100		
Alignment Errors & Rate	A counter that counts all frames that are **not** an integer multiple of 8 bits and have an invalid FCS. The frame is truncated to the nearest octet and then the FCS is validated. If the FCS is bad, then this frame is counted as an alignment error.	alignmentErrors
Dribble Errors & Rate	A counter that counts all frames that are **not** an integer multiple of 8 bits and have a valid FCS. The frame is truncated to the nearest octet and then the FCS is validated. If the FCS is good, then this frame is counted as a dribble bit error.	dribbleErrors
Collisions & Rate	A counter that counts all occurrences (only one count per frame or fragment) of the Collision Detect signal from the physical layer controller that are not late collisions.	collisions
Late Collisions & Rate	A counter that counts all collisions that occur after the 512th bit time (preamble included) or after the 56th byte.	lateCollisions
Collision Frames & Rate	A counter that counts the number of frames that were retransmitted due to one or more collisions.	collisionFrames

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Excessive Collision Frames & Rate	A counter that counts the number of frames that were attempted to be sent but had 16 or more consecutive collisions.	excessiveCollisionFrames
Gigabit		
Oversize and CRC Errors & Rate	A counter that counts the number of frames greater than 1518 bytes in size with a bad FCS.	oversizeAndCrcErrors
Line Error Frames & Rate	A counter that counts the number of frames received that contain symbol errors.	symbolErrorFrames
Byte Alignment Error & Rate	A counter that counts the number of times that a comma character is detected to be out of alignment.	synchErrorFrames
POS		
Section LOS	'OK' or 'ALARM' during loss of signal. (See note 3 in *Notes*.)	sectionLossOfSignal
Section LOF	'OK' or 'ALARM' during loss of frame. (See note 3 in *Notes*.)	sectionLossOfFrame
Section BIP(B1) & Rate	The number of section bit interleaved parity errors.	sectionBip
Line AIS	'OK' or 'ALARM' during a line alarm indication signal condition. (See note 3 in *Notes*.)	lineAis
Line RDI	'OK' or 'ALARM' during a remote defect indication. (See note 3 in *Notes*.)	lineRdi
Line REI(FEBE) & Rate	A count of the number of remote error indicate conditions.	lineRei
Line BIP(B2) & Rate	The number of line bit interleaved parity errors.	lineBip
Path AIS	'OK' or 'ALARM' during a path alarm indication signal condition. (See note 3 in *Notes*.)	pathAis
Path RDI	'OK' or 'ALARM' during a path remote defect indication. (See note 3 in *Notes*.)	pathRdi
Path REI(FEBE) & Rate	A count of the number of path remote error indicate conditions.	pathRei
Path BIP(B3) & Rate	The number of path bit interleaved parity errors.	pathBip
Path LOP	'OK' or 'ALARM' during a loss of pointer condition. (See note 3 in *Notes*.)	pathLossOfPointer

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Path PLM(C2)	Either 'OK' or 'ALARM' along with the current received path signal label byte. 'ALARM' occurs when a path signal label mismatch occurs. (See note 5 in *Notes*.)	pathPlm
Section BIP Errored Seconds	A count of the number of seconds during which (at any point during the second) at least one section layer BIP was detected.	sectionBipErroredSecs
Section BIP Severely Errored Seconds	A count of the number of seconds during which K or more Section layer BIP errors were detected, where K = 2,392 for OC-48 (per ANSI T1.231-1997).	sectionBipSeverlyErrored Secs
Section LOS Seconds	A count of the number of seconds during which (at any point during the second) at least one section layer LOS defect was present.	sectionLossOfSignalSecs
Line BIP Errored Seconds	A count of the seconds during which (at any point during the second) at least one Line layer BIP was detected.	lineBipErroredSecs
Line REI Errored Seconds	A count of the seconds during which at least one line BIP error was reported by the far end.	lineReiErroredSecs
Line AIS Alarmed Seconds	A count of the seconds during which (at any point during the second) at least one Line layer AIS defect was present.	lineAisAlarmSecs
Line RDI Unavailable Seconds	A count of the seconds during which the line is considered unavailable at the far end.	lineRdiUnavailableSec
Path BIP Errored Seconds	A count of the seconds during which (at any point during the second) at least one Path BIP error was detected.	pathBipErroredSecs
Path REI Errored Seconds	A count of the seconds during which (at any point during the second) at least one STS Path error was reported by the far end.	pathReiErroredSecs
Path AIS Alarmed Seconds	A count of the seconds during which (at any point during the second) an AIS defect was present)	pathAisAlarmSec
Path AIS Unavailable Seconds	A count of the seconds during which the STS path was considered unavailable.	pathAisUnavailableSecs
Path RDI Unavailable Seconds	A count of the seconds during which the STS path was considered unavailable at the far end.	pathRdiUnavailableSec
Input Signal Strength (dB)	(OC-192) This statistic monitors the receive optical input power. (See note 8 in *Notes*)	inputSignalStrength

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
POS K1 Byte	Monitors the k1 status byte in SONET Headers.	posK1byte
POS K2 Byte	Monitors the k1 status byte in SONET Headers.	posK2byte
SRP		
SRP Data Frames Received	The number of data frames received. IPv4 frames fall in this category.	srpDataFramesReceived
SRP Discovery Frames Received	The number of discovery type frames received.	srpDiscoveryFrames Received
SRP IPS Frames Received	The number of IPS type frames received.	srpIpsFramesReceived
SRP Header Parity Errors	The number of SRP frames received with SRP header parity error. This includes all frame types.	srpParityErrors
SRP Usage Frames Received	The number of usage frames received with good CRC, good header parity, and only those that match the MAC address set for the SRP's port. Bad CRC frames, frames with header errors or those with other MAC addresses are received but not counted.	srpUsageFrames Received
SRP Usage Frames Sent	The number of usage frames sent.These are sent periodically to keep the link alive.	srpUsageFramesSent
SRP Usage Status	If the number of consecutive timeouts exceeds the Keep Alive threshold, this status changes to FAIL. Otherwise shows OK.	srpUsageStatus
SRP Usage Timeouts	The number of times a usage frame was not received within the time period.	srpUsageTimeouts
RPR		
RPR Discovery Frames Received	The number of RPR discovery frames received.	rprDiscoveryFrames Received
RPR Data Frames Received	The number of RPR encapsulated data frames received.	rprDataFramesReceived
RPR Fairness Frames Received	The number of RPR fairness frames received.	rprFairnessFrames Received
RPR Fairness Frames Sent	The number of RPR fairness frames sent.	rprFairnessFramesSent
RPR Timeout Events	The number of timeouts that occurred waiting for RPR fairness frames.	rprFairnessTimeouts
RPR Header CRC Errors	The number of RPR frames received with header CRC errors.	rprHeaderCrcErrors
RPR OAM Frames Received	The number of RPR OAM frames received.	rprOamFramesReceived

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
RPR Payload CRC Errors	The number of RPR frames received with payload CRC errors.	rprPayloadCrcErrors
RPR Protection Frames Received	The number of RPR protection frames received.	rprProtectionFrames Received
RPR Idle Frames Received	The number or RPR idle frames received.	rprIdleFramesReceived
GFP		
GFP Idle Frames	The number of GFP idle frames received.	gfpIdleFrames
GFP Sync State	The GFP sync state.	gfpSyncState
GFP SYNC/HUNT Transitions	The number of Sync/Hunt state transition frames received.	gfpSyncHuntTransitions
GFP eHEC Errors	Number of GFP extension header HEC errors detected.	gfpeHecErrors
GFP Payload FCS Errors	Number of payload FCS errors detected.	gfpPayloadFcsErrors
GFP Receive Bandwidth	The measured receive GFP bandwidth, in Mbps.	gfpRxBandwidth
GFP tHEC Errors	Number of GFP type header HEC errors detected.	gfptHecErrors
BERT		
BERT Status	For BERT: The status of the connection. ‘Locked’ when the receiving interface locks onto the data pattern. (See note 1 in *Notes*)	bertStatus
BERT Bits Sent	For BERT, it is the total number of bits sent.	bertBitsSent
BERT Bits Received	For BERT, it is the total number of bits received.	bertBitsReceived
BERT Bit Errors Sent	For BERT, it is the total number of bit errors sent.	bertBitErrorsSent
BERT Bit Errors Received	For BERT, it is the total number of bit errors received.	bertBitErrorsReceived
BERT Bit Error Ratio	For BERT, it is the ratio of the number of errored bits compared to the total number of bits transmitted.	bertBitErrorRatio
BERT Errored Blocks	For BERT—(EB) Number of blocks containing at least one errored second.	bertErroredBlocks
BERT Errored Seconds	For BERT—(ES) Number of seconds containing at least one errored block or a defect.	bertErroredSeconds
BERT Errored Second Ratio	For BERT—(ESR) the ratio of Errored Seconds (ES) to the total seconds.	bertErroredSecondRatio

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
BERT Severely Errored Seconds	For BERT—(SES) Number of seconds with 30% or more of the errored blocks or a defect.	bertSeverelyErrored Seconds
BERT Severely Errored Second Ratio	For BERT—(SESR) the ratio of Severely Errored Seconds (SESs) to the total seconds in available time.	bertSeverelyErrored SecondsRatio
BERT Error Free Seconds	For BERT—(EFS) Number of seconds with no errored blocks or defects.	bertErrorFreeSeconds
BERT Available Seconds	For BERT—(AS) Number of seconds which have occurred during Available Periods.	bertAvailableSeconds
BERT Unavailable Seconds	For BERT—(UAS) Number of seconds which have occurred during Unavailable Periods.	bertUnavailableSeconds
BERT Block Error State	For BERT—Available Period or Unavailable Period, determined according to the running count and calculation of seconds in various error conditions. A min. of 10 non-SESs must pass for the state to change from Unavailable to Available. A min. of 10 SESs must pass for the state to change from Available to Unavailable. (See note 4 in *Notes*.)	bertBlockErrorState
BERT Background Block Errors	For BERT—(BBE) The number of errored blocks not occurring as part of a Severely Errored Second.	bertBackgroundBlock Errors
BERT Background Block Error Ratio	For BERT—(BBER) the ratio of Background Block Errors (BBEs) to the total number of blocks in available time.	bertBackgroundBlockError Ratio
BERT Elapsed Test Time	For BERT—the elapsed test time, expressed in seconds.	bertElapsedTestTime
BERT Number Mismatched Zeros	The number of expected zeroes received as ones.	bertNumberMismatched Zeros
BERT Mismatched Zeros Ratio	The ratio of the number of expected zeroes received as ones to all bits.	bertismatchedZerosRatio
BERT Number Mismatched Ones	The number of expected ones received as zeroes.	bertNumberMismatched Ones
BERT Mismatched Ones Ratio	The ratio of the number of expected ones received as zeroes to all bits.	bertMismatchedOnes Ratio

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Service Disruption	A service disruption is the period of time during which the service is unavailable while switching rings. The SONET spec calls for this to be less than 50 ms.	
Last Service Disruption Time (ms)	The length of the last service disruption that occurred, expressed in milliseconds.	bertLastServiceDisruption Time
Min Service Disruption Time (ms)	The shortest service disruption that occurred, expressed in milliseconds.	bertMinServiceDisruption Time
Max Service Disruption Time (ms)	The longest service disruption that occurred, expressed in milliseconds.	bertMaxServiceDisruption Time
Cumulative Service Disruption Time (ms)	The total service disruption time encountered, expressed in milliseconds.	bertServiceDisruption Cumulative
DCC		
DCC Bytes Received	The number of DCC bytes received.	dccBytesReceived
DCC Bytes Sent	The number of DCC bytes sent.	dccBytesSent
DCC CRC Receive Errors	The number of DCC CRC errors received.	dccCrcErrorsReceived
DCC Frames Received	The number of DCC frames received.	dccFramesReceived
DCC Frames Sent	The number of DCC frames sent.	dccFramesSent
DCC Framing Errors Received	The number of DCC framing errors received.	dccFramingErrors Received
Link Fault Signalling		
Insertion State	The current state of link fault insertion. 0 = not inserting, 1 = inserting.	insertionState
Link Fault State	The current state of link fault detection on a port. 0 = no fault, 1 = local fault, 2 = remote fault.	linkFaultState
Local Faults	The number of local faults detected.	localFaults
Remote Faults	The number of remote faults detected.	remoteFaults
CDL	Converged Data Layer	
CDL Error Frames Received	The number of CDL error frames received.	cdlErrorFramesReceived
CDL Good Frames Received	The number of good CDL frames received.	cdlGoodFramesReceived.
FEC	Forwarding Error Correction	
FEC Corrected 0s Count	Number of 0 errors (1s changed to 0s) that have been corrected.	fecCorrected0sCount
FEC Corrected 1s Count	Number of 1 errors (0s changed to 1s) that have been corrected.	fecCorrected1sCount

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
FEC Corrected Bits Count	Number of flipped bits errors (0s changed to 1s and vice versa) that have been corrected.	fecCorrectedBitsCount
FEC Corrected Bytes Count	Number of bytes that have had errors corrected.	fecCorrectedBytesCount
FEC Uncorrectable Subrow Count	Number of subrows that have had uncorrectable errors.	fecUncorrectableSubrow Count
OC192		
Temperature		
DMA Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the DMA chip.	dMATemperature
Capture Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the Capture chip.	captureTemperature
Latency Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the Latency chip.	latencyTemperature
Background Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the Background chip.	backgroundTemperature
Overlay Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the Overlay chip.	overlayTemperature
Front End Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the Front End Chip.	frontEndTemperature
Scheduler Chip Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature of the Scheduler Chip.	scheduleTemperature
Plm Internal Chip Temperature 1 (C)	(OC-192 - Temperature Sensors Stats) Internal temperature of temperature measuring device #1.	plmDevice1Internal Temperature
Plm Internal Chip Temperature 2 (C)	(OC-192 - Temperature Sensors Stats) Internal temperature of temperature measuring device #2.	plmDevice2Internal Temperature
Plm Internal Chip Temperature 3(C)	(OC-192 - Temperature Sensors Stats) Internal temperature of temperature measuring device #3.	plmDevice3Internal Temperature
Fom Port Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature for one of the sensors on the Fiber optic module (Fom).	fobPort1FpgaTemperature fobPort2FpgaTemperature
Fom Board Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature for one of the sensors on the Fiber optic module (Fom).	fobBoardTemperature
Fom Internal Temperature (C)	(OC-192 - Temperature Sensors Stats) Temperature for one of the sensors on the Fiber optic module (Fom).	fobDevice1Internal Temperature

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
VSR	The statistics in this sub-section relate to all VSR channels. See **VSR per Channel** statistics for further per-channel statistics.	
Rx Channel Protection Disabled	The status of the channel protection on the receiving interface.	rxChannelProtection Disabled[8]
Rx Channel Skew Error	The status of the channel skew error detection on the receiving interface.	rxChannelSkewError[8]
RX Channel Skew First	The channel number of the earliest channel to arrive on the receiving interface. If more than one channel arrives at the same time, Channel #1 has the highest priority and so on.	rxChannelSkewFirst[8]
Rx Channel Skew Last	The channel number of the latest channel to arrive on the receiving interface. If more than one channel arrives at the same time, Channel #1 has the highest priority, and so on.	rxChannelSkewLast[8]
Rx Channel Skew Max	This counter increments every time the channel skew is equal to or greater than the maximum channel skew.	rxChannelSkewMax[8]
Rx Channel Swapped	Indicates one or more channel swap errors.	rxChannelSwapped[8]
Rx Code Word Violation Error	Indicates one or more 8b/10b code word violation errors.	rxCodeWordViolation Error[8]
Rx CRC Corrected Errors	The number of corrected CRC block errors accumulated on the receiving interface.	rxCrcCorrectedError Counter[8]
Rx CRC Correction Disabled	Indicates the status of the CRC correction on the receiving interface.	rxCrcCorrectionDisabled[8]
Rx CRC Error	Indicates one or more detected CRC errors.	rxCrcError[8]
Rx CRC Uncorrected Errors	The number of uncorrected CRC block errors accumulated on the receiving interface.	rxCrcUnCorrectedError Counter[8]
Rx Hardware Error	The number of hardware errors detected on the receive side.	rxHardwareError[8]
Rx Loss Of Synchronization Counter	Indicates the number of times that a protection channels was in the loss of synchronization state.	rxLossOfSynchronization Counter[8]
Rx Multi-loss Of Synchronization Counter	Indicates the number of times that two or more data or protection channels were in the Loss of Synchronization state.	rxMultiLossOfSynchroniza tionCounter[8]

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Rx Multi-loss Of Synchronization Status	Indicates that two or more data or protection channels are in the Loss of Synchronization state.	rxMultiLossOfSynchronizationStatus[8]
Rx Out of Frame Counter	Indicates the number of frame errors for the receiving interface.	rxOutOfFrameCounter[8]
Rx Out of Frame Status	Indicates one or more out of frame errors for the receiving interface.	rxOutOfFrameStatus[8]
Rx Section BIP Error Counter	The number of Section BIP errors detected on the receiving interface.	rxSectionBipErrorCounter[8]
Tx Hardware Error Counter	The number of hardware errors detected on the transmit side.	txHardwareError[8]
Tx Out Of Frame Counter	The number of out of frame errors detected on the transmit side.	txOutOfFrameCounter[8]
Tx Out of Frame Status	Indicates one or more out of frame errors for the transmit interface.	txOutOfFrameStatus[8]
Tx Section BIP Error Counter	The number of Section Bit Interleaved Parity (BIP) errors which have been detected on the transmit interface.	txSectionBipErrorCounter[8]
VSR per Channel	The statistics in this sub-section relate to a specific VSR channel.	
Rx Code Word Violation Counter	This per-channel statistic indicates the number of codeword violations detected on the receiving channel interface. Codeword violations include running disparity errors, undefined codewords, and any control characters besides K28.5.	rxCodeWordViolationCounter[9]
Rx CRC Error Counter	This per-channel statistic indicates the number of corrected and uncorrected errors on the receive interface.	rxCrcErrorCounter[9]
Rx Loss Of Synchronization Status	This per-channel statistic indicates the loss of synchronization status of the receiving interface.	rxLossOfSynchronization[9]
Rx Out of Frame Status	This per-channel statistic indicates the out of frame status of the receiving interface for a particular channel.	rxOutOfFrame[9]
10 Gig		
LSM		
Local Ordered Sets Sent	The number of local ordered sets sent. Ordered sets are part of Link Fault Signaling, and can be configured in the *Link Fault Signaling* tab.	localOrderedSetsSent

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Local Ordered Sets Received	The number of local ordered sets received. Ordered sets are part of Link Fault Signaling, and can be configured in the *Link Fault Signaling* tab.	localOrderedSets Received
Remote Ordered Sets Sent	The number of remote ordered sets sent.Ordered sets are part of Link Fault Signaling, and can be configured in the *Link Fault Signaling* tab.	remoteOrderedSetsSent
Remote Ordered Sets Received	The number of remote ordered sets received.Ordered sets are part of Link Fault Signaling, and can be configured in the *Link Fault Signaling* tab.	remoteOrderedSets Received
Custom Ordered Sets Sent	The number of custom ordered sets sent.Ordered sets are part of Link Fault Signaling, and can be configured in the *Link Fault Signaling* tab.	customOrderedSetsSent
Custom Ordered Sets Received	The number of custom ordered sets received.Ordered sets are part of Link Fault Signaling, and can be configured in the *Link Fault Signaling* tab.	customOrderedSets Received
Frames Received with Coding Errors	The number of frames received with coding errors.	codingErrorFrames Received
Frames Received with /E/ error Character	The number of frames received with DUT labeled errors received.	eErrorCharacterFrames Received
Dropped Frames	The number of dropped frames.	droppedFrames
Pause Frame		
Pause Acknowledge	The number of clocks for which transmit has been paused.	pauseAcknowledge
Pause End Frames	The number of pause frames received with a quanta of 0.	pauseEndFrames
Pause Overwrite	The number of pause frames received while transmit was paused with a quanta not equal to 0.	pauseOverwrite
Temperature		
Lan Transmit FPGA Temperature	For the 10Gig LAN board, the temperature at the transmit FPGA.	10GigLanTxFpga Temperature
Lan Receive FPGA Temperature	For the 10Gig LAN board, the temperature at the receive FPGA.	10GigLanRxFpga Temperature
ATM and ATM/POS		
ATM AAL5 Bytes Received	The number of AAL5 bytes received.	atmAal5BytesReceived
ATM AAL5 Bytes Sent	The number of AAL5 bytes sent.	atmAal5BytesSent

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
ATM AAL5 CRC Error Frames	The number of AAL5 frames received with CRC errors.	atmAal5CrcErrorFrames
ATM AAL5 Frames Received	The number of AAL5 frames received.	atmAal5FramesReceived
ATM AAL5 Frames Sent	The number of AAL5 frames sent.	atmAal5FramesSent
ATM AAL5 Length Error Frames	The number of AAL5 frames received with length errors.	atmAal5LengthError Frames
ATM AAL5 Timeout Error Frames	The number of AAL5 frames received with timeout errors.	atmAal5TimeoutError Frames
ATM Cells Received	The number of ATM cells received.	atmCellsReceived
ATM Cells Sent	The number of ATM cells sent.	atmCellsSent
ATM Corrected HCS Error Count	The number of AAL5 frames received with HCS errors that were corrected.	atmCorrectedHcsError Count
ATM Idle Cell Count	The number of idle ATM cells sent.	atmIdleCellCount
ATM Scheduled Cells Sent	The number of scheduled (non-idle) ATM cells sent.	atmScheduledCellsSent
ATM Uncorrected HCS Error Count	The number of AAL5 frames received with HCS errors that were not corrected.	atmUncorrectedHcsError Count
ATM Unregistered Cells	The number of unregistered ATM cells that were received.	atmUnregisteredCells Received
OAM Tx Cells	Number of ATM OAM cells transmitted.	atmOamTxCells
OAM Tx Bytes	Number of ATM OAM bytes transmitted.	atmOamTxBytes
OAM Tx Fault Management AIS	Number of ATM OAM Fault Management AIS cells transmitted.	atmOamTxFaultMgmtAIS
OAM Tx Fault Management RDI	Number of ATM OAM Fault Management RDI cells transmitted.	atmOamTxFaultMgmtRDI
OAM Tx Fault Management CC	Number of ATM OAM Fault Management CC cells transmitted.	atmOamTxFaultMgmtCC
OAM Tx Fault Management LB	Number of ATM OAM Fault Management LB cells transmitted.	atmOamTxFaultMgmtLB
OAM Tx Fault ActDeact CC	Number of ATM OAM ActDeact cells transmitted.	atmOamTxActDeactCC
OAM Rx Good Cells	Number of ATM OAM good cells received.	atmOamRxGoodCells
OAM Rx Bytes	Number of ATM OAM bytes received.	atmOamRxBytes
OAM Rx Fault Management AIS	Number of ATM OAM Fault Management AIS cells received.	atmOamRxFaultMgmtAIS
OAM Rx Fault Management RDI	Number of ATM OAM Fault Management RDI cells received.	atmOamRxFaultMgmtRDI

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
OAM Rx Fault Management CC	Number of ATM OAM Fault Management CC cells received.	atmOamRxFaultMgmtCC
OAM Rx Fault Management LB	Number of ATM OAM Fault Management LB cells received.	atmOamRxFaultMgmtLB
OAM Rx Bad Cells	Number or ATM OAM bad cells received.	atmOamRxBadCells
OAM Rx ActDeact CC	Number of ATM OAM ActDeact cells transmitted.	atmOamRxActDeactCC
Ethernet CRC	The Ethernet CRC, representing AAL5 CRCs.	ethernetCrc
Power Over Ethernet		
PoE Status	The PoE status.	poeStatus
PoE Input Voltage	The PoE input voltage.	poeInputVoltage
PoE Input Current	The PoE input current.	poeInputCurrent
PoE Input Power	The PoE input power.	poeInputPower
PoE Amplitude Arm Status	The state of the current signal acquisition arming for amplitude measurements.	poeAmplitudeArmStatus
PoE Amplitude Done Status	Indicates whether the signal acquisition of the amplitude measurement has occurred.	poeAmplitudeDoneStatus
PoE Amplitude Time Status	The state of the current signal acquisition arming for time measurements.	poeTimeArmStatus
PoE Amplitude Time Status	Indicates whether the signal acquisition of the time measurement has occurred.	poeTimeDoneStatus
PoE Trigger Amplitude DC Amps	The DC amps of the measured PoE amplitude measurements.	poeTriggerAmplitudeDC Amps
PoE Trigger Amplitude DC Volts	The DC voltage of the measured PoE amplitude measurements.	poeTriggerAmplitudeDC Volts
PoE Active Input	Displays the type of PSE in use, Alt. A or Alt B.	poeActiveInput
PoE Temperature	The temperature of the PoE port, in Celsius.	poeTemperature
PoE AutoCalibration	The stage in the port diagnostic test.	poeAutocalibration
Stream Extraction Module		
Bytes from Application	The number of bytes received on either port 2 or 3 from the application.	bytesFromApplication
Packets from Application	The number of packets received on either port 2 or 3 from the application.	packetsFromApplication

Table B-6. Statistics Counters

Counter	Interpretation	Internal Basename
Bytes from Port 2	The number of bytes received on the monitor port from port 2.	monitorBytesFromPort2
Bytes from Port 3	The number of bytes received on the monitor port from port 3.	monitorBytesFromPort3
Packets from Port 2	The number of packets received on the monitor port from port 2.	monitorPacketsFromPort2
Packets from Port 3	The number of packets received on the monitor port from port 3.	monitorPacketsFromPort3

Notes

Table B-7. Notes for Statistics Counters

NOTE	Choices Displayed for Statistic
1	Locked - All Ones
	Locked - Inverted Alternating One/Zero
	Locked - Inverted User Defined Pattern
	Locked - Inverted 2^31 Linear Feedback Shift Reg
	Locked - Inverted 2^11 Linear Feedback Shift Reg
	Locked - Inverted 2^15 Linear Feedback Shift Reg
	Locked - Inverted 2^20 Linear Feedback Shift Reg
	Locked - Inverted 2^23 Linear Feedback Shift Reg
	Locked - All Zero
	Locked - Alternating One/Zero
	Locked - User Defined Pattern
	Locked - 2^11 Linear Feedback Shift Reg
	Locked - 2^15 Linear Feedback Shift Reg
	Locked - 2^20 Linear Feedback Shift Reg
	Locked - 2^23 Linear Feedback Shift Reg
	Not Locked
2	Demo Mode
	Link Up
	Link Down
	Loopback
	WriteMii
	Restart AutoNegotiate
	End RestartAutoNegotiate
	AutoNegotiate
	WriteMii Failed
	No Transceiver
	Invalid PHY Address
	Read LinkPartner
	No LinkPartner
	FPGA Download Failed

Table B-7. Notes for Statistics Counters

NOTE	Choices Displayed for Statistic
	No GBIC Module
	Fifo Reset
	Fifo Reset Compete
	PPP Off
	PPP Up
	PPP Down
	PPP Init
	PPP WaitForOpen
	PPP AutoNegotiate
	PPP Close
	PPP Connect
	Loss of Frame
	Loss of Signal
	StateMachine Failure
	PPP RestartNegotiation
	PPP RestartNegotiation Init
	PPP RestartNegotiation WaitForOpen
	PPP RestartNegotiation WaitForClose
	PPP RestartNegotiation Finish
	LP Boot Failed
	PPP Disabled - LOF
	Ignore Link
	Temperature Alarm
	PPP Closing
	PPP LCP Negotiate
	PPP Authenticate
	PPP NCP Negotiate
3	OK
	Alarm
	'-'
	Defect

Table B-7. Notes for Statistics Counters

NOTE	Choices Displayed for Statistic
4	Unavailable Period
	Available Period
5	OK
	OK (%)
	Alarm (%)
	'-'
6	OC-3c
	OC-12c
	OC-48c
	OC-192c
	10GE WAN
	10 Mbps
	100 Mbps
	1000 Mbps
7	Full
	Half
8	Loss of Signal
	[-] %d.%d

Table B-7. Notes for Statistics Counters

NOTE	Choices Displayed for Statistic
8	The statistics in this section must be accessed using the *vsrStat* command in TCL and the *TCLvsrStat* class in C++.
9	The statistics in this section must be accessed using the *vsrStat* command in TCL and the *TCLvsrStat* class in C++. In addition, the desired channel must be set with the *getChannel* sub-command (TCL) or method (C++).

Table B-8. Statistics for 10/100 Cards

	Normal				Qos	StreamTrigger			
	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp	Capture	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp
Type: User Configurable									
UserDefinedStat1	X	X	X	X		X	X	X	X
UserDefinedStat2	X	X	X	X		X	X	X	X
CaptureTrigger	X		X			X		X	
CaptureFilter	X		X			X		X	
StreamTrigger1						X			
StreamTrigger2						X			
Type: States									
Link	X	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X
DuplexMode	X	X	X	X	X	X	X	X	X
TransmitState	X	X	X	X	X	X	X	X	X

Table B-8. Statistics for 10/100 Cards

	Normal				Qos	StreamTrigger			
	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp	Capture	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp
CaptureState	X	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X	X
Type: Common									
FramesSent	X	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X	X
BytesReceived	X	X	X	X		X	X	X	X
FcsErrors	X	X	X	X	X	X	X	X	X
BitsReceived	X	X	X	X		X	X	X	X
BitsSent	X	X	X	X	X	X	X	X	X
PortCpuStatus									
PortCpuDodStatus									
Type: Transmit Duration									
TransmitDuration	X	X		X	X	X	X		X
Type: Quality of Service									
QualityOfService0					X				
Type: Ethernet									
Fragments	X	X	X	X	X	X	X	X	X
Undersize	X	X	X	X	X	X	X	X	X
Oversize	X	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X		X					X	
FlowControlFrames	X	X	X	X	X	X	X	X	X
Type: 10/100									
AlignmentErrors	X	X	X	X	X	X	X	X	X

Table B-8. Statistics for 10/100 Cards

	Normal				Qos	StreamTrigger			
	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp	Capture	Capture	PacketGroup	RxTcpRoundTrip	RxFirstTimeStamp
DribbleErrors	X	X	X	X		X	X	X	X
Collisions	X	X	X	X	X	X	X	X	X
LateCollisions	X	X	X	X	X	X	X	X	X
CollisionFrames	X	X	X	X	X	X	X	X	X
ExcessiveCollisionFrames	X	X	X	X	X	X	X	X	X
Type: 10/100 + Gigabit									
SymbolErrors	X								
OversizeAndCrcErrors									

Table B-9. Statistics for 10/100 TXS Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X	X	X					X	X	X	X	X	X	X			X		X		X	X	X	X	X	X

Table B-9. Statistics for 10/100 TXS Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
CaptureTrigger	X	X	X		X		X					X	X	X		X		X	X	X		X		X	X	X		X		X
CaptureFilter	X	X	X		X		X					X	X	X		X		X	X	X		X		X	X	X		X		X
StreamTrigger1												X	X			X		X												
StreamTrigger2												X	X			X		X												
Type: States																														
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DuplexMode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Common																														
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesReceived	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsReceived	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PortCpuStatus	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-9. Statistics for 10/100 TXS Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
PortCpuDodStatus	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Transmit Duration																														
TransmitDuration	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Quality of Service																														
QualityOfService0								X	X	X	X																			
Type: Checksum Stats																														
IpPackets																			X	X		X		X						
UdpPackets																			X	X		X		X						
TcpPackets																			X	X		X		X						
IpChecksumErrors																			X	X		X		X						
UdpChecksumErrors																			X	X		X		X						
TcpChecksumErrors																			X	X		X		X						
Type: Data Integrity																														
DataIntegrityFrames				X											X						X						X			
DataIntegrityErrors				X											X						X						X			
Type: Sequence Checking																														
SequenceFrames						X											X						X						X	
SequenceErrors						X											X						X						X	
Type: Ethernet																														
Fragments	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-9. Statistics for 10/100 TXS Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Undersize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Oversize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X	X	X		X		X							X											X	X		X		X
FlowControlFrames	X	X	X		X		X	X	X	X	X	X	X	X		X		X							X	X		X		X
Type: 10/100																														
AlignmentErrors	X	X	X		X		X							X											X	X		X		X
DribbleErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Collisions	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LateCollisions	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
CollisionFrames	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ExcessiveCollisionFrames	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: 10/100 + Gigabit																														
SymbolErrors																														
OversizeAndCrcErrors	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-10. Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards

Statistics Mode	Normal					Qos			StreamTrigger					ModeChecksum Errors					ModeData Integrity				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Type: User Configurable																							
UserDefinedStat1	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X				X	X	X	X	X		X	X	X		X	X	X	X	X
CaptureTrigger	X		X		X				X		X	X	X	X		X	X	X	X			X	X
CaptureFilter	X		X		X				X		X	X	X	X		X	X	X	X			X	X
StreamTrigger1									X				X										
StreamTrigger2									X				X										
Type: States																							
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DuplexMode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Common																							
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-10. Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards

Statistics Mode	Normal					Qos			StreamTrigger					ModeChecksum Errors					ModeData Integrity				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
BytesReceived	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsReceived	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PortCpuStatus					X		X	X					X					X					X
PortCpuDodStatus					X		X	X					X					X					X
Type: Transmit Duration																							
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Quality of Service																							
QualityOfService0						X	X	X															
Type: Checksum Stats																							
IPv4Packets														X	X								
UdpPackets														X	X								
TcpPackets														X	X								
IPv4ChecksumErrors														X	X								
UdpChecksumErrors														X	X								
TcpChecksumErrors														X	X								
Type: Data Integrity																							
DataIntegrityFrames			X								X					X					X		
DataIntegrityErrors			X								X					X					X		

Table B-10. Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards

Statistics Mode	Normal					Qos			StreamTrigger					ModeChecksum Errors					ModeData Integrity				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Type: Sequence Checking																							
SequenceFrames				X								X					X					X	
SequenceErrors				X								X					X					X	
Type: Ethernet																							
Fragments	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Undersize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Oversize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X	X			X					X					X				X	X			X
FlowControlFrames	X	X			X	X	X	X	X	X			X		X				X	X			X
Type: 10/100																							
AlignmentErrors					X																		X
DribbleErrors					X		X	X					X					X					X
Collisions					X		X	X					X					X					X
LateCollisions					X		X	X					X					X					X
CollisionFrames					X		X	X					X					X					X
ExcessiveCollisionFrames					X		X	X					X					X					X
Type: Gigabit																							
SymbolErrorFrames	X	X	X	X					X	X	X	X			X	X	X		X	X	X	X	
SynchErrorFrames	X	X				X			X	X					X				X	X			

Table B-10. Statistics for 10/100/1000 TXS, 10/100/1000 XMS(R)12, 1000 SFPS4, and 1000STXS24 Cards

Statistics Mode	Normal					Qos			StreamTrigger					ModeChecksum Errors					ModeData Integrity				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Type: 10/100 + Gigabit																							
SymbolErrors	X	X								X					X				X	X			
OversizeAndCrcErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-11. Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards

Statistics Mode	Normal					Qos			StreamTrigger					ModeData Integrity				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Type: User Configurable																		
UserDefinedStat1	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X

Table B-11. Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards

Statistics Mode	**Normal**					**Qos**			**StreamTrigger**					**ModeData Integrity**				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
CaptureTrigger	X		X		X				X		X	X	X	X			X	X
CaptureFilter	X		X		X				X		X	X	X	X			X	X
StreamTrigger1									X				X					
StreamTrigger2									X				X					
Type: States																		
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DuplexMode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Common																		
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesReceived	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsReceived	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PortCpuStatus					X		X	X					X					X

Table B-11. Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards

Statistics Mode	Normal					Qos			StreamTrigger					ModeData Integrity				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
PortCpuDodStatus					X		X	X					X					X
Type: Transmit Duration																		
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Quality of Service																		
QualityOfService0						X	X	X										
Type: Checksum Stats																		
IPv4Packets	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UdpPackets	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TcpPackets	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
IPv4ChecksumErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UdpChecksumErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TcpChecksumErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Data Integrity																		
DataIntegrityFrames			X								X					X		
DataIntegrityErrors			X								X					X		
Type: Sequence Checking																		
SequenceFrames				X								X					X	
SequenceErrors				X								X					X	
Type: Ethernet																		
Fragments	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-11. Statistics for 10/100/1000 LSM XMV(R)4/8/12/16, and 10/100/1000 ASM XMV12X Cards

Statistics Mode	**Normal**					**Qos**			**StreamTrigger**					**ModeData Integrity**				
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Undersize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Oversize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X	X			X					X				X	X			X
FlowControlFrames	X	X			X	X	X	X	X	X			X	X	X			X
Type: 10/100																		
AlignmentErrors					X													X
DribbleErrors					X		X	X					X					X
Collisions					X		X	X					X					X
LateCollisions					X		X	X					X					X
CollisionFrames					X		X	X					X					X
ExcessiveCollisionFrames					X		X	X					X					X
Type: Gigabit																		
SymbolErrorFrames	X	X	X	X					X	X	X	X		X	X	X	X	
SynchErrorFrames	X	X				X			X	X				X	X			
Type: 10/100 + Gigabit																		
SymbolErrors	X	X								X				X	X			
OversizeAndCrcErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-12. Statistics for Gigabit Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X	X	X					X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X
CaptureTrigger	X		X	X			X					X		X	X		X	X	X		X		X	X	X				X	X
CaptureFilter	X		X	X			X					X		X	X		X	X	X		X		X	X	X				X	X
StreamTrigger1												X						X												
StreamTrigger2												X						X												
Type: States																														
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DuplexMode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Common																														
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesReceived	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-12. Statistics for Gigabit Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsReceived	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PortCpuStatus							X		X	X	X							X						X						X
PortCpuDodStatus							X		X	X	X							X						X						X
Type: Transmit Duration																														
TransmitDuration	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Quality of Service																														
QualityOfService0								X	X	X	X																			
Type: Checksum Stats																														
IpPackets																			X					X						
UdpPackets																			X					X						
TcpPackets																			X					X						
IpChecksumErrors																			X					X						
UdpChecksumErrors																			X					X						
TcpChecksumErrors																			X					X						
Type: Data Integrity																														
DataIntegrityFrames				X											X						X						X			
DataIntegrityErrors				X											X						X						X			

Table B-12. Statistics for Gigabit Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
Type: Sequence Checking																														
SequenceFrames						X											X						X						X	
SequenceErrors						X											X						X						X	
Type: Ethernet																														
Fragments	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Undersize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Oversize	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X	X	X		X		X						X	X		X				X		X			X	X		X		X
FlowControlFrames	X	X	X		X		X	X	X	X	X	X	X	X		X		X		X		X			X	X		X		X
Type: 10/100																														
AlignmentErrors			X				X							X																X
DribbleErrors			X				X		X	X	X			X				X						X						X
Collisions			X				X		X	X	X			X				X						X						X
LateCollisions			X				X		X	X	X			X				X						X						X
CollisionFrames			X				X		X	X	X			X				X						X						X
ExcessiveCollisionFrames			X				X		X	X	X			X				X						X						X
Type: Gigabit																														
SymbolErrorFrames	X	X		X	X	X						X	X		X	X	X			X	X	X	X		X	X	X	X	X	
SynchErrorFrames	X	X			X			X				X	X			X				X		X			X	X		X		
Type: 10/100 + Gigabit																														

Table B-12. Statistics for Gigabit Modules

	Normal							Qos				StreamTrigger							ModeChecksumErrors						ModeDataIntegrity					
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup
SymbolErrors	X	X			X								X			X				X		X			X	X		X		
OversizeAndCrcErrors	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-13. Statistics for OC12c/OC3c Modules

	Normal							Qos				StreamTrigger							ModeChecksum Errors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PosExtendedStats	
Type: User Configurable																																
UserDefinedStat1	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X	X					X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X		
CaptureTrigger	X		X				X					X		X				X	X					X	X					X		
CaptureFilter	X		X				X					X		X				X	X					X	X					X		

Table B-13. Statistics for OC12c/OC3c Modules

	Normal							Qos				StreamTrigger							ModeChecksum Errors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PosExtendedStats	
StreamTrigger1												X	X					X														
StreamTrigger2												X	X					X														
Type: States																																
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode			X		X		X			X	X			X		X		X				X		X				X		X		
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsReceived	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus							X			X	X							X						X						X		
PortCpuDodStatus							X			X	X							X						X						X		
Type: Transmit Duration																																

Table B-13. Statistics for OC12c/OC3c Modules

	Normal							Qos				StreamTrigger							ModeChecksum Errors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PosExtendedStats	
TransmitDuration	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																																
QualityOfService0								X	X	X	X																					
Type: Framer																																
FramerFCSErrors																																
FramerAbort																															X	
FramerMinLength																															X	
FramerMaxLength																															X	
Type: Checksum Stats																																
IpPackets																			X					X								
UdpPackets																			X					X								
TcpPackets																			X					X								
IpChecksumErrors																			X					X								
UdpChecksumErrors																			X					X								
TcpChecksumErrors																			X					X								
Type: Data Integrity																																
DataIntegrityFrames				X											X						X						X					
DataIntegrityErrors				X											X						X						X					
Type: Sequence Checking																																

Table B-13. Statistics for OC12c/OC3c Modules

	Normal							Qos				StreamTrigger							ModeChecksum Errors							ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PosExtendedStats	
SequenceFrames						X											X						X							X			
SequenceErrors						X											X						X							X			
Type: Ethernet																																	
Fragments			X		X		X			X	X			X		X		X				X		X				X		X			
Undersize			X		X		X			X	X			X		X		X				X		X				X		X			
Oversize			X		X		X			X	X			X		X		X				X		X				X		X			
VlanTaggedFramesRx			X		X		X							X		X						X						X		X			
FlowControlFrames			X		X		X			X	X			X		X		X				X						X		X			
Type: 10/100																																	
AlignmentErrors			X				X							X										X						X			
DribbleErrors			X				X			X	X			X				X						X						X			
Collisions			X				X			X	X			X				X						X						X			
LateCollisions			X				X			X	X			X				X						X						X			
CollisionFrames			X				X			X	X			X				X						X						X			
ExcessiveCollisionFrames			X				X			X	X			X				X						X						X			
Type: Gigabit																																	
SymbolErrorFrames					X											X						X						X					
SynchErrorFrames					X											X						X						X					
Type: 10/100 + Gigabit																																	
SymbolErrors					X											X						X						X					

Table B-13. Statistics for OC12c/OC3c Modules

	Normal							Qos				StreamTrigger							ModeChecksum Errors							ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PosExtendedStats	
OversizeAndCrcErrors					X		X			X	X					X		X				X		X				X		X		
Type: POS																																
SectionLossOfSignal																															X	
SectionLossOfFrame																															X	
SectionBip																															X	
LineAis																															X	
LineRdi																															X	
LineRei																															X	
LineBip																															X	
PathAis																															X	
PathRdi																															X	
PathRei																															X	
PathBip																															X	
PathLossOfPointer																															X	
PathPlm																															X	
SectionBipErroredSecs																																
SectionBipSeverlyErrored Secs																																
SectionLossOfSignalSecs																																
LineBipErroredSecs																																

Table B-13. Statistics for OC12c/OC3c Modules

	Normal							Qos				StreamTrigger							ModeChecksum Errors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeWidePacketGroup	PosExtendedStats	
LineReiErroredSecs																																
LineAisAlarmSecs																																
LineRdiUnavailableSecs																																
PathBipErroredSecs																																
PathReiErroredSecs																																
PathAisAlarmSecs																																
PathAisUnavailableSecs																																
PathRdiUnavailableSecs																																
InputSignalStrength																																
PosK1Byte																																
PosK2Byte																																
SrpDataFramesReceived																																
SrpDiscoveryFrames Received																																
SrpIpsFramesReceived																																
SrpParityErrors																																
SrpUsageFramesReceived																																
SrpUsageStatus																																
SrpUsageTimeouts																																

Table B-14. Statistics for OC48c Modules with BERT

	Normal								Qos						StreamTrigger								ModeChecksum Errors							ModeDataIntegrity							Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PosExtendedStats	
Type: User Configurable																																						
UserDefinedStat1	X	X	X	X	X	X	X	X							X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X	X	X							X	X	X	X	X	X	X	X		X	X	X	X			X	X	X	X	X	X	X		
CaptureTrigger	X		X					X							X		X					X	X					X	X	X						X		
CaptureFilter	X		X					X							X		X					X	X						X	X						X		
StreamTrigger1															X	X				X	X	X																
StreamTrigger2															X	X				X	X	X																
Type: States																																						
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode			X		X			X			X			X			X		X			X				X			X				X			X		
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																						
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	X	X							X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-14. Statistics for OC48c Modules with BERT

	Normal								Qos						StreamTrigger								ModeChecksum Errors							ModeDataIntegrity							Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PosExtendedStats	
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsReceived	X	X	X	X	X	X	X	X							X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X		X		X		X	X	X	X	X		X	X	X		X		X		X	X	X	X		X		X	X	X	X		X		X		
PortCpuDodStatus	X	X		X		X		X	X	X	X	X		X	X	X		X		X		X	X	X	X		X		X	X	X	X		X		X		
Type: Transmit Duration																																						
TransmitDuration	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																																						
QualityOfService0									X	X	X	X	X	X																								
Type: Checksum Stats																																						
IpPackets																							X					X	X									
UdpPackets																							X					X	X									
TcpPackets																							X					X	X									
IpChecksumErrors																							X					X	X									
UdpChecksumErrors																							X					X	X									
TcpChecksumErrors																							X					X	X									
Type: Data Integrity																																						
DataIntegrityFrames				X														X							X							X						
DataIntegrityErrors				X														X							X							X						
Type: Sequence Checking																																						

Table B-14. Statistics for OC48c Modules with BERT

	Normal								Qos						StreamTrigger								ModeChecksum Errors						ModeDataIntegrity							Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PosExtendedStats	
SequenceFrames						X						X								X							X							X				
SequenceErrors						X						X								X							X							X				
Type: Ethernet																																						
Fragments			X		X			X			X			X			X		X			X				X			X				X			X		
Undersize			X		X			X			X			X			X		X			X				X			X				X			X		
Oversize			X		X			X			X			X			X		X			X				X			X				X			X		
VlanTaggedFramesRx			X		X			X									X		X							X							X			X		
FlowControlFrames			X		X			X			X			X			X		X			X				X							X			X		
Type: 10/100																																						
AlignmentErrors			X					X									X																			X		
DribbleErrors			X					X			X			X			X					X							X							X		
Collisions			X					X			X			X			X					X							X							X		
LateCollisions			X					X			X			X			X					X							X							X		
CollisionFrames			X					X			X			X			X					X							X							X		
ExcessiveCollisionFrames			X					X			X			X			X					X							X							X		
Type: Gigabit																																						
SymbolErrorFrames					X														X							X							X					
SynchErrorFrames					X														X							X							X					
Type: 10/100 + Gigabit																																						
SymbolErrors					X														X							X							X					

Table B-14. Statistics for OC48c Modules with BERT

	Normal								Qos						StreamTrigger								ModeChecksum Errors							ModeDataIntegrity							Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PosExtendedStats	
OversizeAndCrcErrors					X			X			X			X					X			X				X			X				X			X		
Type: POS																																						
SectionLossOfSignal																																					X	
SectionLossOfFrame																																					X	
SectionBip																																					X	
LineAis																																					X	
LineRdi																																					X	
LineRei																																					X	
LineBip																																					X	
PathAis																																					X	
PathRdi																																					X	
PathRei																																					X	
PathBip																																					X	
PathLossOfPointer																																					X	
PathPlm																																					X	
SectionBipErroredSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
SectionBipSeverlyErrored Secs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
SectionLossOfSignalSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
LineBipErroredSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
LineReiErroredSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			

Table B-14. Statistics for OC48c Modules with BERT

	Normal								Qos						StreamTrigger								ModeChecksum Errors							ModeDataIntegrity							Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeWidePacketGroup	PosExtendedStats	
LineAisAlarmSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
LineRdiUnavailableSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
PathBipErroredSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
PathReiErroredSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
PathAisAlarmSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
PathAisUnavailableSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
PathRdiUnavailableSecs	X	X		X		X	X		X	X		X	X		X	X		X		X	X		X	X	X		X	X		X	X	X		X	X			
InputSignalStrength																																							
PosK1Byte																																							
PosK2Byte																																							
SrpDataFramesReceived																																							
SrpDiscoveryFrames Received																																							
SrpIpsFramesReceived																																							
SrpParityErrors																																							
SrpUsageFramesReceived																																							
SrpUsageStatus																																							
SrpUsageTimeouts																																							

Table B-15. Statistics for OC48c Modules with SRP and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X					X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X		
CaptureTrigger	X										X						X					X	X					X		
CaptureFilter	X										X						X						X					X		
StreamTrigger1											X	X			X	X														
StreamTrigger2											X	X			X	X														
Type: States																														
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X										X						X						X				
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																														
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-15. Statistics for OC48c Modules with SRP and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
BitsReceived	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PortCpuDodStatus	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
Type: Transmit Duration																														
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																														
QualityOfService0							X	X	X	X																				
Type: Checksum Stats																														
IpPackets																	X					X								
UdpPackets																	X					X								
TcpPackets																	X					X								
IpChecksumErrors																	X					X								
UdpChecksumErrors																	X					X								
TcpChecksumErrors																	X					X								
Type: Data Integrity																														
DataIntegrityFrames			X										X						X						X					
DataIntegrityErrors			X										X						X						X					
Type: Sequence Checking																														
SequenceFrames					X				X						X						X						X			
SequenceErrors					X				X						X						X						X			

Table B-15. Statistics for OC48c Modules with SRP and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
Type: Ethernet																														
Fragments				X										X						X						X				
Undersize				X										X						X						X				
Oversize				X										X						X						X				
VlanTaggedFramesRx				X										X						X						X				
FlowControlFrames				X										X						X						X				
Type: Gigabit																														
SymbolErrorFrames				X										X						X						X				
SynchErrorFrames				X										X						X						X				
Type: 10/100 + Gigabit																														
SymbolErrors				X										X						X						X				
OversizeAndCrcErrors				X										X						X						X				
Type: POS																														
SectionLossOfSignal																													X	
SectionLossOfFrame																													X	
SectionBip																													X	
LineAis																													X	
LineRdi																													X	
LineRei																													X	
LineBip																													X	
PathAis																													X	
PathRdi																													X	

Table B-15. Statistics for OC48c Modules with SRP and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
PathRei																													X	
PathBip																													X	
PathLossOfPointer																													X	
PathPlm																													X	
SectionBipErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
SectionBipSeverlyErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
SectionLossOfSignalSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineBipErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineReiErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineAisAlarmSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathBipErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathReiErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathAisAlarmSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathAisUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
InputSignalStrength																														
PosK1Byte	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
PosK2Byte	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpDataFramesReceived	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		

Table B-15. Statistics for OC48c Modules with SRP and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
SrpDiscoveryFrames Received	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpIpsFramesReceived	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpParityErrors	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpUsageFramesReceived	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpUsageStatus	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
SrpUsageTimeouts	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
Type: DCC																														
DccBytesReceived						X				X						X						X						X		
DccBytesSent																														
DccCrcErrorsReceived						X				X						X						X						X		
DccFramesReceived						X				X						X						X						X		
DccFramesSent																														
DccFramingErrors Received																														

Table B-16. Statistics for OC48c Modules with RPR and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
Type: User Configurable																														
UserDefinedStat1	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X					X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X		
CaptureTrigger	X										X						X					X	X					X		
CaptureFilter	X										X						X						X					X		
StreamTrigger1											X	X			X	X														
StreamTrigger2											X	X			X	X														
Type: States																														
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X										X						X						X				
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																														
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-16. Statistics for OC48c Modules with RPR and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
BitsReceived	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PortCpuDodStatus	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
Type: Transmit Duration																														
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																														
QualityOfService0							X	X	X	X																				
Type: Checksum Stats																														
IpPackets																	X					X								
UdpPackets																	X					X								
TcpPackets																	X					X								
IpChecksumErrors																	X					X								
UdpChecksumErrors																	X					X								
TcpChecksumErrors																	X					X								
Type: Data Integrity																														
DataIntegrityFrames			X										X						X						X					
DataIntegrityErrors			X										X						X						X					
Type: Sequence Checking																														
SequenceFrames					X				X						X						X						X			
SequenceErrors					X				X						X						X						X			

Table B-16. Statistics for OC48c Modules with RPR and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
Type: Ethernet																														
Fragments				X										X						X						X				
Undersize				X										X						X						X				
Oversize				X										X						X						X				
VlanTaggedFramesRx				X										X						X						X				
FlowControlFrames				X										X						X						X				
Type: Gigabit																														
SymbolErrorFrames				X										X						X						X				
SynchErrorFrames				X										X						X						X				
Type: 10/100 + Gigabit																														
SymbolErrors				X										X						X						X				
OversizeAndCrcErrors				X										X						X						X				
Type: POS																														
SectionLossOfSignal																													X	
SectionLossOfFrame																													X	
SectionBip																													X	
LineAis																													X	
LineRdi																													X	
LineRei																													X	
LineBip																													X	
PathAis																													X	

Table B-16. Statistics for OC48c Modules with RPR and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
PathRdi																													X	
PathRei																													X	
PathBip																													X	
PathLossOfPointer																													X	
PathPlm																													X	
SectionBipErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
SectionBipSeverlyErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
SectionLossOfSignalSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineBipErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineReiErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineAisAlarmSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
LineRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathBipErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathReiErroredSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathAisAlarmSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathAisUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
PathRdiUnavailableSecs	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X	X		X	X	X	X	X		X	X		
InputSignalStrength																														
PosK1Byte																														
PosK2Byte																														
SrpDataFramesReceived																														

Table B-16. Statistics for OC48c Modules with RPR and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
SrpDiscoveryFrames Received																														
SrpIpsFramesReceived																														
SrpParityErrors																														
SrpUsageFramesReceived																														
SrpUsageStatus																														
SrpUsageTimeouts																														
Type: DCC																														
DccBytesReceived						X				X						X						X						X		
DccBytesSent																														
DccCrcErrorsReceived						X				X						X						X						X		
DccFramesReceived						X				X						X						X						X		
DccFramesSent																														
DccFramingErrors Received																														
Type: RPR																														
RprDiscoveryFrames Received	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprDataFramesReceived	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprFairnessFrames Received	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprFairnessFramesSent	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprFairnessTimeouts	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		

Table B-16. Statistics for OC48c Modules with RPR and DCC

	Normal						Qos				StreamTrigger						ModeChecksumErrors						ModeDataIntegrity						Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	PosExtendedStats	
RprHeaderCrcErrors	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprOamFramesReceived	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprPayloadCrcErrors	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		
RprProtectionFrames Received	X	X	X		X	X					X	X	X		X	X							X	X	X		X	X		

Table B-17. Statistics for 2.5G MSM POS modules

	Normal								Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: User Configurable																																											
UserDefinedStat1	X	X	X	X	X		X	X	X	X	X	X	X			X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X		X	X	X	X	X	X	X			X	X	X	X	X	X	X		X	X	X				X			X	X	X	X	X	X	X	X	X		
CaptureTrigger	X	X	X		X				X	X	X	X	X			X	X	X	X	X		X			X	X					X			X	X	X		X			X		

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
CaptureFilter	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X	X							X	X	X		X				X		
StreamTrigger1	X	X	X		X				X	X	X	X	X				X	X	X	X		X		X	X	X								X	X	X		X				X		
StreamTrigger2	X	X	X		X				X	X	X	X	X				X	X	X	X		X		X	X	X								X	X	X		X				X		
Type: States																																												
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X																X										X							X						
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																											
FramesSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				X			X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				X			X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				X			X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X		X	X	X									X	X	X	X	X	X	X	X				X			X	X	X	X	X	X	X	X	X	X		
FcsErrors	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X	X	X	X	X		
BitsReceived	X	X	X	X	X		X	X	X									X	X	X	X	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X	X	X			X	X	X	X	X			X	X	X	X		X			X	X		
PortCpuDodStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X	X	X			X	X	X	X	X			X	X	X	X		X			X	X		

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: Transmit Duration																																									
TransmitDuration	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	
Type: Quality of Service																																									
QualityOfService0										X	X	X	X	X	X	X	X																										
Type: Checksum Stats																																									
IpPackets																										X	X	X		X		X											
UdpPackets																										X	X	X		X		X											
TcpPackets																										X	X	X		X		X											
IpChecksumErrors																										X	X	X		X		X											
UdpChecksumErrors																										X	X	X		X		X											
TcpChecksumErrors																										X	X	X		X		X											
Type: Data Integrity																																									
DataIntegrityFrames			X									X								X															X							
DataIntegrityErrors			X									X								X															X							
Type: Sequence Checking																																									
SequenceFrames					X								X									X															X					
SequenceErrors					X								X									X															X					
Type: Ethernet																																									
Fragments				X			X							X	X						X			X												X		X	X			
Undersize				X			X							X	X						X			X												X		X	X			

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos									StreamTrigger									ModeChecksum Errors									ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Oversize				X			X							X	X						X			X						X						X			X	X				
VlanTaggedFramesRx				X			X							X	X						X			X						X						X			X	X				
FlowControlFrames				X			X							X	X						X			X						X						X			X	X				
Type: Gigabit																																													
SymbolErrorFrames				X																	X									X						X								
SynchErrorFrames				X																	X									X						X								
Type: 10/100 + Gigabit																																													
SymbolErrors				X																	X									X						X								
OversizeAndCrcErrors				X			X							X	X						X			X						X						X			X	X				
Type: POS																																													
SectionLossOfSignal						X																X									X												X	
SectionLossOfFrame																																												X	
SectionBip																																												X	
LineAis																																												X	
LineRdi																																												X	
LineRei																																												X	
LineBip																																												X	
PathAis																																												X	
PathRdi																																												X	
PathRei																																												X	

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PathBip																																									X	
PathLossOfPointer																																									X	
PathPlm																																									X	
SectionBipErroredSecs																X																X									X	
SectionBipSeverlyErrored Secs																X																X									X	
SectionLossOfSignalSecs																X																X									X	
LineBipErroredSecs																X																X									X	
LineReiErroredSecs																X																X									X	
LineAisAlarmSecs																X																X									X	
LineRdiUnavailableSecs																X																X									X	
PathBipErroredSecs																X																X									X	
PathReiErroredSecs																X																X									X	
PathAisAlarmSecs																X																X									X	
PathAisUnavailableSecs																X																X									X	
PathRdiUnavailableSecs																X																X									X	
InputSignalStrength							X	X						X	X									X	X													X	X	X			
PosK1Byte	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		
PosK2Byte	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		
SrpDataFramesReceived	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
SrpDiscoveryFrames Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
SrpIpsFramesReceived	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
SrpParityErrors	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
SrpUsageFramesReceived	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
SrpUsageStatus	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
SrpUsageTimeouts	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
Type: DCC																																											
DccBytesReceived								X								X									X							X										
DccBytesSent																																											
DccCrcErrorsReceived								X								X									X							X										
DccFramesReceived								X								X									X							X										
DccFramesSent																																											
DccFramingErrors Received																																											
Type: BERT																																											
BertStatus						X																	X									X										
BertBitsSent						X																	X									X										
BertBitsReceived						X																	X									X										
BertBitErrorsSent						X																	X									X										
BertBitErrorsReceived						X																	X									X										

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
BertErroredBlocks						X																X								X											
BertErroredSeconds						X																X								X											
BertSeverelyErrored Seconds						X																X								X											
BertErrorFreeSeconds						X																X								X											
BertAvailableSeconds						X																X								X											
BertUnavailableSeconds						X																X								X											
BertBlockErrorState						X																X								X											
BertBackgroundBlock Errors						X																X								X											
BertBitErrorRatio						X																X								X											
BertErroredSecondRatio						X																X								X											
BertSeverlyErrored SecondRatio						X																X								X											
BertBackgroundBlockError Ratio						X																X								X											
BertNumberMismatched Ones						X																X								X											
BertMismatchedOnesRatio						X																X								X											
BertNumberMismatched Zeros						X																X								X											
BertMismatchedZerosRatio						X																X								X											

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
BertElapsedTestTime						X																	X									X										
BertUnframedOutputSignal Strength																																											
BertUnframedDetectedLine Rate																																											
BertDeskewPatternLock																																											
BertRxDeskewErrored Frames																																											
BertRxDeskewErrorFree Frames																																											
BertRxDeskewLossOf Frame																																											
BertTimeSinceLastError																																											
BertTriggerCount																																											
BertTxDeskewBitErrors																																											
BertTxDeskewErrored Frames																																											
BertTxDeskewErrorFree Frames																																											
Type: Service Disruption																																											
BertLastServiceDisruption Time						X																	X									X										

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
BertMinServiceDisruption Time						X																	X									X										
BertMaxServiceDisruption Time						X																	X									X										
BertServiceDisruption Cumulative						X																	X									X										
Type: OC192 - Temperature																																										
DMATemperature																																										X
CaptureTemperature																																										X
LatencyTemperature																																										X
BackgroundTemperature																																										X
OverlayTemperature																																										X
FrontEndTemperature																																										X
SchedulerTemperature																																										
PlmDevice1Internal Temperature																																										
PlmDevice2Internal Temperature																																										
PlmDevice3Internal Temperature																																										
FobPort1FpgaTemperature																																										

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
FobPort2FpgaTemperature																																										
FobBoardTemperature																																										
FobDevice1Internal Temperature																																										
Type: 10 Gig																																										
PauseAcknowledge							X							X	X								X															X	X				
PauseEndFrames							X							X	X								X															X	X				
PauseOverwrite							X							X	X								X															X	X				
10GigLanTxFpga Temperature																																											
10GigLanRxFpga Temperature																																											
CodingErrorFrames Received																																											
EErrorCharacterFrames Received																																											
DroppedFrames																																											
Type: Link Fault Signaling																																										
LinkFaultState							X								X								X																X				
LocalFaults							X								X								X																X				
RemoteFaults							X								X								X																X				

Table B-17. Statistics for 2.5G MSM POS modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: RPR																																									
RprDiscoveryFrames Received								X																	X																X		
RprDataFramesReceived								X																	X																X		
RprFairnessFrames Received								X																	X																X		
RprFairnessFramesSent								X																	X																X		
RprFairnessTimeouts								X																	X																X		
RprHeaderCrcErrors								X																	X																X		
RprOamFramesReceived								X																	X																X		
RprPayloadCrcErrors								X																	X																X		
RprProtectionFrames Received								X																	X																X		

Table B-18. Statistics for OC192c Modules with BERT

	Normal										Qos								StreamTrigger									ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: User Configurable																																												
UserDefinedStat1	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
UserDefinedStat2	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X		X	X	X	X			X	X	X	X	X	X	X	X	X	
CaptureTrigger	X		X																X		X							X					X	X	X	X							X		
CaptureFilter	X		X																X		X														X	X							X		
StreamTrigger1																			X	X				X	X	X	X	X																	
StreamTrigger2																			X	X				X	X	X	X	X																	
Type: States																																												
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
DuplexMode			X		X								X								X		X								X								X						
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Common																																												
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BytesReceived	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Table B-18. Statistics for OC192c Modules with BERT

	Normal										Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsReceived	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PortCpuStatus	X	X		X		X			X	X	X	X	X	X			X	X	X	X		X		X			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PortCpuDodStatus	X	X		X		X			X	X	X	X	X	X			X	X	X	X		X		X			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Transmit Duration																																											
TransmitDuration	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Quality of Service																																											
QualityOfService0											X	X	X	X	X	X	X	X																										
Type: Checksum Stats																																											
IpPackets																													X					X	X	X								
UdpPackets																													X					X	X	X								
TcpPackets																													X					X	X	X								
IpChecksumErrors																													X					X	X	X								
UdpChecksumErrors																													X					X	X	X								
TcpChecksumErrors																													X					X	X	X								
Type: Data Integrity																																											
DataIntegrityFrames				X																		X								X														
DataIntegrityErrors				X																		X								X														
Type: Sequence Checking																																											

Table B-18. Statistics for OC192c Modules with BERT

	Normal										Qos										StreamTrigger										ModeChecksum Errors										ModeDataIntegrity										Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
SequenceFrames						X								X										X								X								X							
SequenceErrors						X								X										X								X								X							
Type: Ethernet																																																
Fragments			X		X								X								X		X								X								X							
Undersize			X		X								X								X		X								X								X							
Oversize			X		X								X								X		X								X								X							
VlanTaggedFramesRx			X		X																X		X								X								X							
FlowControlFrames			X		X								X								X		X								X								X							
Type: 10/100																																																
AlignmentErrors			X																		X																											
DribbleErrors			X										X								X																											
Collisions			X										X								X																											
LateCollisions			X										X								X																											
CollisionFrames			X										X								X																											
ExcessiveCollisionFrames			X										X								X																											
Type: Gigabit																																																
SymbolErrorFrames					X																		X								X								X							
SynchErrorFrames					X																		X								X								X							
Type: 10/100 + Gigabit																																															
SymbolErrors					X																		X								X								X							

Table B-18. Statistics for OC192c Modules with BERT

	Normal										Qos										StreamTrigger										ModeChecksum Errors										ModeDataIntegrity										Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
OversizeAndCrcErrors					X								X										X								X					X										
Type: POS																																															
SectionLossOfSignal																																														X	
SectionLossOfFrame																																													X	
SectionBip																																													X	
LineAis																																													X	
LineRdi																																													X	
LineRei																																													X	
LineBip																																													X	
PathAis																																													X	
PathRdi																																													X	
PathRei																																													X	
PathBip																																													X	
PathLossOfPointer																																													X	
PathPlm																																													X	
SectionBipErroredSecs									X								X										X					X	X	X		X	X	X							X		
SectionBipSeverlyErrored Secs									X								X										X					X	X	X		X	X	X							X		
SectionLossOfSignalSecs									X								X										X					X	X	X		X	X	X							X		
LineBipErroredSecs									X								X										X					X	X	X		X	X	X							X		
LineReiErroredSecs									X								X										X					X	X	X		X	X	X							X		

Table B-18. Statistics for OC192c Modules with BERT

	Normal										Qos										StreamTrigger										ModeChecksum Errors										ModeDataIntegrity										Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
LineAisAlarmSecs									X								X										X		X	X	X		X	X	X								X			
LineRdiUnavailableSecs									X								X										X		X	X	X		X	X	X								X			
PathBipErroredSecs									X								X										X		X	X	X		X	X	X								X			
PathReiErroredSecs									X								X										X		X	X	X		X	X	X								X			
PathAisAlarmSecs									X								X										X		X	X	X		X	X	X								X			
PathAisUnavailableSecs									X								X										X		X	X	X		X	X	X								X			
PathRdiUnavailableSecs									X								X										X		X	X	X		X	X	X								X			
InputSignalStrength	X	X		X		X	X	X		X	X	X		X	X	X		X	X	X		X		X	X	X		X									X	X	X		X	X	X		X		
PosK1Byte																																																
PosK2Byte																																																
SrpDataFramesReceived																																																
SrpDiscoveryFrames Received																																																
SrpIpsFramesReceived																																																
SrpParityErrors																																																
SrpUsageFramesReceived																																																
SrpUsageStatus																																																
SrpUsageTimeouts																																																
Type: DCC																																																
DccBytesReceived									X								X										X								X									X			

Table B-18. Statistics for OC192c Modules with BERT

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
DccBytesSent																																										
DccCrcErrorsReceived									X								X										X							X								X	
DccFramesReceived									X								X										X							X								X	
DccFramesSent																																											
DccFramingErrors Received																																											
Type: OC192 - Temperature																																											
DMATemperature																																										X
CaptureTemperature																																										X
LatencyTemperature																																										X
BackgroundTemperature																																										
OverlayTemperature																																										X
FrontEndTemperature																																										X
SchedulerTemperature																																										X
PlmDevice1Internal Temperature																																										X
PlmDevice2Internal Temperature																																										X
PlmDevice3Internal Temperature																																										X
FobPort1FpgaTemperature																																										X

Notes

Table B-18. Statistics for OC192c Modules with BERT

	Normal										Qos										StreamTrigger										ModeChecksum Errors										ModeDataIntegrity										Add'l	
	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxTcpRoundTrip	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
FobPort2FpgaTemperature																																															
FobBoardTemperature																																															X
FobDevice1Internal Temperature																																														X

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: User Configurable																																				
UserDefinedStat1	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X	X	X		

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
CaptureTrigger	X												X								X					X	X						X			
CaptureFilter	X												X								X						X						X			
StreamTrigger1													X	X			X	X	X	X																
StreamTrigger2													X	X			X	X	X	X																
Type: States																																				
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X												X								X						X						
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																				
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsReceived	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X	X		X		X	X	X	X	X	X	X	X	X		X		X	X	X	X	X		X	X	X	X	X		X		X	X		

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PortCpuDodStatus	X	X	X		X		X	X	X	X	X	X	X	X	X		X		X	X	X	X	X		X	X	X	X	X		X		X	X		
Type: Transmit Duration																																				
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																																				
QualityOfService0									X	X	X	X																								
Type: Checksum Stats																																				
IpPackets																					X					X										
UdpPackets																					X					X										
TcpPackets																					X					X										
IpChecksumErrors																					X					X										
UdpChecksumErrors																					X					X										
TcpChecksumErrors																					X					X										
Type: Data Integrity																																				
DataIntegrityFrames			X												X								X						X							
DataIntegrityErrors			X												X								X						X							
Type: Sequence Checking																																				
SequenceFrames					X						X						X								X						X					
SequenceErrors					X						X						X								X						X					
Type: Ethernet																																				

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Fragments				X												X								X						X						
Undersize				X												X								X						X						
Oversize				X												X								X						X						
VlanTaggedFramesRx				X												X								X						X						
FlowControlFrames				X												X								X						X						
Type: Gigabit																																				
SymbolErrorFrames				X												X								X						X						
SynchErrorFrames				X												X								X						X						
Type: 10/100 + Gigabit																																				
SymbolErrors				X												X								X						X						
OversizeAndCrcErrors				X												X								X						X						
Type: POS																																				
SectionLossOfSignal																																			X	
SectionLossOfFrame																																			X	
SectionBip																																			X	
LineAis																																			X	
LineRdi																																			X	
LineRei																																			X	
LineBip																																			X	
PathAis																																			X	

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PathRdi																																			X	
PathRei																																			X	
PathBip																																			X	
PathLossOfPointer																																			X	
PathPlm																																			X	
SectionBipErroredSecs									X	X	X	X									X	X	X		X	X										
SectionBipSeverlyErrored Secs									X	X	X	X									X	X	X		X	X										
SectionLossOfSignalSecs									X	X	X	X									X	X	X		X	X										
LineBipErroredSecs									X	X	X	X									X	X	X		X	X										
LineReiErroredSecs									X	X	X	X									X	X	X		X	X										
LineAisAlarmSecs									X	X	X	X									X	X	X		X	X										
LineRdiUnavailableSecs									X	X	X	X									X	X	X		X	X										
PathBipErroredSecs									X	X	X	X									X	X	X		X	X										
PathReiErroredSecs									X	X	X	X									X	X	X		X	X										
PathAisAlarmSecs									X	X	X	X									X	X	X		X	X										
PathAisUnavailableSecs									X	X	X	X									X	X	X		X	X										
PathRdiUnavailableSecs									X	X	X	X									X	X	X		X	X										
InputSignalStrength	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
PosK1Byte	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PosK2Byte	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpDataFramesReceived	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpDiscoveryFrames Received	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpIpsFramesReceived	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpParityErrors	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpUsageFramesReceived	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpUsageStatus	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
SrpUsageTimeouts	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
Type: DCC																																				
DccBytesReceived						X	X					X						X	X							X						X	X			
DccBytesSent																																				
DccCrcErrorsReceived						X	X					X						X	X							X						X	X			
DccFramesReceived						X	X					X						X	X							X						X	X			
DccFramesSent																																				
DccFramingErrors Received																																				
Type: OC192 - Temperature																																				
DMATemperature																																				X
CaptureTemperature																																				X

Table B-19. Statistics for OC192c Modules with SRP and DCC

	Normal								Qos				StreamTrigger								ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
LatencyTemperature																																		X
BackgroundTemperature																																		
OverlayTemperature																																		X
FrontEndTemperature																																		X
SchedulerTemperature																																		X
PlmDevice1Internal Temperature																																		X
PlmDevice2Internal Temperature																																		X
PlmDevice3Internal Temperature																																		X
FobPort1FpgaTemperature																																		X
FobPort2FpgaTemperature																																		
FobBoardTemperature																																		X
FobDevice1Internal Temperature																																		X

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: User Configurable																																		
UserDefinedStat1	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X	X	X	
CaptureTrigger	X												X								X					X	X					X		
CaptureFilter	X												X								X						X					X		
StreamTrigger1													X	X			X	X	X	X														
StreamTrigger2													X	X			X	X	X	X														
Type: States																																		
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X												X								X						X				
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																		
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsReceived	X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PortCpuStatus	X	X	X		X		X	X	X	X	X	X	X	X	X		X		X	X	X	X	X		X	X	X	X	X		X		X	X	
PortCpuDodStatus	X	X	X		X		X	X	X	X	X	X	X	X	X		X		X	X	X	X	X		X	X	X	X	X		X		X	X	
Type: Transmit Duration																																			
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Quality of Service																																		
QualityOfService0									X	X	X	X																						
Type: Checksum Stats																																		
IpPackets																					X					X								
UdpPackets																					X					X								
TcpPackets																					X					X								
IpChecksumErrors																					X					X								
UdpChecksumErrors																					X					X								
TcpChecksumErrors																					X					X								
Type: Data Integrity																																		
DataIntegrityFrames			X												X								X						X					
DataIntegrityErrors			X												X								X						X					

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: Sequence Checking																																		
SequenceFrames					X						X						X								X									
SequenceErrors					X						X						X								X									
Type: Ethernet																																		
Fragments				X												X								X						X				
Undersize				X												X								X						X				
Oversize				X												X								X						X				
VlanTaggedFramesRx				X												X								X						X				
FlowControlFrames				X												X								X						X				
Type: Gigabit																																		
SymbolErrorFrames				X												X								X						X				
SynchErrorFrames				X												X								X						X				
Type: 10/100 + Gigabit																																		
SymbolErrors				X												X								X						X				
OversizeAndCrcErrors				X												X								X						X				
Type: POS																																		
SectionLossOfSignal																																	X	
SectionLossOfFrame																																	X	
SectionBip																																	X	
LineAis																																	X	

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
LineRdi																																		X	
LineRei																																		X	
LineBip																																		X	
PathAis																																		X	
PathRdi																																		X	
PathRei																																		X	
PathBip																																		X	
PathLossOfPointer																																		X	
PathPlm																																		X	
SectionBipErroredSecs									X	X	X	X									X	X	X		X	X									
SectionBipSeverlyErrored Secs									X	X	X	X									X	X	X		X	X									
SectionLossOfSignalSecs									X	X	X	X									X	X	X		X	X									
LineBipErroredSecs									X	X	X	X									X	X	X		X	X									
LineReiErroredSecs									X	X	X	X									X	X	X		X	X									
LineAisAlarmSecs									X	X	X	X									X	X	X		X	X									
LineRdiUnavailableSecs									X	X	X	X									X	X	X		X	X									
PathBipErroredSecs									X	X	X	X									X	X	X		X	X									
PathReiErroredSecs									X	X	X	X									X	X	X		X	X									
PathAisAlarmSecs									X	X	X	X									X	X	X		X	X									

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PathAisUnavailableSecs									X	X	X	X									X	X	X		X	X										
PathRdiUnavailableSecs									X	X	X	X									X	X	X		X	X										
InputSignalStrength	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
PosK1Byte																																				
PosK2Byte																																				
SrpDataFramesReceived																																				
SrpDiscoveryFrames Received																																				
SrpIpsFramesReceived																																				
SrpParityErrors																																				
SrpUsageFramesReceived																																				
SrpUsageStatus																																				
SrpUsageTimeouts																																				
Type: DCC																																				
DccBytesReceived						X	X					X						X	X							X						X	X			
DccBytesSent																																				
DccCrcErrorsReceived						X	X					X						X	X							X						X	X			
DccFramesReceived						X	X					X						X	X							X						X	X			
DccFramesSent																																				
DccFramingErrors Received																																				

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: OC192 - Temperature																																		
DMATemperature																																		X
CaptureTemperature																																		X
LatencyTemperature																																		X
BackgroundTemperature																																		
OverlayTemperature																																		X
FrontEndTemperature																																		X
SchedulerTemperature																																		X
PlmDevice1Internal Temperature																																		X
PlmDevice2Internal Temperature																																		X
PlmDevice3Internal| Temperature																																		X
FobPort1FpgaTemperature																																		X
FobPort2FpgaTemperature																																		
FobBoardTemperature																																		X
FobDevice1Internal Temperature																																		X
Type: RPR																																		

Table B-20. Statistics for OC192c Modules with RPR and DCC

	Normal								Qos				StreamTrigger								ModeChecksum Errors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
RprDiscoveryFrames Received	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprDataFramesReceived	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprFairnessFrames Received	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprFairnessFramesSent	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprFairnessTimeouts	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprHeaderCrcErrors	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprOamFramesReceived	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprPayloadCrcErrors	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		
RprProtectionFrames Received	X	X	X		X	X	X	X					X	X	X		X	X	X	X							X	X	X		X	X	X	X		

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: User Configurable																																								
UserDefinedStat1	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X	X	X	X
CaptureTrigger	X																X									X					X	X							X		
CaptureFilter	X																X									X					X	X							X		
StreamTrigger1																	X	X			X	X	X	X	X																
StreamTrigger2																	X	X			X	X	X	X	X																
Type: States																																								
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DuplexMode				X																X									X											
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Type: Common																																								
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BytesReceived	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsReceived	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PortCpuStatus	X	X	X		X			X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X	X	X	X	X	X	X			X	X	
PortCpuDodStatus	X	X	X		X			X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X	X	X	X	X	X	X			X	X	
Type: Transmit Duration																																								
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Quality of Service																																								
QualityOfService0										X	X	X	X	X	X	X																									
Type: Checksum Stats																																								
IpPackets																									X					X											
UdpPackets																									X					X											
TcpPackets																									X					X											
IpChecksumErrors																									X					X											
UdpChecksumErrors																									X					X											
TcpChecksumErrors																									X					X											
Type: Data Integrity																																								
DataIntegrityFrames			X																X								X													
DataIntegrityErrors			X																X								X													
Type: Sequence Checking																																								

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors					ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
SequenceFrames					X							X									X									X									
SequenceErrors					X							X									X									X									
Type: Ethernet																																							
Fragments	X	X		X	X	X	X		X	X	X	X	X	X		X	X	X		X	X	X	X		X				X			X	X		X	X	X	X		X	
Undersize	X	X		X	X	X	X		X	X	X	X	X	X		X	X	X		X	X	X	X		X				X			X	X		X	X	X	X		X	
Oversize	X	X		X	X	X	X		X	X	X	X	X	X		X	X	X		X	X	X	X		X				X			X	X		X	X	X	X		X	
VlanTaggedFramesRx	X	X		X	X	X	X		X	X	X	X	X	X		X	X	X		X	X	X	X		X				X			X	X		X	X	X	X		X	
FlowControlFrames	X	X		X	X	X	X		X	X	X	X	X	X		X	X	X		X	X	X	X		X				X			X	X		X	X	X	X		X	
Type: Gigabit																																							
SymbolErrorFrames				X															X									X						X						
SynchErrorFrames				X															X									X						X						
Type: 10/100 + Gigabit																																							
SymbolErrors				X															X									X						X						
OversizeAndCrcErrors	X	X		X	X	X	X		X	X	X	X	X	X		X	X	X		X	X	X	X		X				X			X	X		X	X	X	X		X	
Type: POS																																							
SectionLossOfSignal																																						X	
SectionLossOfFrame																																						X	
SectionBip																																						X	
LineAis																																						X	
LineRdi																																						X	

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
LineRei																																							X	
LineBip																																							X	
PathAis																																							X	
PathRdi																																							X	
PathRei																																							X	
PathBip																																							X	
PathLossOfPointer																																							X	
PathPlm																																							X	
SectionBipErroredSecs															X											X	X	X		X	X										
SectionBipSeverlyErroredSecs															X											X	X	X		X	X										
SectionLossOfSignalSecs															X											X	X	X		X	X										
LineBipErroredSecs															X											X	X	X		X	X										
LineReiErroredSecs															X											X	X	X		X	X										
LineAisAlarmSecs															X											X	X	X		X	X										
LineRdiUnavailableSecs															X											X	X	X		X	X										
PathBipErroredSecs															X											X	X	X		X	X										
PathReiErroredSecs															X											X	X	X		X	X										
PathAisAlarmSecs															X											X	X	X		X	X										
PathAisUnavailableSecs															X											X	X	X		X	X										
PathRdiUnavailableSecs															X											X	X	X		X	X										

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
InputSignalStrength	X	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X							X	X	X		X	X	X	X	X	
PosK1Byte			X					X											X					X									X						X		
PosK2Byte			X					X											X					X									X						X		
SrpDataFramesReceived			X					X											X					X									X						X		
SrpDiscoveryFrames Received			X					X											X					X									X						X		
SrpIpsFramesReceived			X					X											X					X									X						X		
SrpParityErrors			X					X											X					X									X						X		
SrpUsageFramesReceived			X					X											X					X									X						X		
SrpUsageStatus			X					X											X					X									X						X		
SrpUsageTimeouts			X					X											X					X									X						X		
Type: DCC																																									
DccBytesReceived								X							X									X							X								X		
DccBytesSent																																									
DccCrcErrorsReceived								X							X									X							X								X		
DccFramesReceived								X							X									X							X								X		
DccFramesSent																																									
DccFramingErrors Received																																									
Type: OC192 - Temperature																																									

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
DMATemperature																																								X
CaptureTemperature																																								X
LatencyTemperature																																								X
BackgroundTemperature																																								
OverlayTemperature																																								X
FrontEndTemperature																																								X
SchedulerTemperature																																								X
PlmDevice1Internal Temperature																																								X
PlmDevice2Internal Temperature																																								X
PlmDevice3Internal Temperature																																								X
FobPort1FpgaTemperature																																								X
FobPort2FpgaTemperature																																								
FobBoardTemperature																																								X
FobDevice1Internal Temperature																																								X
Type: 10 Gig																																								
PauseAcknowledge	X	X			X	X	X		X	X	X	X	X	X		X	X	X			X	X	X		X							X	X			X	X	X		X		
PauseEndFrames	X	X			X	X	X		X	X	X	X	X	X		X	X	X			X	X	X		X							X	X			X	X	X		X		
PauseOverwrite	X	X			X	X	X		X	X	X	X	X	X		X	X	X			X	X	X		X							X	X			X	X	X		X		

Table B-21. Statistics for 10GE Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
10GigLanTxFpga Temperature																																								
10GigLanRxFpga Temperature																																								
CodingErrorFrames Received																																								
EErrorCharacterFrames Received																																								
DroppedFrames																																								
Type: Link Fault Signaling																																								
LinkFaultState	X	X			X		X		X	X	X	X		X		X	X	X			X		X		X							X	X			X		X		X		
LocalFaults	X	X			X		X		X	X	X	X		X		X	X	X			X		X		X							X	X			X		X		X		
RemoteFaults	X	X			X		X		X	X	X	X		X		X	X	X			X		X		X							X	X			X		X		X		

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger									ModeCheck sumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: User Configurable																																							
UserDefinedStat1	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X	X	X	
CaptureTrigger	X																X								X						X	X								
CaptureFilter	X																X								X							X								
StreamTrigger1																	X	X			X	X	X	X	X															
StreamTrigger2																	X	X			X	X	X	X	X															
Type: States																																							
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X																X									X											
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																							
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger								ModeCheck sumErrors					ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsReceived	X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PortCpuStatus	X	X	X		X			X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X	X	X	X		X			X	X	
PortCpuDodStatus	X	X	X		X			X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X	X	X	X		X			X	X	
Type: Transmit Duration																																								
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Quality of Service																																								
QualityOfService0										X	X	X	X	X	X	X																									
Type: Checksum Stats																																								
IpPackets																									X					X										
UdpPackets																									X					X										
TcpPackets																									X					X										
IpChecksumErrors																									X					X										
UdpChecksumErrors																									X					X										
TcpChecksumErrors																									X					X										
Type: Data Integrity																																								
DataIntegrityFrames			X																X								X												
DataIntegrityErrors			X																X								X												

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors									ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: Sequence Checking																																										
SequenceFrames					X							X									X									X						X						
SequenceErrors					X							X									X									X						X						
Type: Ethernet																																										
Fragments				X		X	X			X	X	X	X	X		X				X		X	X						X						X		X	X				
Undersize				X		X	X			X	X	X	X	X		X				X		X	X						X						X		X	X				
Oversize				X		X	X			X	X	X	X	X		X				X		X	X						X						X		X	X				
VlanTaggedFramesRx				X		X	X			X	X	X	X	X		X				X		X	X						X						X		X	X				
FlowControlFrames				X		X	X			X	X	X	X	X		X				X		X	X						X						X		X	X				
Type: Gigabit																																										
SymbolErrorFrames				X																X									X						X						
SynchErrorFrames				X																X									X						X						
Type: 10/100 + Gigabit																																										
SymbolErrors				X																X									X						X						
OversizeAndCrcErrors				X		X	X			X	X	X	X	X		X				X		X	X						X						X		X	X				
Type: POS																																										
SectionLossOfSignal																																									X	
SectionLossOfFrame																																									X	
SectionBip																																									X	
LineAis																																									X	

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger									ModeCheck sumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
LineRdi																																							X	
LineRei																																							X	
LineBip																																							X	
PathAis																																							X	
PathRdi																																							X	
PathRei																																							X	
PathBip																																							X	
PathLossOfPointer																																							X	
PathPlm																																							X	
SectionBipErroredSecs															X											X	X	X		X	X										
SectionBipSeverlyErrored Secs															X											X	X	X		X	X										
SectionLossOfSignalSecs															X											X	X	X		X	X										
LineBipErroredSecs															X											X	X	X		X	X										
LineReiErroredSecs															X											X	X	X		X	X										
LineAisAlarmSecs															X											X	X	X		X	X										
LineRdiUnavailableSecs															X											X	X	X		X	X										
PathBipErroredSecs															X											X	X	X		X	X										
PathReiErroredSecs															X											X	X	X		X	X										
PathAisAlarmSecs															X											X	X	X		X	X										

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger									ModeCheck sumErrors						ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PathAisUnavailableSecs															X											X	X	X		X	X										
PathRdiUnavailableSecs															X											X	X	X		X	X										
InputSignalStrength	X	X	X		X	X	X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X							X	X	X		X	X	X	X	X		
PosK1Byte																																									
PosK2Byte																																									
SrpDataFramesReceived																																									
SrpDiscoveryFrames Received																																									
SrpIpsFramesReceived																																									
SrpParityErrors																																									
SrpUsageFramesReceived																																									
SrpUsageStatus																																									
SrpUsageTimeouts																																									
Type: DCC																																									
DccBytesReceived								X							X								X							X									X			
DccBytesSent																																									
DccCrcErrorsReceived								X							X								X							X									X			
DccFramesReceived								X							X								X							X									X			
DccFramesSent																																									
DccFramingErrors Received																																									

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger									ModeChecksumErrors									ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
Type: OC192 - Temperature																																											
DMATemperature																																											X
CaptureTemperature																																											X
LatencyTemperature																																											X
BackgroundTemperature																																											
OverlayTemperature																																											X
FrontEndTemperature																																											X
SchedulerTemperature																																											X
PlmDevice1Internal Temperature																																											X
PlmDevice2Internal Temperature																																											X
PlmDevice3Internal Temperature																																											X
FobPort1FpgaTemperature																																											X
FobPort2FpgaTemperature																																											
FobBoardTemperature																																											X
FobDevice1Internal Temperature																																											X
Type: 10 Gig																																											
PauseAcknowledge						X	X			X	X	X	X	X		X						X	X														X	X				

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos										StreamTrigger										ModeChecksumErrors										ModeDataIntegrity										Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PauseEndFrames						X	X			X	X	X	X	X		X							X	X													X	X				
PauseOverwrite						X	X			X	X	X	X	X		X							X	X													X	X				
10GigLanTxFpga Temperature																																												
10GigLanRxFpga Temperature																																												
CodingErrorFrames Received																																												
EErrorCharacterFrames Received																																												
DroppedFrames																																												
Type: Link Fault Signaling																																												
LinkFaultState							X			X	X	X		X		X							X															X					
LocalFaults							X			X	X	X		X		X							X															X					
RemoteFaults							X			X	X	X		X		X							X															X					
Type: RPR																																												
RprDiscoveryFrames Received	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X			
RprDataFramesReceived	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X			
RprFairnessFrames Received	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X			

Table B-22. Statistics for 10G UNIPHY Modules with BERT

	Normal									Qos							StreamTrigger								ModeCheck sumErrors						ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
RprFairnessFramesSent	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X		
RprFairnessTimeouts	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X		
RprHeaderCrcErrors	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X		
RprOamFramesReceived	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X		
RprPayloadCrcErrors	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X		
RprProtectionFrames Received	X	X	X		X			X	X								X	X	X		X			X	X							X	X	X		X			X	X		

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors					ModeDataIntegrity									Add'l	
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeDcc**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**PosExtendedStats**	**TemperatureSensorsStats**
Type: User Configurable																																								
UserDefinedStat1	X	X	X	X	X	X	X	X	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X	X	X	X	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X	X	X		
CaptureTrigger	X	X							X	X	X						X	X	X						X	X					X	X	X						X		
CaptureFilter	X	X							X	X	X						X	X	X						X	X						X	X						X		
StreamTrigger1	X	X	X		X				X	X	X	X	X				X	X	X	X		X	X	X	X	X						X	X	X		X				X		
StreamTrigger2	X	X	X		X				X	X	X	X	X				X	X	X	X		X	X	X	X	X						X	X	X		X				X		
Type: States																																								
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X																	X								X						X						
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																								
FramesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X	X	X	X	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger									ModeCheck sumErrors						ModeDataIntegrity									Add'l	
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeDcc**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**PosExtendedStats**	**TemperatureSensorsStats**
FcsErrors	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsReceived	X	X	X	X	X	X	X	X	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X	X	X	X	X		X			X	X		
PortCpuDodStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X	X	X	X	X		X			X	X		
Type: Transmit Duration																																											
TransmitDuration	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																																											
QualityOfService0										X	X	X	X	X	X	X	X																										
Type: Checksum Stats																																											
IpPackets																											X					X											
UdpPackets																											X					X											
TcpPackets																											X					X											
IpChecksumErrors																											X					X											
UdpChecksumErrors																											X					X											
TcpChecksumErrors																											X					X											
Type: Data Integrity																																											
DataIntegrityFrames			X									X								X									X						X								
DataIntegrityErrors			X									X								X									X						X								

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors					ModeDataIntegrity								Add'l	
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeDcc**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**PosExtendedStats**	**TemperatureSensorsStats**
Type: Sequence Checking																																							
SequenceFrames					X								X									X								X					X				
SequenceErrors					X								X									X								X					X				
Type: Ethernet																																							
Fragments	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				X			X	X	X	X	X	X	X		X	
Undersize	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				X			X	X	X	X	X	X	X		X	
Oversize	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				X			X	X	X	X	X	X	X		X	
VlanTaggedFramesRx	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				X			X	X	X	X	X	X	X		X	
FlowControlFrames	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				X			X	X	X	X	X	X	X		X	
Type: Gigabit																																							
SymbolErrorFrames				X																	X								X										
SynchErrorFrames				X																	X								X										
Type: 10/100 + Gigabit																																							
SymbolErrors				X																	X								X										
OversizeAndCrcErrors	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X				X			X	X	X	X	X	X	X			
Type: POS																																							
SectionLossOfSignal																																						X	
SectionLossOfFrame																																						X	
SectionBip																																						X	
LineAis																																						X	

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors						ModeDataIntegrity								Add'l	
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
LineRdi																																							X	
LineRei																																							X	
LineBip																																							X	
PathAis																																							X	
PathRdi																																							X	
PathRei																																							X	
PathBip																																							X	
PathLossOfPointer																																							X	
PathPlm																																							X	
SectionBipErroredSecs																	X									X	X	X		X	X									
SectionBipSeverlyErrored Secs																	X									X	X	X		X	X									
SectionLossOfSignalSecs																	X									X	X	X		X	X									
LineBipErroredSecs																	X									X	X	X		X	X									
LineReiErroredSecs																	X									X	X	X		X	X									
LineAisAlarmSecs																	X									X	X	X		X	X									
LineRdiUnavailableSecs																	X									X	X	X		X	X									
PathBipErroredSecs																	X									X	X	X		X	X									
PathReiErroredSecs																	X									X	X	X		X	X									
PathAisAlarmSecs																	X									X	X	X		X	X									

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors						ModeDataIntegrity								Add'l	
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
PathAisUnavailableSecs																X											X	X	X		X	X										
PathRdiUnavailableSecs																X											X	X	X		X	X										
InputSignalStrength	X	X	X		X	X	X	X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X	X							X	X	X		X	X	X	X	X	
PosK1Byte																																										
PosK2Byte																																										
SrpDataFramesReceived																																										
SrpDiscoveryFrames Received																																										
SrpIpsFramesReceived																																										
SrpParityErrors																																										
SrpUsageFramesReceived																																										
SrpUsageStatus																																										
SrpUsageTimeouts																																										
Type: DCC																																										
DccBytesReceived								X								X								X							X								X			
DccBytesSent																																										
DccCrcErrorsReceived								X								X								X							X								X			
DccFramesReceived								X								X								X							X								X			
DccFramesSent																																										
DccFramingErrors Received																																										

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors						ModeDataIntegrity								Add'l	
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeDcc**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**PosExtendedStats**	**TemperatureSensorsStats**
Type: OC192 - Temperature																																							
DMATemperature																																							X
CaptureTemperature																																							X
LatencyTemperature																																							X
BackgroundTemperature																																							X
OverlayTemperature																																							X
FrontEndTemperature																																							X
SchedulerTemperature																																							
PlmDevice1Internal Temperature																																							
PlmDevice2Internal Temperature																																							
PlmDevice3Internal Temperature																																							
FobPort1FpgaTemperature																																							
FobPort2FpgaTemperature																																							
FobBoardTemperature																																							
FobDevice1Internal Temperature																																							
Type: 10 Gig																																							
PauseAcknowledge	X	X	X		X	X	X		X	X	X	X	X	X	X		X	X	X	X		X	X	X		X						X	X	X		X	X	X		X	

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors						ModeDataIntegrity								Add'l	
Receive Mode	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeDcc**	**Capture**	**PacketGroup**	**RxDataIntegrity**	**RxFirstTimeStamp**	**RxSequenceChecking**	**RxModeBert**	**RxModeBertChannelized**	**RxModeDcc**	**RxModeWidePacketGroup**	**PosExtendedStats**	**TemperatureSensorsStats**
PauseEndFrames	X	X	X		X	X	X		X	X	X	X	X	X	X		X	X	X	X		X	X	X		X							X	X	X		X	X	X		X	
PauseOverwrite	X	X	X		X	X	X		X	X	X	X	X	X	X		X	X	X	X		X	X	X		X							X	X	X		X	X	X		X	
10GigLanTxFpga Temperature																																									
10GigLanRxFpga Temperature																																									
CodingErrorFrames Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X				X	
EErrorCharacterFrames Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X				X	
DroppedFrames	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X				X	
Type: Link Fault Signaling																																									
LinkFaultState	X	X	X		X		X		X	X	X	X	X		X		X	X	X	X		X		X		X							X	X	X		X		X		X	
LocalFaults	X	X	X		X		X		X	X	X	X	X		X		X	X	X	X		X		X		X							X	X	X		X		X		X	
RemoteFaults	X	X	X		X		X		X	X	X	X	X		X		X	X	X	X		X		X		X							X	X	X		X		X		X	
Type: RPR																																									
RprDiscoveryFrames Received								X																	X													X			
RprDataFramesReceived								X																	X													X			
RprFairnessFrames Received								X																	X													X			

Table B-23. Statistics for 10GE LSM Modules (except NGY)

Statistics Mode	Normal									Qos								StreamTrigger								ModeCheck sumErrors						ModeDataIntegrity								Add'l	
Receive Mode	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	TemperatureSensorsStats
RprFairnessFramesSent								X																	X														X			
RprFairnessTimeouts								X																	X														X			
RprHeaderCrcErrors								X																	X														X			
RprOamFramesReceived								X																	X														X			
RprPayloadCrcErrors								X																	X														X			
RprProtectionFrames Received								X																	X														X			
Type: Ordered Sets																																										
LocalOrderedSetsSent	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X			X		
LocalOrderedSets Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X			X		
RemoteOrderedSetsSent	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X			X		
RemoteOrderedSets Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X			X		
CustomOrderedSetsSent	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X			X		
CustomOrderedSets Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X							X	X	X		X			X		

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Type: User Configurable								
UserDefinedStat1	X	X	X	X	X	X	X	X
UserDefinedStat2	X	X	X	X	X	X	X	X
CaptureTrigger	X			X	X			X
CaptureFilter	X			X	X			X
StreamTrigger1	X	X	X	X	X	X	X	X
StreamTrigger2	X	X	X	X	X	X	X	X
Type: States								
Link	X	X	X	X	X	X	X	X
LineSpeed	X	X	X	X	X	X	X	X
DuplexMode								
TransmitState	X	X	X	X	X	X	X	X
CaptureState	X	X	X	X	X	X	X	X
PauseState	X	X	X	X	X	X	X	X
Type: Common								
FramesSent	X	X	X	X	X	X	X	X
FramesReceived	X	X	X	X	X	X	X	X
BytesSent	X	X	X	X	X	X	X	X
BytesReceived	X	X	X	X	X	X	X	X
FcsErrors	X	X	X	X	X	X	X	X

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
BitsReceived	X	X	X	X	X	X	X	X
BitsSent	X	X	X	X	X	X	X	X
PortCpuStatus	X	X	X	X	X	X	X	X
PortCpuDodStatus	X	X	X	X	X	X	X	X
Type: Transmit Duration								
TransmitDuration	X	X	X	X	X	X	X	X
Type: Quality of Service								
QualityOfService0					X	X	X	X
Type: Checksum Stats								
IPv4Packets	X	X	X	X	X	X	X	X
UdpPackets	X	X	X	X	X	X	X	X
TcpPackets	X	X	X	X	X	X	X	X
IPv4ChecksumErrors	X	X	X	X	X	X	X	X
UdpChecksumErrors	X	X	X	X	X	X	X	X
TcpChecksumErrors	X	X	X	X	X	X	X	X
Type: Data Integrity								
DataIntegrityFrames		X				X		
DataIntegrityErrors		X				X		
Type: Sequence Checking								
SequenceFrames			X				X	
SequenceErrors			X				X	

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
Type: Ethernet								
Fragments	X	X	X	X	X	X	X	X
Undersize	X	X	X	X	X	X	X	X
Oversize	X	X	X	X	X	X	X	X
VlanTaggedFramesRx	X	X	X	X	X	X	X	X
FlowControlFrames	X	X	X	X	X	X	X	X
Type: Gigabit								
SymbolErrorFrames								
SynchErrorFrames								
Type: 10/100 + Gigabit								
SymbolErrors								
OversizeAndCrcErrors	X	X	X	X	X	X	X	X
Type: POS								
SectionLossOfSignal								
SectionLossOfFrame								
SectionBip								
LineAis								
LineRdi								
LineRei								
LineBip								
PathAis								

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup
PathRdi								
PathRei								
PathBip								
PathLossOfPointer								
PathPlm								
SectionBipErroredSecs								
SectionBipSeverlyErrored Secs								
SectionLossOfSignalSecs								
LineBipErroredSecs								
LineReiErroredSecs								
LineAisAlarmSecs								
LineRdiUnavailableSecs								
PathBipErroredSecs								
PathReiErroredSecs								
PathAisAlarmSecs								
PathAisUnavailableSecs								
PathRdiUnavailableSecs								
InputSignalStrength	X	X	X	X	X	X	X	X
PosK1Byte								
PosK2Byte								

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
SrpDataFramesReceived								
SrpDiscoveryFrames Received								
SrpIpsFramesReceived								
SrpParityErrors								
SrpUsageFramesReceived								
SrpUsageStatus								
SrpUsageTimeouts								
Type: DCC								
DccBytesReceived								
DccBytesSent								
DccCrcErrorsReceived								
DccFramesReceived								
DccFramesSent								
DccFramingErrors Received								
Type: OC192 - Temperature								
DMATemperature								
CaptureTemperature								
LatencyTemperature								
BackgroundTemperature								
OverlayTemperature								

Table B-24. Statistics for NGY Modules

Statistics Mode	**Normal**				**Qos**			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
FrontEndTemperature								
SchedulerTemperature								
PlmDevice1Internal Temperature								
PlmDevice2Internal Temperature								
PlmDevice3Internal Temperature								
FobPort1FpgaTemperature								
FobPort2FpgaTemperature								
FobBoardTemperature								
FobDevice1Internal Temperature								
Type: 10 Gig								
PauseAcknowledge	X	X	X	X	X	X	X	X
PauseEndFrames	X	X	X	X	X	X	X	X
PauseOverwrite	X	X	X	X	X	X	X	X
10GigLanTxFpga Temperature								
10GigLanRxFpga Temperature								
CodingErrorFrames Received	X	X	X	X	X	X	X	X

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
EErrorCharacterFrames Received	X	X	X	X	X	X	X	X
DroppedFrames	X	X	X	X	X	X	X	X
Type: Link Fault Signaling								
LinkFaultState	X	X	X	X	X	X	X	X
LocalFaults	X	X	X	X	X	X	X	X
RemoteFaults	X	X	X	X	X	X	X	X
Type: RPR								
RprDiscoveryFrames Received								
RprDataFramesReceived								
RprFairnessFrames Received								
RprFairnessFramesSent								
RprFairnessTimeouts								
RprHeaderCrcErrors								
RprOamFramesReceived								
RprPayloadCrcErrors								
RprProtectionFrames Received								
Type: Ordered Sets								
LocalOrderedSetsSent	X	X	X	X	X	X	X	X

Table B-24. Statistics for NGY Modules

Statistics Mode	Normal				Qos			
Receive Mode	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**	**Capture**	**RxDataIntegrity**	**RxSequenceChecking**	**RxModeWidePacketGroup**
LocalOrderedSets Received	X	X	X	X	X	X	X	X
RemoteOrderedSetsSent	X	X	X	X	X	X	X	X
RemoteOrderedSets Received	X	X	X	X	X	X	X	X
CustomOrderedSetsSent	X	X	X	X	X	X	X	X
CustomOrderedSets Received	X	X	X	X	X	X	X	X

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
Type: User Configurable																																									
UserDefinedStat1	X	X	X	X	X		X	X	X	X	X	X	X				X	X	X	X	X	X		X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X		X	X	X	X	X	X	X				X	X	X	X	X	X		X	X	X				X				X	X	X	X	X	X	X	X		
CaptureTrigger	X	X							X	X	X						X	X	X						X	X							X	X							X		
CaptureFilter	X	X							X	X	X						X	X	X						X	X							X	X							X		
StreamTrigger1	X	X	X		X				X	X	X	X	X				X	X	X	X		X		X	X	X								X	X	X		X				X		
StreamTrigger2	X	X	X		X				X	X	X	X	X				X	X	X	X		X		X	X	X								X	X	X		X				X		
Type: States																																										
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X																	X										X											
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																										
FramesSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X				X				X	X	X	X	X	X	X	X		
FramesReceived	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X				X				X	X	X	X	X	X	X	X		
BytesSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X				X				X	X	X	X	X	X	X	X		
BytesReceived	X	X	X	X	X		X	X	X	X	X	X	X				X	X	X	X	X	X		X	X	X				X				X	X	X	X	X	X	X	X		

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
FcsErrors	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsReceived	X	X	X	X	X		X	X	X	X	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
BitsSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
PortCpuStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X			X	X	X	X		X		X	X	
PortCpuDodStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X			X	X	X	X		X		X	X	
Type: Transmit Duration																																											
TransmitDuration	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Type: Quality of Service																																											
QualityOfService0										X	X	X	X	X	X	X	X																											
Type: Checksum Stats																																											
IpPackets																										X	X	X		X		X												
UdpPackets																										X	X	X		X		X												
TcpPackets																										X	X	X		X		X												
IpChecksumErrors																										X	X	X		X		X												
UdpChecksumErrors																										X	X	X		X		X												
TcpChecksumErrors																										X	X	X		X		X												
Type: Data Integrity																																											
DataIntegrityFrames			X									X								X																X							
DataIntegrityErrors			X									X								X																X							

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
Type: Sequence Checking																																									
SequenceFrames					X								X									X																X			
SequenceErrors					X								X									X																X			
Type: Ethernet																																									
Fragments	X	X	X	X	X		X		X	X	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	X	X	X	X	X	X		X	
Undersize	X	X	X	X	X		X		X	X	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	X	X	X	X	X	X		X	
Oversize	X	X	X	X	X		X		X	X	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	X	X	X	X	X	X		X	
VlanTaggedFramesRx	X	X	X	X	X		X		X	X	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	X	X	X	X	X	X		X	
FlowControlFrames	X	X	X	X	X		X		X	X	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	X	X	X	X	X	X		X	
Type: Gigabit																																									
SymbolErrorFrames				X																	X									X							X					
SynchErrorFrames				X																	X									X							X					
Type: 10/100 + Gigabit																																									
SymbolErrors				X																	X									X							X					
OversizeAndCrcErrors	X	X	X	X	X		X		X	X	X	X	X	X	X		X	X	X	X	X	X		X		X				X				X	X	X	X	X	X	X		X	
Type: POS																																									
SectionLossOfSignal						X																X							X													
SectionLossOfFrame																																									
SectionBip																																									
LineAis																																									

Table B-25. Statistics for 10G MSM modules

	Normal									Qos							StreamTrigger									ModeChecksum Errors									ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc		Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
LineRdi																																												
LineRei																																												
LineBip																																												
PathAis																																												
PathRdi																																												
PathRei																																												
PathBip																																												
PathLossOfPointer																																												
PathPlm																																												
SectionBipErroredSecs																X																X												
SectionBipSeverlyErrored Secs																X																X												
SectionLossOfSignalSecs																X																X												
LineBipErroredSecs																X																X												
LineReiErroredSecs																X																X												
LineAisAlarmSecs																X																X												
LineRdiUnavailableSecs																X																X												
PathBipErroredSecs																X																X												
PathReiErroredSecs																X																X												
PathAisAlarmSecs																X																X												

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger									ModeChecksum Errors									ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
PathAisUnavailableSecs																X																	X											
PathRdiUnavailableSecs																X																	X											
InputSignalStrength	X	X	X		X		X	X	X	X	X	X	X	X	X		X	X	X	X		X		X	X	X								X	X	X		X	X	X	X	X		
PosK1Byte																																												
PosK2Byte																																												
SrpDataFramesReceived																																												
SrpDiscoveryFrames Received																																												
SrpIpsFramesReceived																																												
SrpParityErrors																																												
SrpUsageFramesReceived																																												
SrpUsageStatus																																												
SrpUsageTimeouts																																												
Type: DCC																																												
DccBytesReceived								X								X								X								X								X			
DccBytesSent																																												
DccCrcErrorsReceived								X								X								X								X								X			
DccFramesReceived								X								X								X								X								X			
DccFramesSent																																												
DccFramingErrors Received																																												

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
Type: BERT																																									
BertStatus						X																	X								X										
BertBitsSent						X																	X								X										
BertBitsReceived						X																	X								X										
BertBitErrorsSent						X																	X								X										
BertBitErrorsReceived						X																	X								X										
BertErroredBlocks						X																	X								X										
BertErroredSeconds						X																	X								X										
BertSeverelyErrored Seconds						X																	X								X										
BertErrorFreeSeconds						X																	X								X										
BertAvailableSeconds						X																	X								X										
BertUnavailableSeconds						X																	X								X										
BertBlockErrorState						X																	X								X										
BertBackgroundBlock Errors						X																	X								X										
BertBitErrorRatio						X																	X								X										
BertErroredSecondRatio						X																	X								X										
BertSeverlyErroredSecond Ratio						X																	X								X										

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
BertBackgroundBlockErrorRatio						X																	X								X										
BertNumberMismatchedOnes						X																	X								X										
BertMismatchedOnesRatio						X																	X								X										
BertNumberMismatchedZeros						X																	X								X										
BertMismatchedZerosRatio						X																	X								X										
BertElapsedTestTime						X																	X								X										
BertUnframedOutputSignalStrength																																										
BertUnframedDetectedLineRate																																										
BertDeskewPatternLock																																										
BertRxDeskewErroredFrames																																										
BertRxDeskewErrorFreeFrames																																									
BertRxDeskewLossOfFrame																																										
BertTimeSinceLastError																																										
BertTriggerCount																																										
BertTxDeskewBitErrors																																										

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
BertTxDeskewErrored Frames																																									
BertTxDeskewErrorFree Frames																																									
Type: Service Disruption																																									
BertLastServiceDisruption Time						X																X									X										
BertMinServiceDisruption Time						X																X									X										
BertMaxServiceDisruption Time						X																X									X										
BertServiceDisruption Cumulative						X																X									X										
Type: OC192 - Temperature																																									
DMATemperature																																									X	
CaptureTemperature																																									X	
LatencyTemperature																																									X	
BackgroundTemperature																																									X	
OverlayTemperature																																									X	
FrontEndTemperature																																									X	
SchedulerTemperature																																										

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
PlmDevice1Internal Temperature																																									
PlmDevice2Internal Temperature																																									
PlmDevice3Internal Temperature																																									
FobPort1FpgaTemperature																																									
FobPort2FpgaTemperature																																									
FobBoardTemperature																																									
FobDevice1Internal Temperature																																									
Type: 10 Gig																																									
PauseAcknowledge	X	X	X		X		X		X	X	X	X	X	X	X		X	X	X	X		X		X		X								X	X	X		X	X	X		X		
PauseEndFrames	X	X	X		X		X		X	X	X	X	X	X	X		X	X	X	X		X		X		X								X	X	X		X	X	X		X		
PauseOverwrite	X	X	X		X		X		X	X	X	X	X	X	X		X	X	X	X		X		X		X								X	X	X		X	X	X		X		
10GigLanTxFpga Temperature																																										
10GigLanRxFpga Temperature																																										
CodingErrorFrames Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		
EErrorCharacterFrames Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
DroppedFrames	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X	
Type: Link Fault Signaling																																										
LinkFaultState	X	X	X		X		X		X	X	X	X	X		X		X	X	X	X		X		X		X								X	X	X		X		X		X	
LocalFaults	X	X	X		X		X		X	X	X	X	X		X		X	X	X	X		X		X		X								X	X	X		X		X		X	
RemoteFaults	X	X	X		X		X		X	X	X	X	X		X		X	X	X	X		X		X		X								X	X	X		X		X		X	
Type: RPR																																										
RprDiscoveryFrames Received								X																	X																X		
RprDataFramesReceived								X																	X																X		
RprFairnessFrames Received								X																	X																X		
RprFairnessFramesSent								X																	X																X		
RprFairnessTimeouts								X																	X																X		
RprHeaderCrcErrors								X																	X																X		
RprOamFramesReceived								X																	X																X		
RprPayloadCrcErrors								X																	X																X		
RprProtectionFrames Received								X																	X																X		
Type: Ordered Sets																																										
LocalOrderedSetsSent																																										

Table B-25. Statistics for 10G MSM modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	TemperatureSensorsStats	
LocalOrderedSets Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		
RemoteOrderedSetsSent																																												
RemoteOrderedSets Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		
CustomOrderedSetsSent																																												
CustomOrderedSets Received	X	X	X		X				X	X	X	X	X				X	X	X	X		X				X								X	X	X		X				X		

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
Type: User Configurable																																										
UserDefinedStat1	X	X	X	X	X		X	X	X								X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
UserDefinedStat2	X	X	X	X	X		X	X	X								X	X	X	X	X	X		X	X	X				X			X	X	X	X	X	X	X	X		
CaptureTrigger	X								X								X	X							X	X							X	X							X		
CaptureFilter	X								X								X	X							X	X							X								X		
StreamTrigger1									X								X	X	X	X		X		X	X	X															X		
StreamTrigger2									X								X	X	X	X		X		X	X	X															X		
Type: States																																										
Link	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
LineSpeed	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
DuplexMode				X																	X									X						X						
TransmitState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CaptureState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
PauseState	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Type: Common																																										
FramesSent				X			X	X	X					X	X	X	X				X			X	X	X				X			X			X	X	X	X		
FramesReceived				X			X	X	X					X	X	X	X				X			X	X	X				X			X			X	X	X	X		
BytesSent				X			X	X	X					X	X	X	X				X			X	X	X				X			X			X	X	X	X		
BytesReceived				X			X	X	X								X				X			X	X	X				X			X			X	X	X	X		
FcsErrors	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
BitsReceived	X	X	X	X	X		X	X	X								X	X	X	X	X	X		X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X		
BitsSent	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X		
PortCpuStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X		X	X	X	X		X			X	X		
PortCpuDodStatus	X	X	X		X			X	X	X	X	X	X			X	X	X	X	X		X			X	X	X	X	X		X		X	X	X	X		X			X	X		
Type: Transmit Duration																																												
TransmitDuration	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X		
Type: Quality of Service																																												
QualityOfService0										X	X	X	X	X	X	X	X																											
Type: Checksum Stats																																												
IpPackets																										X	X	X		X		X												
UdpPackets																										X	X	X		X		X												
TcpPackets																										X	X	X		X		X												
IpChecksumErrors																										X	X	X		X		X												
UdpChecksumErrors																										X	X	X		X		X												
TcpChecksumErrors																										X	X	X		X		X												
Type: Data Integrity																																												
DataIntegrityFrames																																				X								
DataIntegrityErrors																																				X								
Type: Sequence Checking																																												
SequenceFrames					X																																X							

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
SequenceErrors					X																																X						
Type: Ethernet																																										
Fragments				X			X		X					X	X		X				X			X		X				X				X			X	X		X		
Undersize				X			X		X					X	X		X				X			X		X				X				X			X	X		X		
Oversize				X			X		X					X	X		X				X			X		X				X				X			X	X		X		
VlanTaggedFramesRx				X			X		X					X	X		X				X			X		X				X				X			X	X		X		
FlowControlFrames				X			X		X					X	X		X				X			X		X				X				X			X	X		X		
Type: Gigabit																																											
SymbolErrorFrames				X																	X									X				X								
SynchErrorFrames				X																	X									X				X								
Type: 10/100 + Gigabit																																											
SymbolErrors				X																	X									X				X								
OversizeAndCrcErrors				X			X		X					X	X		X				X			X		X				X				X			X	X		X		
Type: POS																																											
SectionLossOfSignal						X																X									X											X	
SectionLossOfFrame																																											X	
SectionBip																																											X	
LineAis																																											X	
LineRdi																																											X	
LineRei																																											X	

Table B-26. Statistics for ATM Modules

	Normal									Qos							StreamTrigger									ModeChecksum Errors									ModeDataIntegrity									Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc		Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
LineBip																																											X	
PathAis																																											X	
PathRdi																																											X	
PathRei																																											X	
PathBip																																											X	
PathLossOfPointer																																											X	
PathPlm																																											X	
SectionBipErroredSecs																X																	X										
SectionBipSeverlyErrored Secs																X																	X										
SectionLossOfSignalSecs																X																	X										
LineBipErroredSecs																X																	X										
LineReiErroredSecs																X																	X										
LineAisAlarmSecs																X																	X										
LineRdiUnavailableSecs																X																	X										
PathBipErroredSecs																X																	X										
PathReiErroredSecs																X																	X										
PathAisAlarmSecs																X																	X										
PathAisUnavailableSecs																X																	X										
PathRdiUnavailableSecs																X																	X										

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
InputSignalStrength							X	X	X						X	X		X							X	X	X												X	X	X	X		
PosK1Byte																																												
PosK2Byte																																												
SrpDataFramesReceived																																												
SrpDiscoveryFrames Received																																												
SrpIpsFramesReceived																																												
SrpParityErrors																																												
SrpUsageFramesReceived																																												
SrpUsageStatus																																												
SrpUsageTimeouts																																												
Type: DCC																																												
DccBytesReceived								X								X									X															X			
DccBytesSent																																												
DccCrcErrorsReceived								X								X									X															X			
DccFramesReceived								X								X									X															X			
DccFramesSent																																												
DccFramingErrors Received																																												
Type: BERT																																												
BertStatus						X																	X								X												

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
BertBitsSent						X																	X								X										
BertBitsReceived						X																	X								X										
BertBitErrorsSent						X																	X								X										
BertBitErrorsReceived						X																	X								X										
BertErroredBlocks						X																	X								X										
BertErroredSeconds						X																	X								X										
BertSeverelyErrored Seconds						X																	X								X										
BertErrorFreeSeconds						X																	X								X										
BertAvailableSeconds						X																	X								X										
BertUnavailableSeconds						X																	X								X										
BertBlockErrorState						X																	X								X										
BertBackgroundBlock Errors						X																	X								X										
BertBitErrorRatio						X																	X								X										
BertErroredSecondRatio						X																	X								X										
BertSeverlyErroredSecond Ratio						X																	X								X										
BertBackgroundBlockError Ratio						X																	X								X										
BertNumberMismatched Ones						X																	X								X										

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
BertMismatchedOnesRatio						X																	X								X										
BertNumberMismatched Zeros						X																	X								X										
BertMismatchedZerosRatio						X																	X								X										
BertElapsedTestTime						X																	X								X										
BertUnframedOutputSignal Strength																																										
BertUnframedDetectedLine Rate																																										
BertDeskewPatternLock																																										
BertRxDeskewErrored Frames																																										
BertRxDeskewErrorFree Frames																																										
BertRxDeskewLossOf Frame																																										
BertTimeSinceLastError																																										
BertTriggerCount																																										
BertTxDeskewBitErrors																																										
BertTxDeskewErrored Frames																																										

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
BertTxDeskewErrorFree Frames																																											
Type: Service Disruption																																											
BertLastService DisruptionTime						X																X									X												
BertMinServiceDisruption Time						X																X									X												
BertMaxServiceDisruption Time						X																X									X												
BertServiceDisruption Cumulative						X																X									X												
Type: 10 Gig																																											
PauseAcknowledge							X		X					X	X		X						X		X														X	X		X		
PauseEndFrames							X		X					X	X		X						X		X														X	X		X		
PauseOverwrite							X		X					X	X		X						X		X														X	X		X		
10GigLanTxFpga Temperature																																											
10GigLanRxFpga Temperature																																											
CodingErrorFrames Received									X								X								X																X		
EErrorCharacterFrames Received									X								X								X																X		

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors							ModeDataIntegrity							Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
DroppedFrames									X								X								X															X		
Type: ATM																																									
AtmAal5BytesReceived	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmAal5BytesSent	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmAal5CrcErrorFrames																																									
AtmAal5FramesReceived	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmAal5FramesSent	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmAal5LengthError Frames																																									
AtmAal5TimeoutError Frames																																									
AtmCellsReceived	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmCellsSent	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmCorrectedHcsError Count	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmIdleCellCount	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmScheduledCellsSent	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmUncorrectedHcsError Count	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
AtmUnregisteredCells Received	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				
EthernetCrc	X	X	X		X					X	X	X	X					X	X	X		X					X	X	X		X			X	X	X		X				

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
Type: Link Fault Signaling																																									
LinkFaultState							X		X						X		X							X		X													X		X		
LocalFaults							X		X						X		X							X		X													X		X		
RemoteFaults							X		X						X		X							X		X													X		X		
Type: RPR																																										
RprDiscoveryFrames Received								X																	X																X			
RprDataFramesReceived								X																	X																X			
RprFairnessFrames Received								X																	X																X			
RprFairnessFramesSent								X																	X																X			
RprFairnessTimeouts								X																	X																X			
RprHeaderCrcErrors								X																	X																X			
RprOamFramesReceived								X																	X																X			
RprPayloadCrcErrors								X																	X																X			
RprProtectionFrames Received								X																	X																X			
Type: Ordered Sets																																												
LocalOrderedSetsSent									X								X									X																X		
LocalOrderedSets Received									X								X									X																X		

Table B-26. Statistics for ATM Modules

	Normal									Qos								StreamTrigger								ModeChecksum Errors								ModeDataIntegrity								Add'l	
	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeDcc	Capture	PacketGroup	RxDataIntegrity	RxFirstTimeStamp	RxSequenceChecking	RxModeBert	RxModeBertChannelized	RxModeDcc	RxModeWidePacketGroup	PosExtendedStats	
RemoteOrderedSetsSent									X								X									X															X		
RemoteOrderedSets Received									X								X									X															X		
CustomOrderedSetsSent									X								X									X															X		
CustomOrderedSets Received									X								X									X															X		

Table B-27. Statistics for PoE Modules

	Single Mode
Type: PoE	
PoeStatus	X
PoeInputVoltage	X
PoeInputCurrent	X
PoeInputPower	X
PoeActiveInput	X
PoeTemperature	X
PoeAutocalibration	X

Table B-28. Statistics for 10/100/1000 AFM

	Single Mode
Type: AFM	
bytesFromApplication	X
packetsFromApplication	X
monitorBytesFromPort2	X
monitorBytesFromPort3	X
monitorPacketsFromPort2	X
monitorPacketsFromPort3	X

Table B-29. Statistics for IxNetwork

	Additional Modes		
	ProtocolServerStats	ArpStats	IcmpStats
Type: Protocol Server - General			
ProtocolServerTx	X		
ProtocolServerRx	X		
TxArpReply		X	
TxArpRequest		X	
TxPingReply			X
TxPingRequest			X
RxArpReply		X	
RxArpRequest		X	
RxPingReply			X
RxPingRequest			X
ProtocolServerVlanDroppedFrames	X		
ScheduledFramesSent			
AsynchronousFramesSent			
PortCPUFramesSent			

Statistics for 1GbE and 10GbE Aggregation Load Modules

In 1GbE Aggregated Mode, the ASM1000XMV12X-01 module has these statistics for ports 1 through 12 (shown in Table B-30). Stats for Port 13 are inactive.

In 10GbE Aggregated Mode, the ASM1000XMV12X-01 module has these statistics for port 13. (shown in Table B-30). The stats in Port 1 to Port 12 are resource only. The active stats are: Central Chip Temperature(C), Port Chip Temperature(C), Port CPU Status, and Port CPU DoD Status.

In Normal mode, the ASM1000XMV12X-01 module statistics are shown in Table B-10 on page B-41. In Normal (non-aggregated) mode only ports 1-12 are active; port 13 is inactive.

Table B-30. Statistics for 1GbE/10GbE Aggregation Load Modules

	1GbE Aggregation	10GbE Aggregation
Ports 1-12		
LinkState	X	Resource only
LineSpeed	X	Resource only
DuplexMode	X	Resource only
FramesSent	X	Resource only
Valid FramesReceived	X	Resource only
Bytes Sent	X	Resource only
Bytes Received	X	Resource only
Port Cpu Status	X	X
Port Cpu Dod Status	X	X
Central Chip Temp (C)	X	X
Port Chip Temp (C)	X	X
Egress Dropped Frames	X	Resource only
Port CPU Ingress Dropped Frames	X	X
Port CPU Frames Received	X	X
Port CPU Bytes Received	X	X
Port 13		
LinkState		X
LineSpeed		X
FramesSent		X
Valid FramesReceived		X
Bytes Sent		X
Bytes Received		X
Egress Dropped Frames		X

Ethernet OAM Statistics

Ethernet OAM statistics are capable of being generated for the load modules listed in Table B-31 on page B-159.

Table B-31.Ethernet OAM Statistics

	Ethernet OAM Stats							
	OAM Information PDUs Sent	OAM Information PDUs Received	OAM Event Notification PDUs Received	OAM Event Notification PDUs Received	OAM Organization PDUs Received	OAM Variable Request PDUs Received	OAM Variable Response PDUs Received	OAM Unsupported PDUs Received
Load Module								
10/100/1000 (S)TX(S)2, 4, 24	X	X	X	X	X	X	X	X
1000 SFP(S)4	X	X	X	X	X	X	X	X
10/100/1000 XMS(R)12	X	X	X	X	X	X	X	X
10/100/1000 LSM XMV(R)4, 16	X	X	X	X	X	X	X	X
10/100/1000 ASM XMV12	X	X	X	X	X	X	X	X
10GE LSM (XM3, XMR3, XL6) in LAN mode	X	X	X	X	X	X	X	X
10GE LSM (XM8, XMR8, XM4, XMR4) in LAN mode	X	X	X	X	X	X	X	X
10GE LSM (XFP, XENPAK, X2, 10GBase-T) in LAN mode	X	X	X	X	X	X	X	X
10G MSM in LAN mode	X	X	X	X	X	X	X	X
10GE LSM MACSec LAN mode	X	X	X	X	X	X	X	X

MACsec Statistics

MACsec statistics can be generated for the LSM10GMS load module and are listed in Table B-32. For details, see *IEEE standard 802.1 AE-2006, Media Access Control (MAC) Security*.

Table B-32. MACsec Statistics

Statistic Type	Name	Description
MACSec Valid Frames Sent	macSecValidFramesSent	32-bit stat counter that indicates the total number valid MACSEC packets transmitted
MACSec Valid Bytes Sent	macSecValidBytesSent	64-bit stat counter that indicates the total numbre valid MACSEC bytes transmitted
MACSec Frames With Unknown Key Sent	macSecFramesWithUnknownKeySent	32-bit stat counter that indicates the total number of transmit packets for which no key was found
MACSec Valid Frames Received	macSecValidFramesReceived	32-bit stat counter that indicates the total number valid MACSEC packets received
MACSec Valid Bytes Received	macSecValidBytesReceived	64-bit stat counter that indicates the total numbre valid MACSEC bytes received
MACSec Frames With Unknown Key Received	macSecFramesWithUnknownKeyReceived	32-bit stat counter that indicates the total number of receive packets for which no key was found
MACSec Frames With Bad Hash Received	macSecFramesWithBadHashReceived	32-bit stat counter that indicates the total number of receive packets with a bad ICV

FCoE Statistics

FCoE statistics can be generated for the NGY LSM10GXM family of load modules and are listed in Table B-33.

Table B-33.FCoE Statistics

Statistic Type	Name
FCoE Fabric Login sent	fcoeFlogiSent
FCoE Fabric Login Link Service Accept received	fcoeFlogiLsAccReceived
FCOE Port Login sent	fcoePlogiSent
FCOE Port Login Link Service Accept received	fcoePlogiLsAccReceived
FCOE Port Login Requests received	fcoePlogiRequestsReceived
FCoE Fabric Logout sent	fcoeFlogoSent
FCOE Port Logout sent	fcoePlogoSent
FCOE Port Logout received	fcoePlogoReceived
FCoE Discovery sent.	fcoeFdiscSent
FCoE Discovery Link Service Accept received	fcoeFdiscLsAccReceived
FCoE Name Server Registration sent	fcoeNSRegSent
FCoE Name Server Registration successful	fcoeNSRegSuccessful
FCoE Nx Ports Enabled	fcoeNxPortsEnabled

Table B-33.FCoE Statistics

Statistic Type	Name
FCoE Nx Port IDs Acquired	fcoeNxPortIdsAcquired
FCoE Rx Shared Stat 1	fcoeRxSharedStat1
FCoE Rx Shared Stat 2	fcoeRxSharedStat2

fcoeRxSharedStat1 and fcoeRxSharedStat2

Select the statistic to be assigned to these two counters from these options::

statFcoeInvalidDelimiter
statFcoeInvalidFrames
statFcoeInvalidSize
statFcoeNormalSizeBadFccRc
statFcoeNormalSizeGoodFccRc
statFcoeUndersizeBadFccRc
statFcoeUndersizeGoodFccRc
statFcoeValidFrames

FIP Statistics

FIP statistics can be generated for any load module capable of FCoE and are listed in Table B-34:

Table B-34.FIP Statistics

Statistic Type	Name
Number of FIP Discovery Solicitations that have been sent	FipDiscoverySolicitationsSent
Number of FIP Discovery Advertisements that have been received.	FipDiscoveryAdvertisementsReceived
Number of FIP Keep Alives that have been sent.	FipKeepAlivesSent
Number of FIP Clear Virtual Links that have been received.	FipClearVirtualLinksReceived

ALM, ELM and CPM Statistics

Statistics generated for ALM1000T8, ELM1000ST2, and CPM1000T8-01 load modules are listed in Table B-35.

Table B-35. Statistics for 10/100/1000 ALM T8, ELM ST2, and CPM T8

	Common	Additional Statistics			
		ArpStats	DHCPv4Stats	DHCPv6Stats	TempSensors Stats
Link State	X				
Line Speed	X				
Duplex Mode	X				

Table B-35. Statistics for 10/100/1000 ALM T8, ELM ST2, and CPM T8

	Common	Additional Statistics			
		ArpStats	DHCPv4Stats	DHCPv6Stats	TempSensors Stats
Frames Sent	X				
Valid Frames Received	X				
Bytes Sent	X				
Bytes Received	X				
Fragments	X				
Undersize	X				
Oversize and Good CRCs	X				
CRC Errors	X				
Alignment Errors	X				
Dribble Errors	X				
Collisions	X				
Late Collisons	X				
Collision Frames	X				
Excessive Collision Frames	X				
Oversize and CRC Errors	X				
ProtocolServer Transmit	X				
ProtocolServer Receive	X				
Transmit ARP Reply		X			
Transmit ARP Request		X			
Transmit Ping Reply	X				
Transmit Ping Request	X				
Receive ARP Reply		X			
Receive ARP Request		X			
Receive Ping Reply	X				
Receive Ping Request	X				
Bits Sent	X				
Bits Received	X				
Central Chip Temperature (C)					X
Port Chip Temperature (C)					X[a]
Port CPU Status	X				
Port CPU DoD Status	X				
DHCPv4 Discovered Messages Sent			X		
DHCPv4 Offers Received			X		
DHCPv4 Requests Sent			X		
DHCPv4 ACKs Received			X		
DHCPv4 NACKs Received			X		
DHCPv4 Releases Sent			X		
DHCPv4 Enabled Interfaces			X		

Table B-35. Statistics for 10/100/1000 ALM T8, ELM ST2, and CPM T8

	Common	Additional Statistics			
		ArpStats	DHCPv4Stats	DHCPv6Stats	TempSensors Stats
DHCPv4 Addresses Learned			X		
DHCPv6 Solicits Sent				X	
DHCPv6 Advertisements Received				X	
DHCPv6 Requests Sent				X	
DHCPv6 Declines Sent				X	
DHCPv6 Replies Received				X	
DHCPv6 Releases Sent				X	
DHCPv6 Enabled Interfaces				X	
DHCPv6 Addresses Learned				X	

a. Not ELM (ALM and CPM only)

40/100 GE Statistics

Table B-36. Statistics for 40/100GE LSM Modules

	Normal				Qos				
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
Type: User Configurable									
UserDefinedStat1	X	X	X	X	X	X	X	X	
UserDefinedStat2	X	X	X	X	X	X	X	X	
CaptureTrigger	X	X	X	X	X	X	X	X	
CaptureFilter	X	X	X	X	X	X	X	X	
StreamTrigger1	X	X	X	X	X	X	X	X	
StreamTrigger2	X	X	X	X	X	X	X	X	
UserDefinedStat5	X	X	X	X	X	X	X	X	
UserDefinedStat6	X	X	X	X	X	X	X	X	
Type: States									
Link	X	X	X	X	X	X	X	X	
LineSpeed	X	X	X	X	X	X	X	X	
TransmitState	X	X	X	X	X	X	X	X	
CaptureState	X	X	X	X	X	X	X	X	
PauseState	X	X	X	X	X	X	X	X	
Type: Common									
FramesSent	X	X	X	X	X	X	X	X	
FramesReceived	X	X	X	X	X	X	X	X	
BytesSent	X	X	X	X	X	X	X	X	
BytesReceived	X	X	X	X	X	X	X	X	
FcsErrors	X	X	X	X	X	X	X	X	
BitsReceived	X	X	X	X	X	X	X	X	
BitsSent	X	X	X	X	X	X	X	X	
PortCpuStatus	X	X	X	X	X	X	X	X	
PortCpuDodStatus	X	X	X	X	X	X	X	X	
ScheduledTransmitTime	X	X	X	X	X	X	X	X	
Type: Transmit Duration									
TransmitDuration	X	X	X	X	X	X	X	X	
Type: Quality of Service									
QualityOfService 0-7					X	X	X	X	
Type: Checksum Stats									
IPv4Packets	X	X	X	X	X	X	X	X	
UdpPackets	X	X	X	X	X	X	X	X	

Table B-36. Statistics for 40/100GE LSM Modules

	Normal				Qos				
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
TcpPackets	X	X	X	X	X	X	X	X	
IPv4ChecksumErrors	X	X	X	X	X	X	X	X	
UdpChecksumErrors	X	X	X	X	X	X	X	X	
TcpChecksumErrors	X	X	X	X	X	X	X	X	
Type: Data Integrity									
DataIntegrityFrames		X				X			
DataIntegrityErrors		X				X			
Type: Sequence Checking									
SequenceFrames			X				X		
SequenceErrors			X				X		
ReverseSequenceErrors			X				X		
SmallSequenceErrors			X				X		
TotalSequenceErrors			X				X		
BigSequenceErrors			X				X		
Type: Ethernet									
Fragments	X	X	X	X	X	X	X	X	
Undersize	X	X	X	X	X	X	X	X	
Oversize	X	X	X	X	X	X	X	X	
VlanTaggedFramesRx	X	X	X	X	X	X	X	X	
FlowControlFrames	X	X	X	X	X	X	X	X	
Type: Temperature									
PCPU FPGA Temperature									X
Capture1 Fpga Temperature									X
Capture2 Fpga Temperature									X
Tx1 Fpga Temperature									X
Tx2 Fpga Temperature									X
Latency1 Fpga Temperature									X
Latency2 Fpga Temperature									X
TxSchedulerOverlay Temperature									X
TxFmx Fpga Temperature									X

Table B-36. Statistics for 40/100GE LSM Modules

	Normal				Qos				
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
RxFmx Fpga Temperature									X
Type: Pause									
PauseEndFrames									
PauseOverwrite	X	X	X	X	X	X	X	X	
Type: Gigabit									
Oversize and CRC Errors	X	X	X	X	X	X	X	X	
Type: POS									
Input Signal Strength	X	X	X	X	X	X	X	X	
Type: ARP									
TxArpReply	X	X	X	X	X	X	X	X	
TxArpRequest	X	X	X	X	X	X	X	X	
RxArpReply	X	X	X	X	X	X	X	X	
RxArpRequest	X	X	X	X	X	X	X	X	
Type: ICMP									
TxPingReply	X	X	X	X	X	X	X	X	
TxPingRequest	X	X	X	X	X	X	X	X	
RxPingReply	X	X	X	X	X	X	X	X	
RxPingRequest	X	X	X	X	X	X	X	X	
ScheduledFramesSent	X	X	X	X	X	X	X	X	
AsynchronousFramesSent	X	X	X	X	X	X	X	X	
PortCPUFramesSent	X	X	X	X	X	X	X	X	
Type: Protocol Server-General									
ProtocolServerTx	X	X	X	X	X	X	X	X	
ProtocolServerRx	X	X	X	X	X	X	X	X	
ProtocolServerVlan DroppedFrames	X	X	X	X	X	X	X	X	
Type: Link Fault Signaling									
LinkFaultState	X	X	X	X	X	X	X	X	
LocalFaults	X	X	X	X	X	X	X	X	
RemoteFaults	X	X	X	X	X	X	X	X	
Type: LSM									
codingErrorFrames Received	X	X	X	X	X	X	X	X	

Table B-36. Statistics for 40/100GE LSM Modules

	Normal				Qos				
	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	Capture	RxDataIntegrity	RxSequenceChecking	RxModeWidePacketGroup	TemperatureSensorsStats
eErrorCharacterFrames Received	X	X	X	X	X	X	X	X	
Type: PCS									
PcsSyncErrorsReceived	X	X	X	X	X	X	X	X	
PcsIllegalCodesReceived	X	X	X	X	X	X	X	X	
PcsRemoteFaultsReceived	X	X	X	X	X	X	X	X	
PcsLocalFaultsReceived	X	X	X	X	X	X	X	X	
PcsIllegalOrderedSet Received	X	X	X	X	X	X	X	X	
PcsIllegalIdleReceived	X	X	X	X	X	X	X	X	
PcsIllegalSofReceived	X	X	X	X	X	X	X	X	
PcsOutOfOrderSof Received	X	X	X	X	X	X	X	X	
PcsOutOfOrderEof Received	X	X	X	X	X	X	X	X	
PcsOutOfOrderData Received	X	X	X	X	X	X	X	X	
PcsOutOfOrderOrderedSet Received	X	X	X	X	X	X	X	X	
TotalFrames	X	X	X	X	X	X	X	X	
ReadTimeStamp	X	X	X	X	X	X	X	X	
Type: Latency/Jitter									
MinLatency	X	X	X	X	X	X	X	X	
MaxLatency	X	X	X	X	X	X	X	X	
MaxminInterval	X	X	X	X	X	X	X	X	
AverageLatency	X	X	X	X	X	X	X	X	
TotalByteCount	X	X	X	X	X	X	X	X	
BitRate	X	X	X	X	X	X	X	X	
ByteRate	X	X	X	X	X	X	X	X	
FrameRate	X	X	X	X	X	X	X	X	
FirstTimeStamp	X	X	X	X	X	X	X	X	
LastTimeStamp	X	X	X	X	X	X	X	X	

C GPS Antenna Installation Requirements

Ixia GPS equipped systems used to provide local Stratum 1 timing signals requires the installation of a GPS antenna kit (942-0003 or 942-0005, where the facility or environment prevent the window mount antenna from functioning). This section describes the installation method we recommend for an IXIA GPS Antenna. This section also provides a scheme for installation of lightning protection for an installed antenna. In order to ensure that all of the following criteria in this manual can be met, we recommend a site survey.

Note: This is not an installation manual and should not be used in place of building codes for electronic installations applicable to specific sites.

This appendix has the following sections:

Roof Mount Antenna

The general location requirements for installation of the GPS antenna and conduit are:

Table C-1. GPS Location Requirements

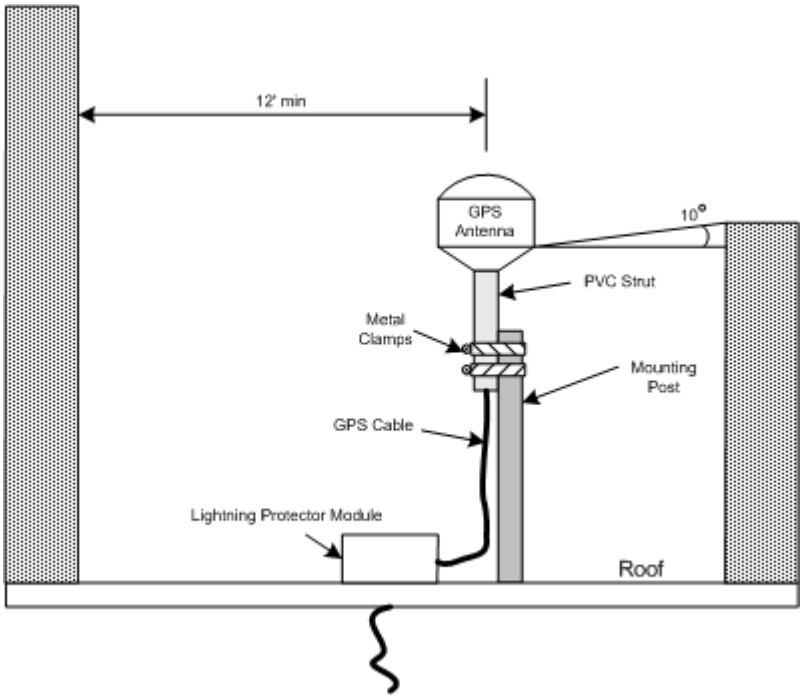
1.	Ideally, a roof area with an unobstructed 360-degree view of the sky above the horizon. At the minimum, a 180-degree view of the sky is required.
2.	Mounted away from and above a plane from items such as elevators, air conditions and other machinery.
3.	Should have the best view of the horizon that is possible. No obstructions should be within a ten-degree angle from the horizontal.
4.	There should be adequate space available on the roof to install two antennas with an absolute minimum of 10 feet between antennas.
5.	The antenna should be 12 feet away from metallic objects.

Table C-1. GPS Location Requirements

6.	Sufficient access to the roof for installation of the GPS conduit/mast and antenna.
7.	Permission to run a 2-inch PVC conduit from the GPS antenna on the roof to the building entrance point.
8.	The coax cable must be connected to the lightning protector (supplied) in the most direct fashion possible, and the lightning protector must be grounded. We recommend that this ground be interconnected to the antenna's tower ground.
	It is very important that the lightning protector be grounded to a low impedance (low R and low L) ground system.

One possible installation is shown in Figure C-1 on page C-2.

Figure C-1. GPS Installation Requirements



The following items are included as part of the Ixia package:

- The GPS Antenna
- GPS Cables (1 long and 1 short)
- Lightning Protector
- The PVC Strut
- Two metal clamps

The placement and construction illustrate many of the recommendations found in this section.

Conduit

We recommend the coax from the GPS antenna to the Ixia unit to be installed in a secure conduit from the point directly above the chassis to the GPS antenna. The conduit serves two purposes:

1. It protects the coax cable.
2. It provides a rigid mast on which the GPS can be mounted.

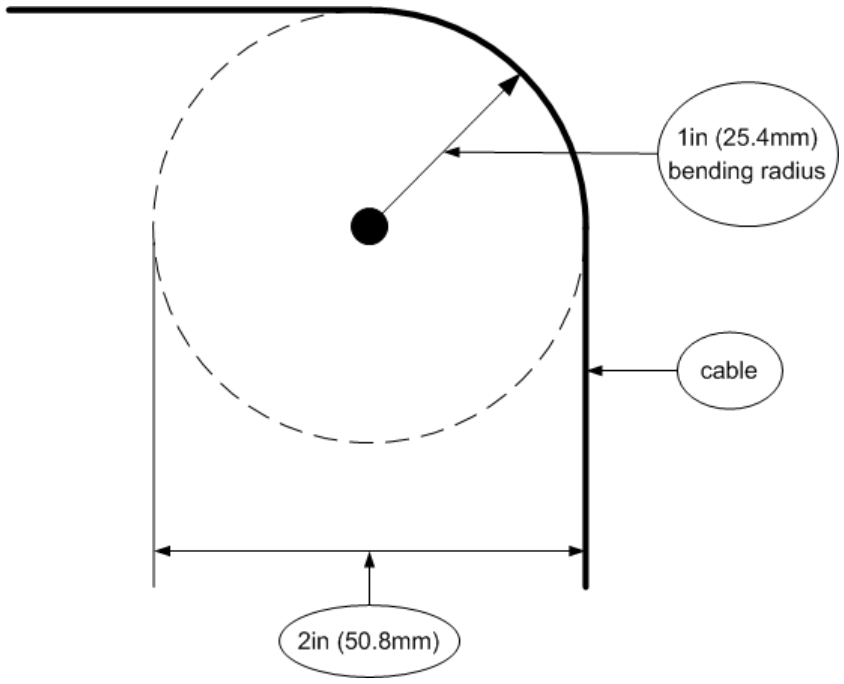
Conduit Type

The GPS conduit should be 2-inch PVC. Installation of the coaxial cable is uncomplicated within the pipe. There should be no more than four 90-degree bends between pull boxes.

Coaxial Bending Radius

The coaxial cable should be run as straight as possible to meet the manufacturer phase stability. The coaxial cable may have a greater than 1in (25.4 mm) bending radius.

Figure C-2. Coaxial Bending Radius



In order to go around a corner a conduit that has less than the required bending radius, it would be necessary to use either a junction box with an accessible elbow installed at each 90-degree turn or two 45-degree elbow connected with a piece of straight pipe. A 2-inch conduit only requires one 90-degree elbow to make the correct bending radius around a 90-degree turn.

Lightning Protection

Lightning protection for the installation is required. The lightning protector must be correctly grounded to function properly. It must be connected to a low

impedance (low R and low L) ground system. We recommend that this ground be interconnected to the tower ground and power ground to form one system.

Note: When attaching to the grounding stud (M8), use a maximum of 88.5 lbf-in. (10 N-m) of torque.

The earth ground electrode should be driven in at least 8 ft. (2.44m) into the earth. A #6 grounding wire should be used.

GPS Mast Location Requirements

Preferred Location

The preferred mounting location for the GPS antenna is an unobstructed 360-degree view of the sky above the horizon. The specific requirements are:

Table C-2. GPS Mast Preferred Location Requirements

1.	Optimal view of the sky.
2.	Not the highest point of the building so as to reduce the possibility of lightning strikes.
3.	Located at least 12 ft. from any large metal objects.
4.	Located at least 10 ft. from any other GPS antenna.
5.	Located within 30 ft. of where the coax cable enters the building.
6.	The GPS antenna mast should be mounted at least 4 feet higher than the highest horizontal **reflective surface** such as roof top mounted AC units.

Requirements if Preferred Location is Not Available

If an unobstructed 360-degree view of the sky is not available then the following requirements should be met:

Table C-3. GPS Mast Location Requirements if a Preferred Location is not Available

1.	300-degree azimuth view of the sky.
2.	No vertical obstructions to obscure the view of the antenna from the horizon for more than 10 degrees.
3.	No high-power radar signal beamed directly at the unit; this may damage the pre-amplifier in the antenna.
4.	No harmonics from a high-power, broad band transmitter within a few megahertz of the carrier frequency (1.575 GHz) should be present. This may jam the GPS receiver.

Window Mount Antenna

The GPS chassis kit includes a window mount antenna. This antenna is capable of operation in areas with a relatively unrestricted view of the sky, and low background interference from other radiators.

Mounting

Mount the antenna on the metal frame of the window. The antenna should be no lower than the lower edge of the glass. A 180-degree view of the sky is preferred, with no buildings adjacent to the window.

In the absence of a metal window frame, a nine centimeter square metal plact can be used to mount the antenna in a position above the window sill.

D Hot-Swap Procedure

Each Optixia chassis provides the ability of removing and reinstalling a Load Module without requiring the removal of power from the rest of the chassis. The process of removing/installing a Load Module does not impact either the operation of the OS or load modules installed in the chassis. The following features are part of the installation/removal process:

- Remove Notification sent to you through IxServer and IxExplorer
- No impact on tests operating on other cards
- Safe power application/removal from the card interface

Legacy modules installed in the SFF adapter module can also be hot-swapped.

Note: The following guidelines should be applied when hot-swapping modules:

- Modules can be hot-swapped in and out of a chassis without impacting server operation only if they are not currently being used to run a test.
- Do not add or remove more than one module at a time.
- Do not add or remove modules during IxServer start up—wait until LCD display shows 'Server OK.'
- 'In Use' LED indicates the module is currently owned by an application. This is to warn of hot-swapping conflicts.

Load Module Hot-Swap Insertion

The process of insertion of a Load Module causes the slot location to apply power to the Load Module and determine that there is no immediate fault condition. The presence of a Load Module in a slot is flagged to IxServer. Upon recognition of a Load Module's presence, IxServer determines if the Load Module is a supported type. All supported types shall be loaded automatically. In all cases, once IxServer has determined the presence of a Load Module in a slot, IxExplorer represents the Load Module as present and advertises the type. For unsupported Load Modules, the module type is shown and is indicated as unsupported in the IxExplorer GUI as long as it resides in a slot.

To insert a load module:

1. Carefully slide the load module along the chassis slot runners until it clicks into place. Ensure that it is firmly connected to the backplane.
2. Secure the holding screws. Be careful not to over tighten the screws.

Note: You should not hot-swap more than one load module at a time into a powered Optixia chassis.

Load Module Hot-Swap Removal

The removal of a load module does not impact the operation of other Load Modules in the chassis with respect to power or independent operation. In the event that an application is using the Load Module, the application operations for that Load Module are terminated and a message is sent to you. In the event that inter-board operations are enabled, the other Load Modules interfacing the removed Load Module are notified of its absence and are instructed to terminate operations to the removed Load Module.

To remove a load module:

1. Loosen the holding screws.
2. Disconnect the load module from the backplane and remove it from the chassis. Be sure to use correct ESD handling procedures at all times.

Note: You should not hot-swap more than one load module at a time into a powered Optixia chassis.

Note: In the event of indications of inadequate power, remove load modules starting from the low-number slots (slot 1, 2, 3), then working upward toward the higher-numbered slots, until the problem is solved.

E IP Port Assignments on Ixia Chassis and Linux port CPUs

Applicability

The information in this bulletin applies to:

- All Ixia chassis
- All Load Modules with embedded Linux port CPUs

Services on Ports

The following table lists the services assigned to IP ports on Ixia chassis and port CPUs as of May 10, 2012. Services listed in the Used on Chassis column are accessed through the chassis management port (the NIC located in the rear of the chassis). Services listed in the Used on Port CPU column are accessed through the test ports.

Note: Do not expose any port on an Ixia chassis to an untrusted network.

Connections are initiated in the following directions:

Table E-1.

Port	Direction
2809 – 2825	client<- ->chassis
2809 – 2825	client<- ->chassis
All others	client ->chassis

Port	Use	TCP	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
9	Discard service	X	X		X	X
21	FTP daemon	X				X
22	SSH (IxLoad)	X		X		
23	Telnet daemon	X			X	X
58	Reserved	X			X	X
80	HTTP, License Management, IxSAN	X		X (IxSAN)	X	X
103	PIM daemon (test port only)	X	X		X	X
111	Sun RPC portmap	X	X	X		X
123	NTP		X	X	X	X
125	Private NTP		X	X		X
135	Windows COM services	X	X	X		X
179	BGP daemon (test port only)	X			X	X
445	Windows COM services	X	X	X		X
797 – 800	NFS mounts		X		X	X
1024 – ?	Windows MStask.exe (Google for 'mstask vulnerability' for details)	X	X	X		X
1080	SOCKS proxy	X		X		X
2048	Service management	X		X	X	
2049	NFS	X	X	X	X	X
2050 – 2111	Service management	X		X	X	
2600 – 26991	Ixia reserved	X			X	X
2705	IxVPN	X			X	X
2782	CliX	X		X		X
2809 – 2825	Aptixia CORBA	X		X		X

Port	Use	TCP	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
3222	File Cabinet port	X		X	X	X
3600 – 39991	Ixia reserved	X			X	X
3705	IxVPN	X			X	X
4501	Licence Management	X		X		X
4555	IxTclServer	X		X		X
4900	VNC	X		X		X
5285	IxServer status connection to IxDodServer	X		X		X
5286	IxServer connection to IxAdmin	X		X		X
5555	IxVPN	X			X	X
6001	Service manager	X		X	X	X
6002	Capture service	X			X	X
6003	Capture service relay	X		X		X
6004	Download on Demand broadcast data		X	X	X	X
6005	Download on Demand server	X		X		X
6101	IxNetwork	X		X	X	
6809 – 6825	Aptixia / CORBA	X			X	X
6665	InterfaceManager (IxAuthenticate & IxAccess)	X			X	X
7768	RPF Impairment	X		X	X	X
8003	IxAuthenticate	X			X	X
8008	IxNetwork	X			X	X
8881	CP/DP	X			X	X
9101 – 9102	Statistics engine (Statengine)	X		X	X	X
9613 – 9676	Service management	X		X	X	X
9888	OTN	X		X		X

Port	Use	TCP	UDP	Used on Chassis	Used on Port CPU	IxOS 5.30 and later
10115	IxChariot	X		X	X	X
17668	IxServer	X		X		X
17669 (4505h)	IxServer	X		X		X
17670 (4506h)	Statistics watch	X		X		X
17671 (4507h)	Protocol watch	X		X		
17672 (4508h)	Port CPU message queue	X		X		X
17674 (450Ah)	Logcollector	X		X		X
17777 (4571h)	Port CPU serial console	X		X		X
26999 – 27009	License Management pre-2.40SP1 (if license server is running on chassis)	X		X		X
27000	License Management 2.40SP1 and later (if license server is running on chassis)	X		X		X
32769	mountd	X		X		X
32800 – 32816	IxVPN CORBA	X			X	X
38001-38096	IxSAN	X			X	X
54321	IxVPN	X		X		X

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