24 IXIA 40/100 Gigabit Ethernet Load Modules

This chapter provides details about Ixia's K2 40-Gigabit and 100-Gigabit Ethernet test modules—the specifications and features.

Ixia's K2 40-Gigabit and 100-Gigabit Ethernet test modules are the world's first IP network traffic generation and layer 2-7 measurement and analysis test solution. K2 load modules are engineered to meet the needs of product teams developing 40 Gb/s and 100 Gb/s network devices such as routers, switches, and communications devices. K2 modules can measure and analyze the performance of Higher Speed Ethernet (HSE) standard-compliant devices at line rate, and are compatible with Ixia's chassis and broad range of 10 Mbps, 100 Mbps, 1 Gbps, and 10 Gbps interfaces, allowing real-world, full product testing in a single box.

Ixia's 40 Gb/s and 100 Gb/s load modules provide network device developers the ability to test 40 GE and 100 GE hardware electronics at full line-rate operation. Early adopters of the HSE technology can use the Ixia test system to validate their compliance with the new PCS lane operation of the IEEE P802.3ba draft standard.

Ixia's K2 load modules are valuable to developers who are integrating firmware and software into new electronics hardware, or integrating optical transceivers into their network devices and systems. Ixia's HSE modules can be used to validate and benchmark the performance limits of these network devices by employing layer 2 and 3 stress testing, virtual scalability testing, and negative testing. Ixia's HSE load modules ensure that a network device is ready to interoperate with other manufacturers' devices that claim compliance to the IEEE P802.3ba draft standard, and facilitate interoperability testing between different vendors of network devices and equipment.

Figure 24-1. 100GE and 40GE LSM XMV Load Modules

Figure 24-2. 40GE LSM XMV QSFP Load Module

Key Features

Industry's first 40 Gb/s and 100 Gb/s Layer 2 through 7 IP test solutions:

- 6 ports per XM12 chassis (10 rack mount units)

  Compatible with XM12 (941-0002) and XM12 High Performance chassis (941-0009)

- 1 port per XM2 (941-0003) desktop chassis

Industry's first commercially available 100 Gb/s Physical Coding Sublayer (PCS) test system:

Provides the ability to check compliance to the IEEE P802.3ba draft standard for both Transmit and Receive sides

Generates and analyzes full 40 Gb/s and 100 Gb/s line rate traffic:

- Tracks and analyzes up to 1 million flows per port for;

- Real-time latency
- Inter-arrival time
- Packet loss
- Data integrity
- Sequence checking
- Packet capture

Ixia's 40 Gb/s and 100 Gb/s load modules are designed for comprehensive layer 2-7 testing with integrated data plane and control plane traffic generation and analysis.

Nomenclature

The LSM HSE family identifying numbers are shown in *Table 24-1*.

Table 24-1. LSM HSE Modules

Load Module	Model Number	Description
40GE LSM XMV1	HSE40GETSP1-01	1-port 40GE, 2-slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications (requires 40GE CFP MSA transceiver).
100GE LSM XMV1	HSE100GETSP1-01	1-port 100GE, 2-slot, full-featured load module. Supports routing protocols, Linux SDK, and L4-7 applications (requires 100GE CFP MSA transceiver).
40/100GE LSM XMV	HSE40/ 100GETSP1-01	1-port, 2-slot, dual-speed, full-featured load module with CFP interface
40GE LSM XMV QSFP	HSE40GEQSFP1-01	1-port, 1-slot, full-featured load module with QSFP interface

Specification are given in Table 24-2..

Table 24-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Number of ports per module	1	1
Number of chassis slots per module	2	1
Maximum ports per chassis	XM12: 6 XM12 High Performance: 6 XM2: 1	
Supported transceivers	CFP MSA Pluggable	QSFP Pluggable

Table 24-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Data Rate	40 Gbps 100 Gbps	40 Gbps
Port CPU Speed and memory	1GHz/2 GB	1GHz/2 GB
Per-port Capture buffer	1.4 GB	700 MB
Interface protocol	40 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 100GBASE-R 100 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 40GBASE-R	40 Gigabit Ethernet per IEEE P802.3ba, Draft 2.0, 100GBASE-R
Ambient Operating Temp. Range	41°F to 95°F (5°C to 35°C) **Note**: Ambient air temperature at the installation site for the system should not exceed 95°F (35°C).	41°F to 95°F (5°C to 35°C) **Note**: Ambient air temperature at the installation site for the system should not exceed 95°F (35°C).
Layer 2/3 routing protocol emulation	Yes	
Layer 4-7 application traffic testing	Yes	
Number of transmit flows per port (sequential)	Billions	
Number of transmit flows per port (arbitrary values)	1 million	
Number of trackable receive flows	1 million	
Captured packet size	49-14,000 bytes	49-14,000 bytes
Number of stream definitions per port	256 In packet stream (sequential) or advanced stream (interleaved) mode, each stream definition can generate millions of unique traffic flows. **Note**: In the Data Center mode, the number of transmit streams is 256.	256
Preamble size	8 bytes	8 bytes
Frame size: min-max (bytes)	49-14,000	49-14,000
Inter-frame gap: min-max	1.8ns - 21.99sec	1.8ns - 21.99sec
Inter-burst gap: min-max	1.8ns - 21.99sec	1.8ns - 21.99sec
Inter-stream gap: min-max	1.8ns - 21.99sec	1.8ns - 21.99sec
Normal stream frame rate	0.045 fps - full line rate	0.045 fps - full line rate

Table 24-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	**HSE40GEQSFP1**
Advanced stream min frame rate	0.091fps	0.091fps
Latency measurements	standard resolution as 20ns user selectable high resolution as 2.5ns	20 nanosecond resolution user selectable high resolution as 2.5ns
Table UDF Entries	1million Comprehensive packet editing function for emulating large numbers of sophisticated flows. Entries of up to 256 bytes, using lists of values, can be specified and placed at designated offsets within a stream. Each list consists of an offset, a size, and a list of values in a table format.	1 million
Max Value List UDF entries	1 million entries for 32-bit and 24-bit, 2 million entries for 8 and 16-bit.	1 million entries for 32-bit and 24-bit, 2 million entries for 8 and 16-bit.
Max Range List UDF entries	N/A	N/A
Packet flow statistics	Track over 1 million flows	
Transmit Engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	
Receive Engine	Wire-speed packet filtering, capturing, real-time latency and inter-arrival time for each packet group, data integrity, and sequence checking	
User defined field features	Fixed, increment, or decrement by user-defined step, value lists, range lists, cascade, random, and chained	
Filters	48-bit source/destination address, 2x128-bit user definable pattern and offset, frame length range, CRC error, data integrity error, sequence checking error (small, big, reverse)	
Data field per stream	Fixed, increment or decrement by user-defined step, value lists, range lists, cascade, random, and chained	

Table 24-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	HSE40GEQSFP1
Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/ received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats, capture trigger (UDS 3), capture filter (UDS 4), user-defined stat 5, user-defined stat 6, 8 QoS counters, data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies	
Error generation	CRC (good/bad/none), undersize, oversize	
MDIO	Ability to calibrate and remove inherent latency from any MSAcompliant 40 Gb/s or 100Gb/s CFP transceiver	
Transmit line clock adjustment	Ability to adjust the parts per million (ppm) line frequency over a range of LAN mode: - 100 to +100 ppm	
Clock In/Out	The load module provides two female SMA coaxial connectors—one for clock input and one for clock output—to allow the device under test (DUT) to frequency-lock with the load module interface. See *Clock In/Out* on page 24-8.	

Table 24-2. HSE Module Specifications

	HSE40GETSP1 HSE100GETSP1 HSE40/100GETSP1	**HSE40GEQSFP1**
Layer 1 BERT capability	The load module supports the following BERT features on both 40 Gb/s and 100 Gb/s speeds: • User selected PRBS pattern for each PCS Lane • User selects from a wide range of PRBS data patterns to be transmitted (true and complement) • Send single, continuous, and exponentially controlled amounts of error injection • Wide range of statistics, including: Pattern Lock, Pattern Transmitted, Pattern Received, Total Number of Bits Sent and Received, Total Number of Errors Sent and Received, Bit Error Ratio (BER), Number of Mismatched 1's and 0's. • Lane Stats Grouping per lambda for SMF and MMF 40 Gb/s and 100 Gb/s based on IEEE802.3ba defined physical medium dependent (PMD).	
Physical Coding Sublayer (PCS) test features	IEEE P802.3ba compliant PCS transmit and receive side test capabilities.	
Per PCS lane, transmit lane mapping	Supports all combination of PCS lane mapping: Default, Increment, Decrement, Random, and Custom.	
Per PCS lane, skew insertion and deskew capability	User selectable from zero up to 3 microseconds of skew insertion on transmit side. Ability to measure deskew up to 6 microseconds on receive side.	
IPv4, IPv6, UDP, TCP	Hardware checksum generation, and verification.	
Frame length controls	Fixed, random, weighted random, or increment by user-defined step, random, weighted random.	
Preamble view	Allows to select to view the preamble in Packet View.	
Link Fault Signaling	Ability to select the option to have the transmit port ignore link faults from a remote link partner.	

Port LEDs

Each 40/100GE port incorporates a set of LEDs, as described in the following tables.

Table 24-3. 40/100GE LSM Port LEDs

LED Label	Usage
Link	Green if Ethernet link is up (established) or the port is in a forced Link Up state, red if link is down. Link may be down due to no signal or no PCS lock.
Tx Active	Green indicates that Tx is active and frames being sent; red indicates Tx is paused; off indicates Tx is not active.
Rx Active	Green indicates that Rx is active and frames being received; red indicates Rx is paused; off indicates Rx is not active.
Rx/Error	Green indicates valid Rx frames are being received; red indicates error frames being received; off indicates no frames being received.
Attention	(Reserved for future use)
Pwr Good	Green when power is on, red if power fault occurs.

Clock In/Out

The load module provides coaxial connectors for clock input and clock output to allow the DUT to frequency-lock with the interface. When running off an external clock, the clock input signal must meet the requirements listed in Table 24-4 to ensure proper performance of the load module.

The clock in/out electrical interface parameters are also defined in Table 24-4.

Table 24-4. Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
Clock Input	Frequency	161.13 MHz ±100ppm
	Duty cycle	50%
	Jitter	±150ps max. cycle to cycle, >1kHz
	Amplitude	Vpp = 4.0
	Impedance	50 ohm ± 5%, DC coupled
	Connector	Female SMA
Clock Output	Frequency	161.13 MHz +/-100ppm (Programmable ppm in Internal Clock Mode)
	Duty cycle	40 to 60%
	Jitter	20ps max cycle to cycle, >1kHz
	Amplitude	0.7Vpp min into 50 ohms, AC coupled output
	Edge rates	200ps to 340ps (20% to 80%) into 50 ohms

Table 24-4. Clock In/Out Electrical Interface Parameters

Parameter		Characteristic
	Impedance	50 ohms +/-5%, AC coupled
	Connector	Female SMA

The load module contains a phase-locked loop (PLL) that reduces the jitter of the input clock, either from the internal or external clock source. The bandwidth of the PLL is approximately 1kHz.

Statistics

Statistics for 40/100GE LSM cards, under various modes of operation may be found in Table B-36 on page B-165.

Intrinsic Latency Adjustment

This option, when present and enabled, reduces the measured latency by the amount of latency that is induced by the test equipment itself (not the DUT). For a specific transceiver, the system retrieves its pre-determined latency value and subtracts this from the measured overall latency. For an ‘unknown’ transceiver (not previously measured), it calculates and stores the intrinsic latency value.

On the **General** tab in **Port Properties**, the **Latency Calibration** option is only enabled for cards with transceivers that have not been pre-measured for intrinisic latency by Ixia. The **Latency Calibration** option is grayed-out if any one of the following conditions are present:

- there is no transceiver
- the transceiver is CFP and a value is found for it in the list of precalibrated values

The **Latency Calibration** option is enabled if the transceiver is CFP but no pre-calibrated value is found in the stored list. The **Latency Calibration** option is also enabled for transceivers that you have previously calibrated, so that the calibration measurement may be repeated (if desired).

Clicking the **Latency Calibration** option runs a Tcl script that measures intrinsic latency and stores the value in an .xml file. The .xml file contains the values that you have produced and saved. Each value is identified for a specific transceiver (per manufacturer, model, and serial number). You can run the calibrate process repeatedly with the same transceiver (if desired). Each new measurement overwrites the previous one for that transceiver.

Running the calibration measurement puts the port into a special loopback mode to measure intrinsic latency. When done, the port is put back into default normal mode. Any port configuration you have set before calibrating intrinsic latency, is lost as the port reverts to a default configuration.

The **Enable** check box is grayed out when no value exists in the system for the specific transceiver. If a value exists in the .xml file, then the **Enable** check box is available. Select the check box to enable the intrinsic latency adjustment.

After the intrinsic latency adjustment has been done, you may want to refresh the chassis or close and reopen the Port Properties dialog.

Multilane Distribution Configuration

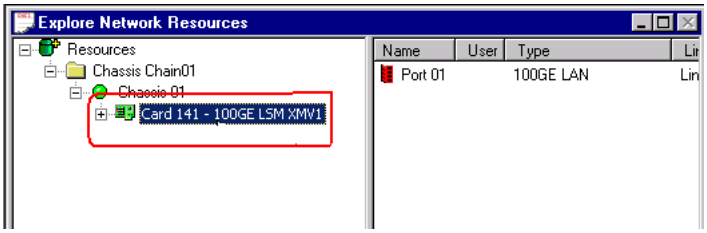
The Tx Lane tab allows to control the PCS (Physical Coding Sublayer) lane configuration and skew. It is part of the Port Properties for the module.

Note: The other tabs in the Port Properties page are described in the *IxExplorer User Guide*, as are the rest of the controls for the module.

To open the Tx Lane tab:

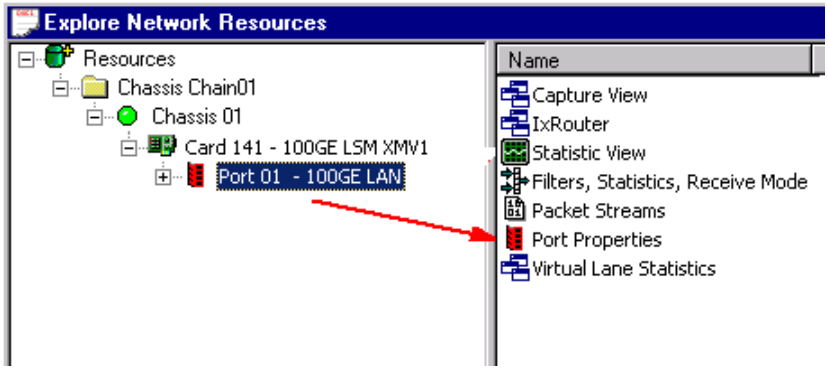
1. Select the 40 or 100GE LSM XMV1 module in the left pane of the IxExplorer window as shown in Figure 24-3.

Figure 24-3. Select Module



2. Expand the node, and select the Port object. In the right window pane, double-click the Port Properties object as shown in Figure 24-4.

Figure 24-4. Port and Port Properties



3. In the Port Properties dialog, select the Tx Lane tab. Use this tab to control the PCS lane order and the skew for each lane.

The Tx Lane tab is shown in Figure 24-5.

Figure 24-5. Tx Lane Tab

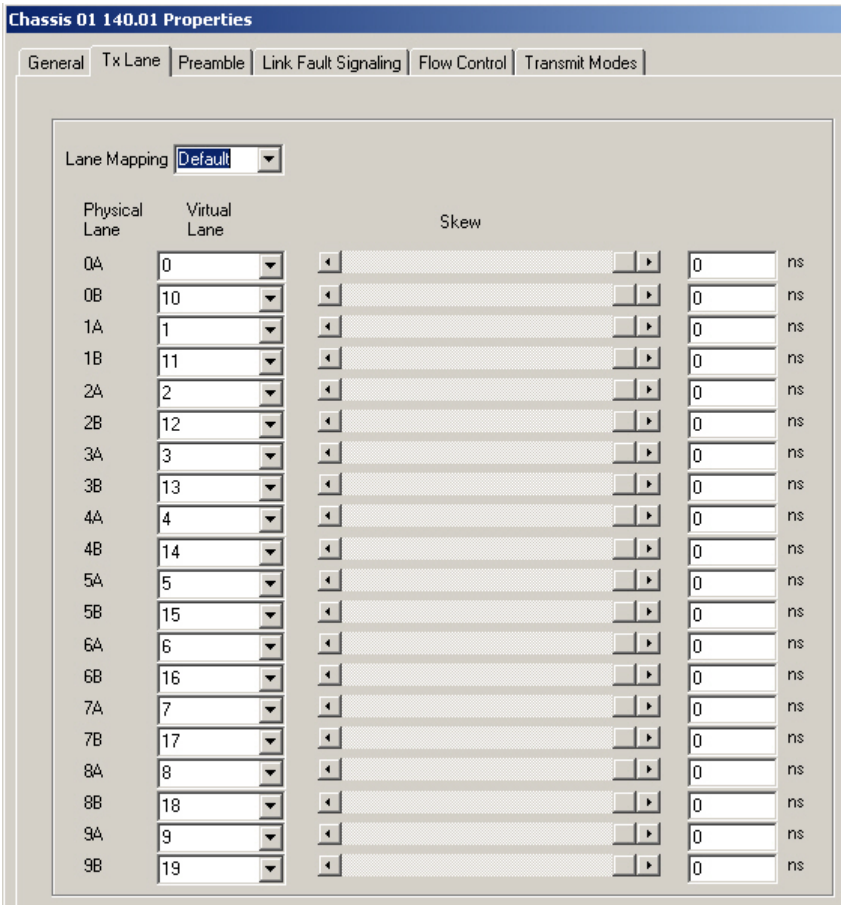


Table 24-5 explains the options in the Tx Lane tab page.

Table 24-5. Tx Lane Tab Configuration

Field	Description
Lane Mapping	Allows you to select a PCS lane ordering method. There are four options: • Default: The default ordering method. The default order is each physical port corresponds to 2 PCS lanes that are n and n+10, where n = physical lane number. • Increment: Orders the lanes from 0 to 19, straight down the list. • Decrement: Orders the lanes from 19 to 0, straight down the list. • Custom: Allows to put the lanes in any order by manually entering the numbers in the fields. The starting order is the last selected mapping.
Physical Lane	The physical lane identifier. The physical lane is paired with a corresponding PCS lane.

Table 24-5. Tx Lane Tab Configuration

Field	Description
PCS Lane	A number identifier for the PCS lane. The PCS lane is paired with a corresponding physical lane.
Skew	The skew slider is used to set a skew value for the PCS lane, in nanoseconds, on the transmit side. Lane Skew is the ability to independently delay one or more of the 20 PCS lanes. When the slider is moved, the nanoseconds field is correspondingly adjusted. You can also enter a nano second value directly into this field. When the slider is fully pushed to the right, the skew injected into the transmit stream is 0 (minimum). When the slider is pushed all the way to the left. the skew injected into the transmit stream is 3 uS (maximum).

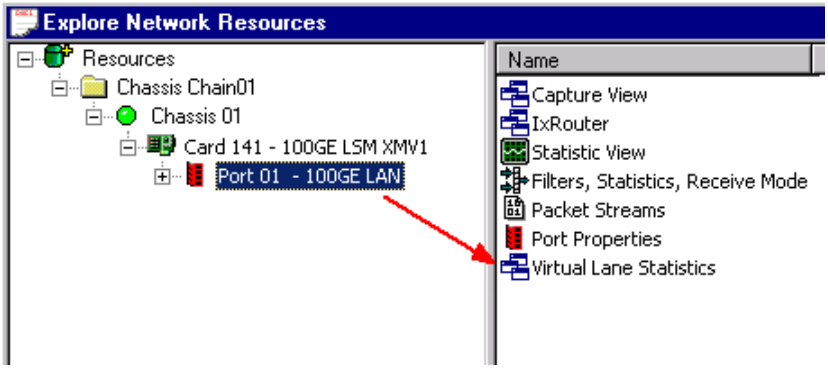
PCS Lane Statistics

The PCS lane statistics table allows to view the statistics for the configured PCS lanes.

To open the PCS lane statistics table:

1. Select the 40 or 100GE LSM XMV1 module in the left pane of the IxExplorer window as shown in Figure 24-3.
2. Expand the node, and select the Port object. In the right window pane, double-click the PCS lane statistics object as shown in Figure 24-6.

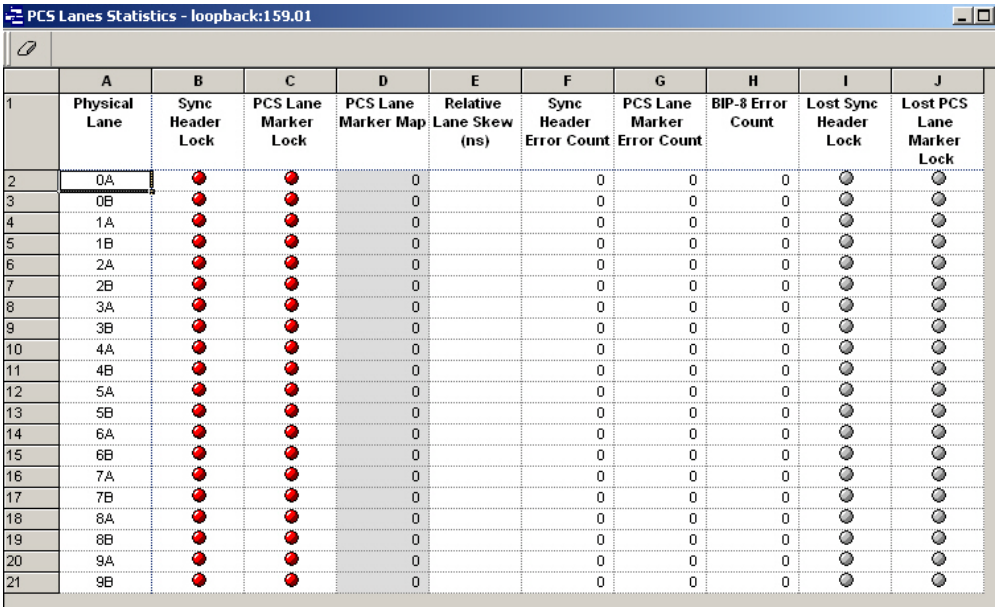
Figure 24-6. Port and PCS Lane Statistics



3. The PCS lane statistics table opens. Use this table to view the PCS lane statistics for each lane. The statistics are for the **receive** side.

The PCS lane statistics table is shown in Figure 24-7.

Figure 24-7. PCS Lane Statistics Table



	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0		0	0	0		
3	0B			0		0	0	0		
4	1A			0		0	0	0		
5	1B			0		0	0	0		
6	2A			0		0	0	0		
7	2B			0		0	0	0		
8	3A			0		0	0	0		
9	3B			0		0	0	0		
10	4A			0		0	0	0		
11	4B			0		0	0	0		
12	5A			0		0	0	0		
13	5B			0		0	0	0		
14	6A			0		0	0	0		
15	6B			0		0	0	0		
16	7A			0		0	0	0		
17	7B			0		0	0	0		
18	8A			0		0	0	0		
19	8B			0		0	0	0		
20	9A			0		0	0	0		
21	9B			0		0	0	0		

Table 24-6 explains the entries in the PCS lane statistics table.

Table 24-6. PCS Lane Statistics Data

Field	Description
Physical Lane	The identifier for the Receive physical lane. This is a tag/ fixed label to ID each lane.
Sync Header Lock	Indicates if the received PCS lane achieved sync-bit lock. Green indicates success, red failure.
PCS Lane Marker Lock	Indicates if the received PCS lane has achieved alignment marker lock. Green indicates success, red failure.
PCS Lane Marker Map	The PCS lane number identified by the alignment marker. This is only valid when PCS Lane Marker Lock is green.
Relative Lane Skew (ns)	Shows the actual skew in nanoseconds. Skew measurements are valid only when all lanes are locked with 20 unique lane markers. The first PCS Lane markers to arrive have skew of 0. All other lane skews are relative to them.
Sync Header Error Count	The number of synchronization bit errors received.
PCS Lane Marker Error Count	The number of incorrect PCS lane markers received while in PCS lane lock state.
BIP-8 Error Count	Bit interleaved parity error count. It detects the number of BIP-8 errors for a PCS lane.

Table 24-6. PCS Lane Statistics Data

Field	Description
Lost Sync Header Lock	When lit, indicates the loss of sync header lock since the last statistic was read. If colored gray, there is no error. If colored red, an error has occurred.
Lost PCS Lane Marker Lock	When lit, indicates the loss of PCS lane marker lock since the last statistic was read. If colored gray, there is no error. If colored red, an error has occurred.